

Project Overview

Computer Architecture



CS3501 - 2025I

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Executive Summary

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- **Motivation:** We implemented a microprocessor in lab.
- **Problem:** We need to extend functionality in our design.
- **Overview:**
 - Project description.
 - Project goals and guideline.
- **Conclusion:** We implemented a complete microprocessor during CS3501.

Outline

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Introduction

Goals

Guideline

Arch Project

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- Define teamworks for the final Project.
 - Up to 2 members.
- For starting:
 - Recall: Verilog and ASM.
 - Recall: Topics from ISA to Microarchitecture.
 - Recall: Floating Point Arithmetic.

Outline

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Introduction

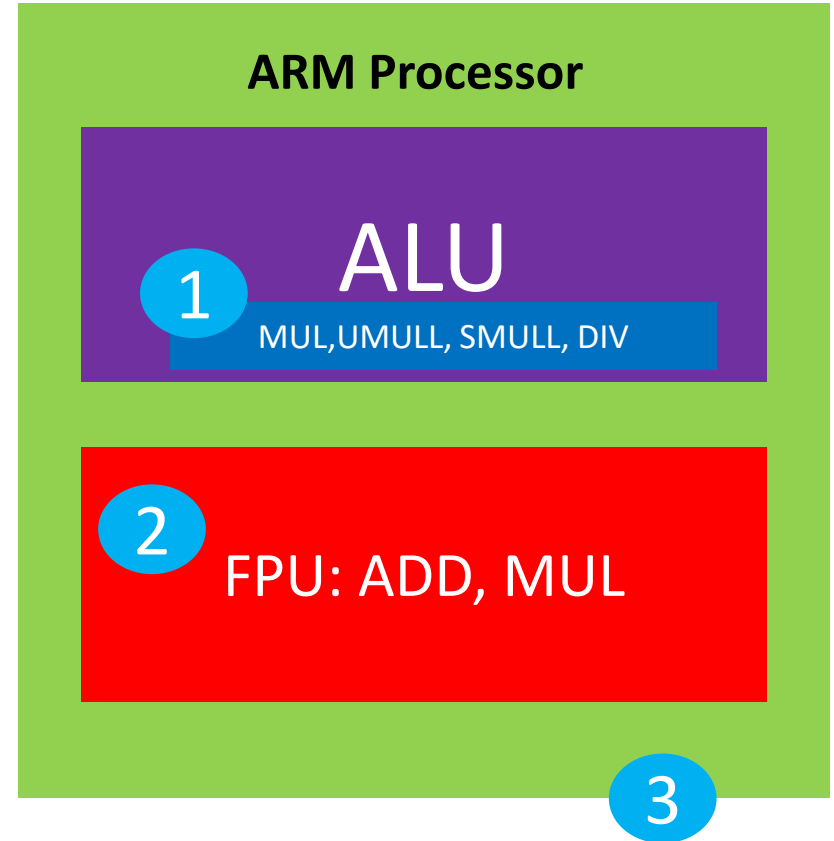
Goals

Guideline

Final Project

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1. **Implement the following multiplication operations:**
 - MUL, UMULL, SMULL, DIV
2. **Extend the functionality of the microprocessor with a Floating Point Unit (FPU).** Implement for single-precision (32-bit) and half-precision (16-bit) the following operations, as a separate block from ALU.
 - ADD and MUL.
 - Solve overflow by defining flag value.



Tasks:

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1. Implement a testing program in ASM that requires MUL, UMULL, SMULL. **Requirements:** 1) define an useful function, 2) implement a testbench for the ALU.
2. Implement a testing program in ASM that requires FP ADD or MUL. Requirements: 1) define a function that makes sense, 2) implement a testbench for the FP unit.
3. **Implement the required hardware in Verilog:** 1) INT MUL units 2) FP ADD and MUL units.
 1. Add and test with the multicycle processor.
4. Prepare an oral presentation, report and answer questions from the instructor following the deadlines explained in rubrica.docx.

Outline

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Goals

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Instructions

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- **P0 Report:**

- Complete the Control Unit of the Multi-cycle processor.
 - Complete the datapath module.
 - Test that the instructions from the Single Cycle Challenge work correctly.
 - Implement and test the MUL instruction.
 - Submit a short report describing how you implemented your microprocessor, including results and your code (Your code will be checked for plagiarism).
- **Upload a P0.zip file** with a folder with: a) Verilog project with comments, b) pdf report.
 - **Follow the instructions to not lose points.**

Instructions

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- **P1 Presentation:**

- Implement and test the UMUL, SMUL, and DIV instructions.
 - Create an ASM program that uses these instructions.
 - Create a testbench and verify these instructions in Verilog.
 - Submit a short report describing how you implemented your microprocessor, including results and your code (Your code will be checked for plagiarism).
 - Prepare a 10-minute presentation explaining how your Multi-cycle microprocessor works and how the new instructions are implemented.
- **Upload a P1.zip file** with a folder with: a) Verilog project with comments, b) ppt slides.
 - **Follow the instructions to not lose points.**

Instructions

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- **P2 Final:**

- Implement and test the Floating Point instructions.
 - Create an ASM program that uses these instructions.
 - Create a testbench and verify these instructions in Verilog.
 - Implement your microprocessor in the FPGA.
 - Submit your final report describing how you implemented your microprocessor, including results and your code (Your code will be checked for plagiarism).
 - Prepare a 15-minute presentation explaining how your Multi-cycle microprocessor works, how the new instructions are implemented, and the FPGA implementation.
- **Upload a P1.tar file** with a folder with: a) Verilog project with comments, b) pdf report, c) ppt slides.
 - **Follow the instructions to not lose points.**

Grading

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- P0 Multicycle with MUL – Report (02pts)
- P1 MUL, UMUL, SMUL, DIV – Presentation (03pts)
- P1 Final Presentation + Final Report + testing on Basys3 (16pts)
- **Important:**
 - Show your progress at Checkpoint (lab sessions): enables presentation and assign grading points.

Conclusions

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- **We implemented a microprocessor in Arch CS3501.**
- **Project has three main activities:**
 - 1) **Modified ALU with multiplication support.**
 - 2) **Implementation of an additional FPU unit for ADD/MUL.**
 - 3) **Test the previous designs with the ARM processor.**
- **Deadline on Canvas (previous week to E2).**

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