3. MMU

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Table of Contents

1 Enable cache 3
1.1 common/cmd_cache.c for the cache commands 3
1.2 Compile cmd_cache.c 3
1.3 Enable the cache commands 3
1.4 Enable dcache(disabled by default) 3
1.5 Check icache and dcache are enabled 4
2 Check the speed when the cache is on and off 5
2.1 icache(Instruction cache) 5
2.2 dcache(Data cache) 5
3 Cache in MMU page table 6
4 Cache in memory map 7

1 Enable cache

1.1 common/cmd_cache.c for the cache commands

cmd_cache.c[1]

1.2 Compile cmd_cache.c

`common/Makefile`

```
obj-$(CONFIG_CMD_CACHE) += cmd_cache.o
```

1.3 Enable the cache commands

```
menu my_commands
config CMD_CACHE
        bool "cache"
        default y
        help
                cache
```

1.4 Enable dcache(disabled by default)

This doesn't work

```
config SYS_DCACHE_OFF
        bool "Do not use Data Cache"
        default n
```

In this file

u-boot-2016.01 > include > configs > C s5p6818_bitminer.h

Change this

```
/* board_init_f, CONFIG_SYS_ICACHE_OFF */
#define CONFIG_SYS_DCACHE_OFF
```

1 https://project.coasia.com/confluence/download/attachments/2076084061/cmd_cache.c?api=v2&modificationDate=1707896830761&version=1

to this

```
/* board_init_f, CONFIG_SYS_ICACHE_OFF */
// #define  CONFIG_SYS_DCACHE_OFF
```

1.5 Check icache and dcache are enabled

```
bitminer# icache
Instruction Cache is ON
bitminer# dcache
Data (writethrough) Cache is ON
```

2 Check the speed when the cache is on and off

2.1 icache(Instruction cache)

1. icache on
2. mw.l 0x7A000000 0x00FF0000 614400 (This is fast)
3. icache off
4. mw.l 0x7A000000 0x00FF0000 614400 (This is slow)

2.2 dcache(Data cache)

```
static void do_test_cache(void)
{
    ulong start_time, end_time;
    printf("Testing cache speed...\n");
    start_time = get_timer(0); // Start timer
    unsigned long long i=1, result=0;
    for(i=1; i<=87654321; i++)
        result += i % 2;
    end_time = get_timer(start_time); // End timer
    printf("Time taken: %lu ms\n", end_time);
    printf("Result: %d\n", result);
}
```

```
bitminer# dcache on
bitminer# test_cache
Testing cache speed...
Time taken: 328 ms
Result: 43827161
bitminer# dcache off
bitminer# test_cache
Testing cache speed...
Time taken: 1095 ms
Result: 43827161
```

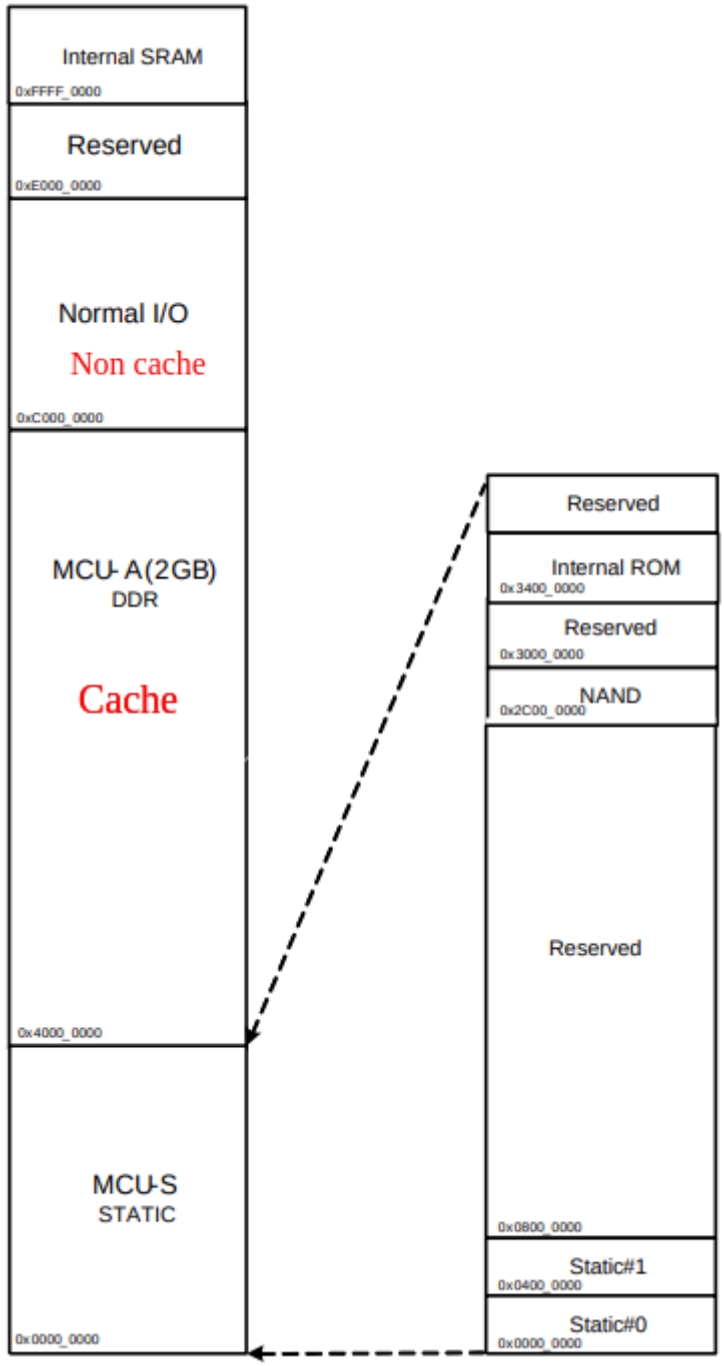
3 Cache in MMU page table

`arch/arm/lib/cache-cp15.c`

```
__weak void dram_bank_mmu_setup(int bank)
{
    debug("%s: bank: %d\n", __func__, bank);
    for (i = bd->bi_dram[bank].start >> 20;
         i < (bd->bi_dram[bank].start >> 20) + (bd->bi_dram[bank].size >> 20);
         i++) {
#if defined(CONFIG_SYS_ARM_CACHE_WRITETHROUGH)
        set_section_dcache(i, DCACHE_WRITETHROUGH);
#elif defined(CONFIG_SYS_ARM_CACHE_WRITEALLOC)
        set_section_dcache(i, DCACHE_WRITEALLOC);
#else
        set_section_dcache(i, DCACHE_WRITEBACK);
#endif
    }
}
```

This code modifies cache attributes in MMU's page table entries

4 Cache in memory map



- SRAM is a cache itself
- DRAM is cacheable for faster speed

- Memory-mapped I/O should be non-cacheable for data consistency (Bits in memory-mapped I/O should not be stored in cache because cache is not mapped to the I/O targets