APB bus 양영식

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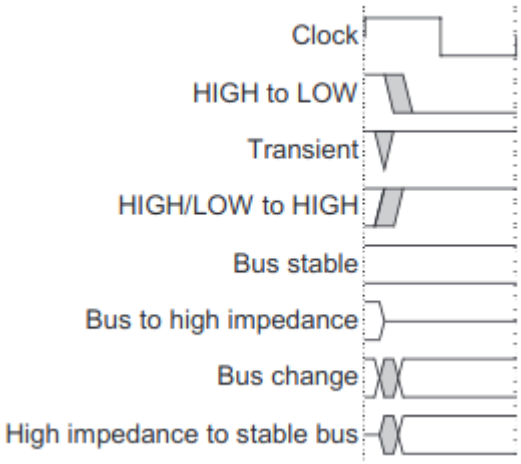
1 APB

The APB (Advanced Peripheral Bus) is part of the AMBA (Advanced Microcontroller Bus Architecture) suite of protocols.
AMBA is a widely used interconnection standard for connecting functional blocks (like CPUs, memory units, and peripherals).

- **Purpose**: APB is designed for low-bandwidth control accesses, for example, peripheral device control. Its primary use is to connect simple peripherals to the primary bus, which could be an AHB (Advanced High-performance Bus) or AXI (Advanced eXtensible Interface) bus in the AMBA standard.
- **Simplicity and Efficiency**: The APB is simpler compared to other buses in the AMBA family. It is optimized for minimal power consumption and reduced complexity of peripherals. This makes it ideal for simple, lower-speed tasks where high throughput is not a critical requirement.
- **Use Cases**: APB is commonly used for interfacing with low-speed peripherals like keyboards, mouse devices, UARTs, SPI (Serial Peripheral Interface) controllers(control signals don't require high speed).

2 Prior knowledge

2.1 Timing diagram conventions



- **Bus change**: This indicates that multiple bits on the bus are changing simultaneously aside from just a single binary digit changing
- **Transient**: This is a temporary, intermediate state during the transition of a signal from one stable state to another. It's a period where the signal is neither high nor low
- **Bus to high impedance**: This shows the bus moving to an electrical disconnection. This state is used when multiple devices can drive the bus, but only one should do so at a time to avoid conflicts.

2.2 APB signal descriptions

4.1 AMBA 3 APB signals

Table 4-1 lists the APB signal descriptions.

Table 4-1 APB signal descriptions

Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of **PCLK** times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a **PSELx** signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when **PWRITE** is HIGH. This bus can be up to 32 bits wide.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when **PWRITE** is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the **PSLVERR** pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

2.3 2.1 Write Transfers

Write transfers can be categorized into two types:

- With no wait states
- With wait states

2.3.1 2.1.1 With no wait states

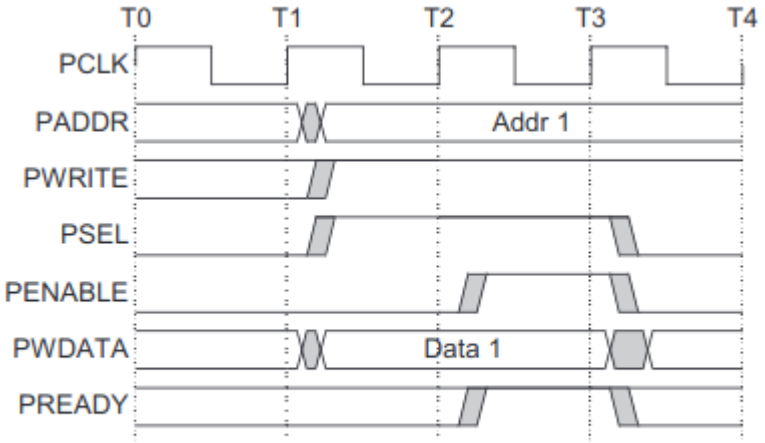


Figure 2-1 Write transfer with no wait states

- **At T0**: The process is idle, waiting for the next clock cycle.
- **T1**: The address (`PADDR`) and write data (`PWDATA`) become valid, and the write signal (`PWRITE`) and select signal (`PSEL`) are asserted.
- **T2-T3**: The `PENABLE` signal is asserted, indicating the Access phase is in progress, during which the address and data remain valid.
- **T4**: The `PENABLE` signal is deasserted, marking the end of the transfer. If another transfer is not immediately following, `PSEL` goes LOW.

The transfer completes at the end of this cycle, with all signals remaining valid throughout the Access phase.

2.3.2 2.1.2 With wait states

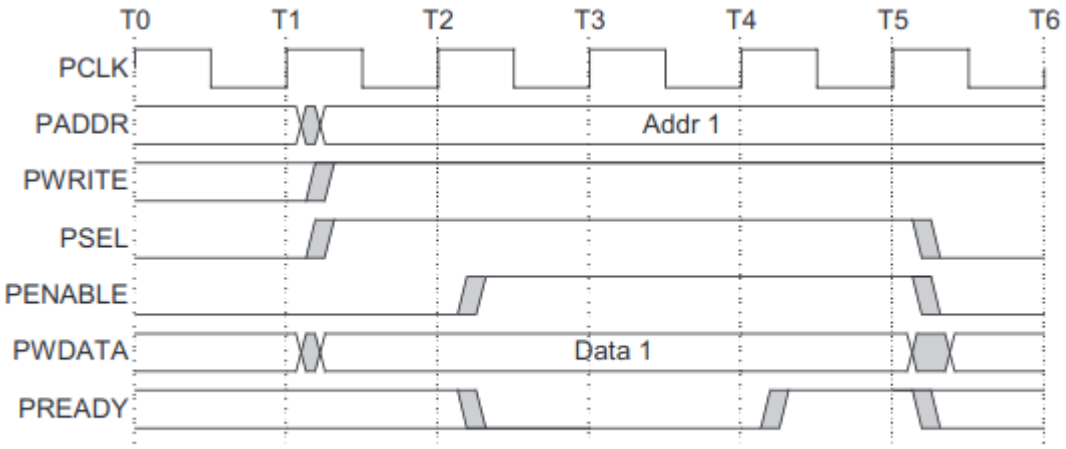


Figure 2-2 Write transfer with wait states

The `PREADY` signal can extend the transfer by driving `PREADY` LOW when `PENABLE` is HIGH.

- **T2-T4**: The `PENABLE` signal is asserted, but the `PREADY` signal goes LOW, indicating the wait states.

> *Note: It is recommended that the address and write signals remain stable until another access occurs to reduce power consumption.*

2.4 2.2 Read transfers(same as write)

The timing of the signals is similar to the write transfer(as described in `Write transfers` on section 2.1) but is oriented towards reading data from a slave device.

2.4.1 2.2.1 With no wait states

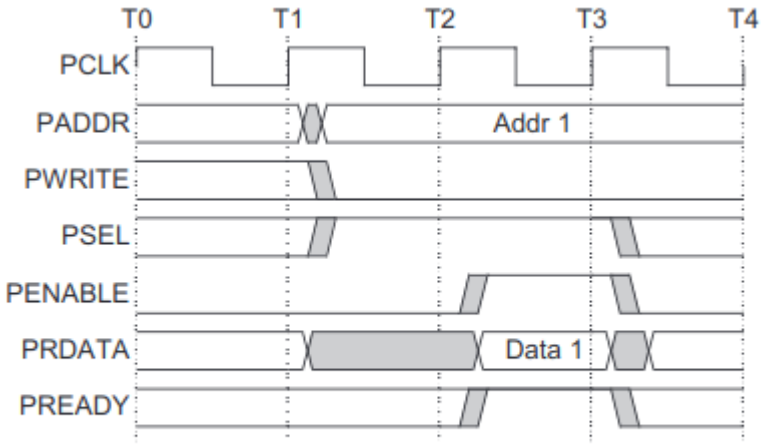


Figure 2-3 Read transfer with no wait states

2.4.2 2.2.2 With wait states

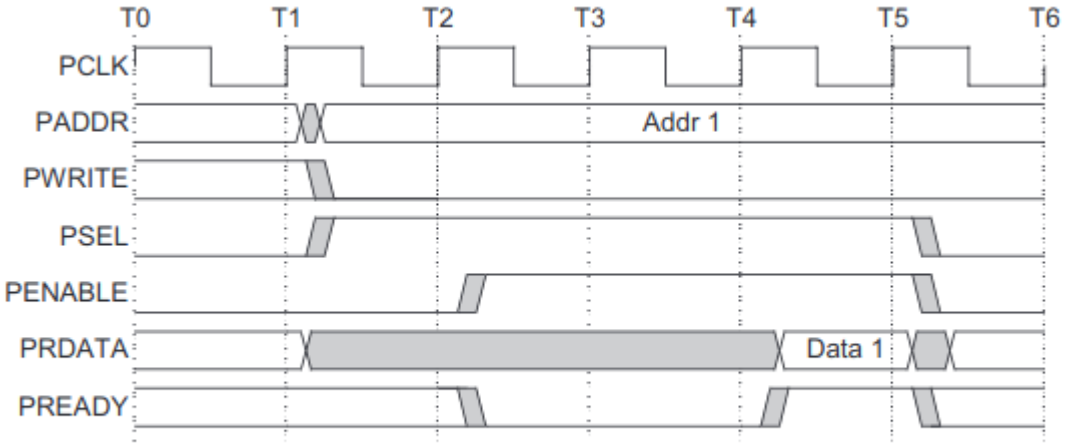


Figure 2-4 Read transfer with wait states

2.5 2.3 Error response

- **PSLVERR**: It's a signal used to indicate an error during an APB transfer.
- **Validity**: PSLVERR is valid only during the last cycle of an APB transfer when PSEL, PENABLE, and PREADY are all HIGH.

- **Recommendation**: It's suggested to drive PSLVERR LOW when not being sampled, i.e., when any of PSEL, PENABLE, or PREADY are LOW.
- **Either behavior**: Whether an error changes the state of the peripheral is peripheral-specific and either behavior is acceptable.

2.5.1 2.3.1 Failing transfer

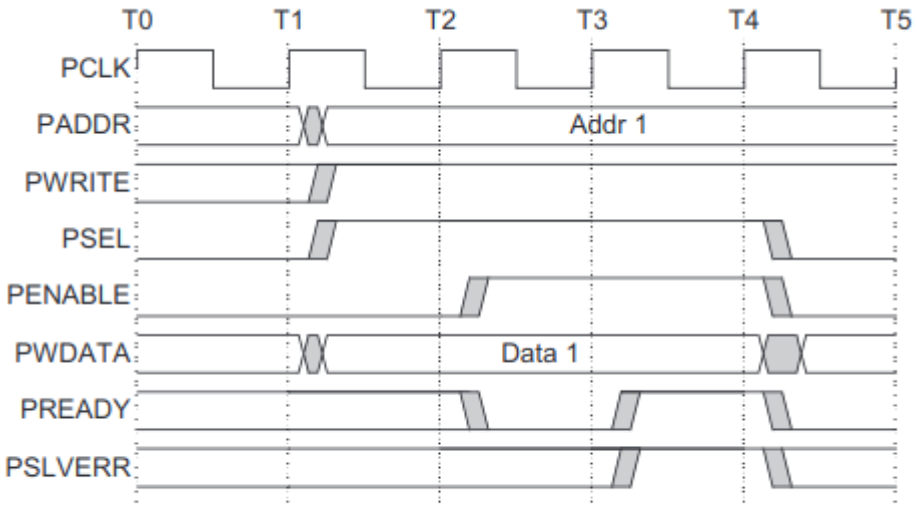


Figure 2-5 Example failing write transfer

The high PSLVERR indicates that there has been an error during the transfer.

2.5.2 2.3.3 Mapping of PSLVERR

- **AXI to APB:** An APB error is mapped back to RESP/BRESP = SLVERR. This is done by mapping PSLVERR to the AXI signals RRESP[1] for reads and BRESP[1] for writes.
- **AHB to APB**: PSLVERR is mapped back to HRESP = ERROR, achieved by mapping PSLVERR to the AHB signal HRESP[0].

2.6 3.1 Operating States

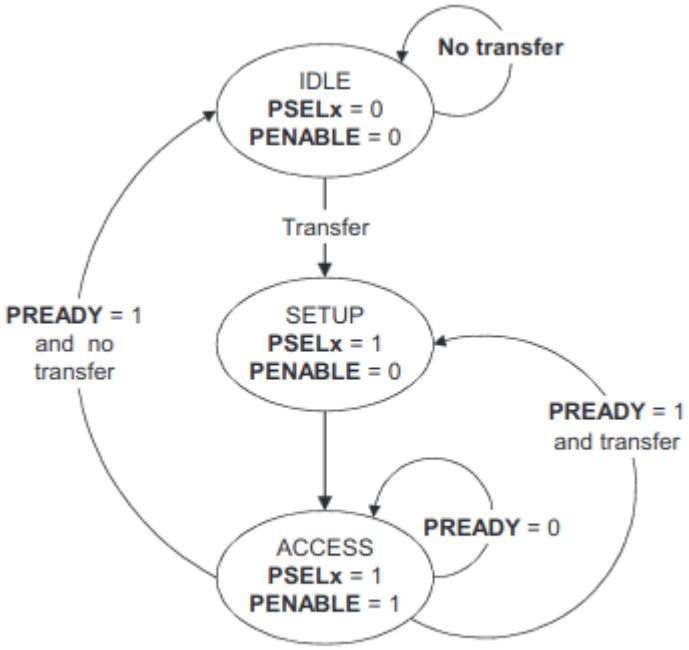


Figure 3-1 State diagram

This diagram visually represents the transitions between the different states of the APB state machine. It shows:

- **IDLE**: The default state of the APB when no transfers are occurring.
  - **To SETUP**: When a transfer is required, the bus moves into the `SETUP` state.
- **SETUP**: The peripheral select signal `PSELx` is asserted, indicating which peripheral is being communicated with.
  - **To ACCESS**: The bus only remains in this state for one clock cycle and moves to the `ACCESS` state on the next clock's rising edge.
- **ACCESS**: The enable signal `PENABLE` is asserted in the `ACCESS` state. Stable signals(address, write, select, and write data) are crucial during the transition from SETUP to ACCESS. The exit from the ACCESS state is dependent on the PREADY signal from the peripheral (slave device).
  - **Remaining in ACCESS**: If `PREADY` is low, the bus remains in the `ACCESS` state.
  - **Exit from ACCESS**: If `PREADY` is high, the bus either returns to the `IDLE` state if no more transfers are needed ***OR*** moves directly to the `SETUP` state if another transfer is pending.