

Vadivel Murugan

15+ years of experience in software design and programming. Passionate about product design optimizations with strong customer focus.

LinkedIn: [Vadivel](#)
Masters, Electrical
Engineering,
San Jose State.

vadivelmurugank@gmail.com
(510) 386-5613
Newark, CA

- ❑ Cloud experience with Ericsson Cloud Platform, Docker Containers, Openstack neutron and Nova.
- ❑ User Plane(UPF) development with Data Plane Development Kit (DPDK) and Kubernetes, Openvswitch.
- ❑ Forwarding Plane programming skills with SAI, Openflow and P4.
- ❑ Working knowledge in L2/L3 Overlay protocols with GRE, MIM, TRILL.
- ❑ Time sensitive protocols with PTP Telecom Boundary networks.
- ❑ Multicore Embedded systems and Real Time operating system services.
- ❑ OpenSource Projects Contributions and development.
- ❑ Programming expertise in C, Python and x86_64/VT-x. Programming skills in C++/STL and ARMv8 Assembly.

Cisco Systems Inc, San Jose, CA — *Technical Lead*

June 2018 - Current

Accomplishments

- Pioneered IEEE 1588 1-step ptp design with kernel timestamping for L2, Vlan and L3 Multicast based boundary clocks.
- Achieved < 200 nano seconds with 1000+ ptp sessions with Broadcom Jericho based platform.
- Achieved Class B Timing (<40ns) with integration of Microsemi Servo controller and Time synchronization algorithm.

Contributions

- Designed mechanisms to profile longevity clock performances, and statistical analysis to determine PTP correction outliers.
- Integration with 5G Timing for Telecom boundary clock (ITU 8275.1).

PTP/1588v2, BMCA
ITU 8275.1, G.8262
T-GM, T-BC
CPRI, PRTC, vDU
FH-TOR, Edge, MBH

Jericho2 Dual Pipeline
L2/L3, 802.1Q
Multicast

PHY/MAC/Serdes
Microsemi Servo
Timestamping
DPLL
PDV and Corrections
SYNCE and 1PPS

Ericsson Inc, Santa Clara, CA — *Technical Lead*

April 2013 - May 2018

Accomplishments

- Improved OpenVswitch/DPDK performance with vEPG Apps by 40% with hyperscaling PMD threads and rte ring buffers. Aligning CPU Pinning and NUMA awareness for Intel Niantic 10G and Fortville 25G.
- Customized openstack neutron ovs plugin and ML2 plugin driver for Ericsson cloud platform. Provisioning of Kubernetes and openvswitch interfaces.
- Optimized Exact match cache and megaflo cache with openflow ACLs.
- Developed Virtual Function (VF) and Physical Function (PF) interfaces using SR-IOV for homogeneous access of Data plane fabric and FPGA components in Xen Hypervisor Domo platform.

Contributions

- Bootstrap Control Plane Processor, Data Plane Spider NPU, and Switch Fabric of 40x10G/4x100G line card.
- Integration of uboot, mini-kernel, linux drivers, and Configuration of Non Transparent PCI Bridge, FPGA, core and serdes PLL, power and fantray modules.
- Resolve Packet drops, credit assignments and calendar resolution, and link partner negotiations.

User Plane(UPF)
Pipeline

Ericsson Cloud
Platform
OpenVswitch, DPDK
Kubernetes, Docker,
QEMU, KVM, SR-IOV

Openstack
Neutron and Nova,
HEAT Engine

vEPG Apps, NFV, DPI
Service Chaining

FPGA, Serdes
Linux, uboot

Intel SmartNIC
Niantic, Fortville
Columbiaville
Mellanox ConnectX

<p>Broadcom Corporation Inc, San Jose, CA — Sr. Staff Engineer October 2010 - April 2013</p> <p>Accomplishments</p> <ul style="list-style-type: none"> Improved efficiency of memory table reads and writes with design and implementation of chunked Memory support. Add regex compiler optimizations and configurations of Deep Packet Inspection (DPI) flow table. <p>Contributions</p> <ul style="list-style-type: none"> Design and Implementation of Wireless LAN CAPWAP Tunnel SDK Interfaces and support roaming configurations. Design and Development of 1588 one-step and two-step time stamping and synchronization modules. Development of L2 Tunneling Protocol for MAC-in-MAC, TRILL and GRE. Maintenance of QOS, VLAN and PLL Programming interfaces. 	<p>Xgs, Trident2, Triumph3</p> <p>BCM SDK MAC, PHY, Serdes PCI, Table DMA, TCAM</p> <p>Mac-in-MAC, TRILL GRE QOS, VLAN Wireless LAN CAPWAP Tunnel and Virtual Ports</p>
<p>Wind River Systems, Alameda, CA — Sr. Software Engineer December 2006 - October 2010</p> <p>Accomplishments</p> <ul style="list-style-type: none"> Design and Implementation of x86_64 dynamic instrumentation (sensorpoint) manager, which includes trap and jmp instrumentation for linux kernel and VxWorks Design and Development of MIPS Linux Kernel exception redirects. Memory optimizations for dynamic memory pool stack and replenishments Memory atomic operations and data allocations. <p>Contributions</p> <ul style="list-style-type: none"> Development of exception redirect handler for PPC and X86_VT Hypervisor. Development of MIPS and ARM static/shared library loader to load instrumented binary stubs. Maintenance of ARM and MIPS stack walk, trace back mechanisms. 	<p>WindRiver Linux Vxworks Eclipse</p> <p>Compiler and AST Sensor and Patch points</p> <p>Linux Kernel and exception redirects Hypervisor X86_64 and VT-x</p>
<p>Open Source Projects</p> <ul style="list-style-type: none"> Inspectshow : Deep inspection of python internals. CallTree : API Call tree with sources. apiParse : Pattern based API parsing. 	<p><u>Github Projects</u></p> <p>Python programming Python Inspect</p> <p>Parsing and Call Tree</p>
<p>Past Projects</p> <p>WIPRO Technologies, (May 2000 - Nov 2006), Bangalore, India</p> <ul style="list-style-type: none"> Development of 802.11b and WindRiver Vxworks Drivers. Developed Windriver Vxworks BSP for ARMv6 based network boards. Design and Development of L2 switch, STP Protocol for Wireless LAN Access point. <p>Embedded Resources Private Limited, (Jan 1999 - May 2000), Pune, India</p> <ul style="list-style-type: none"> Development of Solaris, pSOS Network DPLI Drivers. Implemented Solaris and pSOS PNA+ Loop back network driver and DLPI STREAMS Driver, and added promiscuous and multicast features <p>Academic Projects</p> <ul style="list-style-type: none"> Master's Project work involved Development of Zigbee Down conversion Receiver based on 45nm Technology. The project involved development of LNA, Filter, Balun and Mixer modules which operated between 2.4-2.483Mhz for channels 11-26. Bachelor's Project work involved Development of Fuzzy logic based temperature controller with inputs from industrial pH and temperature sensors. 	<p>TCP/IP VxWorks BSP L2 Switch and STP Wireless LAN</p> <p>MultiCore Embedded Programming</p> <p>pSOS and DLPI Streams</p> <p>ZigBee , LNA Filter, Mixer</p> <p>Fuzzy Logic Industrial Automation</p>