

Vadivel Murugan

Envisioning to Architect, Incubate and develop virtual platforms and services, for software defined networks.

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Engineering, San Jose State.

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15+ years of experience in software design and programming. Technical Lead roles in Edge Router and Data center platforms. Passionate about product design optimizations with strong customer focus.

Cisco Systems Inc, San Jose, CA — Technical Lead

June 2018 - Current

Development and support of *Cisco Nexus Data center router platform*. Lead time sensitive protocols and customer deployments.

Ericsson Inc, Santa Clara, CA — Technical Lead

April 2013 - May 2018

Development of Ericsson *Smart Service Edge Routers* and Ericsson Virtual Routing platform and *Ericsson cloud platform*

Broadcom Corporation Inc, San Jose, CA — Sr. Staff Engineer

October 2010 - April 2013

Development and support of Broadcom SDK interfaces and Silicon-On-Chip driver interfaces for 32x40G/100+x10G (BCM56850/Trident2), 240Gb/s Switch (BCM56640/Triumph3), HiGig2 Switch (bcm88732/shadow)

Wind River Systems, Alameda, CA — Sr. Software Engineer

December 2006 - October 2010

Development and support of Multicore WindRiver Linux and vxWorks embedded platform.

User Plane(UPF) with
DPDK, Kubernetes,
Docker Containers,
OpenVswitch.

Ericsson Cloud Platform
QEMU, KVM, vEPG Apps,
vDU, 5G, CPRI

Openstack
Neutron and Nova

L2/L3 overlay protocols
GRE, MIM, TRILL.

ASIC programming with
SAI, Openflow and P4.
Deep Packet Inspection
(DPI) Services.

Time sensitive protocols
with PTP/1588 and
Telecom boundary
networks.

Multicore Embedded
systems and Windriver
Linux.

Programming skills in C,
Python, x86_64/VT-x

Cisco Systems Inc

Accomplishments

- Pioneered IEEE 1588 1-step ptp design with kernel timestamping for L2, Vlan and L3 Multicast based boundary clocks.
- Achieved less than 200 nano seconds with 1000+ ptp sessions with Broadcom Jericho based platform.
- Designed mechanisms to profile longevity clock performances, and statistical analysis to determine PTP correction outliers.
- Achieved Class B Timing (<40ns) with integration of Microsemi Servo controller and Time synchronization algorithm.
- Integration with **5G Timing for Telecom boundary clock** (ITU 8275.1).

PTP/1588v2, BMCA
ITU 8275.1, G.8262
T-GM, T-BC
CPRI, PRTC, vDU
FH-TOR, Edge, MBH

Jericho2 Dual Pipeline
L2/L3
802.1Q
Multicast

PHY/MAC/Serdes
Microsemi Servo
Timestamping
DPLL
PDV and Corrections
SYNCE and 1PPS

Ericsson Inc

Accomplishments

- Improved **OpenVswitch/DPDK performance** with vEPG Apps by 40% with hyperscaling PMD threads and rte ring buffers. Aligning CPU Pinning and NUMA awareness for Intel Niantic 10G and Fortville 25G.
- Customized openstack neutron ovs plugin and ML2 plugin driver for **Ericsson cloud platform**. Provisioning of **Kubernetes and openvswitch** interfaces.
- Optimized Exact match cache and megaflow cache with openflow ACLs.
- Developed **Virtual Function (VF) and Physical Function (PF)** interfaces using **SR-IOV** for homogeneous access of Data plane fabric and FPGA components in Xen Hypervisor Domo platform.

Contributions

- Bootstrap Control Plane Processor, Data Plane Spider NPU, and Switch Fabric of 40x10G/4x100G line card.
- Integration of uboot, mini-kernel, linux drivers, and Configuration of Non Transparent PCI Bridge, FPGA, core and serdes PLL, power and fantray modules.
- Resolve Packet drops, credit assignments and calendar resolution, and link partner negotiations.

OpenVswitch, DPDK
Kubernetes, Docker
containers
QEMU,
KVM,
SR-IOV

Openstack
Neutron and Nova,
HEAT Engine

vEPG Apps,
NFV
Service Chaining,
DPI.

User Plane(UPF) Pipeline
FPGA, Serdes
Linux, uboot

Intel SmartNIC
Niantic, Fortville
Columbiaville
Mellanox ConnectX

Broadcom Corporation

Accomplishments

- Improved efficiency of memory table reads and writes with design and implementation of chunked Memory support.
- Add regex compiler optimizations and configurations of **Deep Packet Inspection (DPI)** flow table.

Contributions

- Design and Implementation of Wireless LAN CAPWAP Tunnel SDK Interfaces and support roaming configurations.
- Design and Development of 1588 one-step and two-step time stamping and synchronization modules.
- Development of L2 Tunneling Protocol interfaces for MAC-in-MAC, TRILL and GRE.
- Maintenance of QOS, VLAN and PLL Programming interfaces.

Xgs, Trident2, Triumph3

BCM SDK
MAC, PHY, Serdes
PCI, Table DMA, TCAM

Mac-in-MAC, TRILL
GRE

QOS, VLAN
Wireless LAN CAPWAP
Tunnel and Virtual Ports

WindRiver Systems Inc

Accomplishments

- Design and Implementation of x86_64 dynamic instrumentation (sensorpoint) manager, which includes trap and jmp instrumentation for linux kernel and VxWorks
- Design and Development of MIPS Linux Kernel exception redirects.
- Hash Algorithm and Memory optimizations for dynamic memory pool stack and replenishments.
- Memory optimizations of data allocations and atomic operations.

Contributions

- Development of exception redirect handler for PPC and X86_VT Hypervisor.
- Development of MIPS and ARM static/shared library loader to load instrumented binary stubs.
- Maintenance of ARM and MIPS stack walk, trace back mechanisms.

WindRiver Linux
Vxworks
Eclipse

Compiler and AST
Sensor and Patch points

Linux Kernel and
exception redirects
Hypervisor
X86_64 and VT-x

Past Projects

WIPRO Technologies, (May 2000 - Nov 2006), Bangalore, India

- Development of 802.11b and WindRiver Vxworks Drivers.
- Developed Windriver Vxworks BSP for ARMv6 based network boards.
- Developed 802.11b wireless device stack and access point in Linux
- Design and Development of L2 switch and STP Protocol for Wireless LAN Access point.

Embedded Resources Private Limited, (Jan 1999 - May 2000), Pune, India

- Development of Solaris, pSOS Network DPLI Drivers.
- Implemented Solaris and pSOS PNA+ Loop back network driver and DLPI STREAMS Driver, and added promiscuous and multicast features

TCP/IP
Network Driver
VxWorks BSP
L2 Switch and STP
Wireless LAN

RTOS
Embedded Programming

pSOS and DLPI Streams
Multicast

Academic Projects

- Master's Project work involved Development of Zigbee Down conversion Receiver based on 45nm Technology. The project involved development of LNA, Filter, Balun and Mixer modules which operated between 2.4-2.483Mhz for channels 11-26.
- Bachelor's Project work involved Development of Fuzzy logic based temperature controller with inputs from industrial pH and temperature sensors.

ZigBee
LNA
Filter
Mixer

Fuzzy Logic
Industrial Automation

Open Source Projects

[Github Projects](#)

- Inspectshow : Deep inspection of python internals.
- Peekextn : Dictionary of file extensions from sources.
- CallTree : API Call tree with sources.
- apiParse : Pattern based API parsing.

Python programming
Python internals
Decorators and Iterators

Parsing and Call Tree