

Vadivel Murugan

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Envision

Envisioning to architect and develop optimized platform and programmable framework for Software Defined Networks and Multicore Silicon.

Summary

- **Passionate** about kernel programming, design optimizations, and statistical analysis.
- **Expertise** in IEEE1588/PTP Stack, ASIC Switch Programming, Network Virtualization with OpenStack, Sensor networks and Wireless LAN.
- **15+ years (Aug 1999 - Current) of experience in software design and programming for Edge Router Platform and network switch silicon Ingress/Egress pipelines.**
 - Technical Leader, Cisco Systems Inc (Jun 2018 - Curr), San Jose, US
 - Technical Lead, Ericsson Inc (Apr 2013 - May 2018), Santa Clara, US
 - Sr. Staff Engineer, Broadcom Corporation (Oct 2010 - April 2013), San Jose, US
 - Senior Software Engineer, WindRiver Systems (Dec2006 - Oct 2010), Alameda, US
 - Senior Software Engineer, Wipro Technologies (May 2000 - Nov 2006), Bangalore, India
- **Programming** expertise in C, Python and X86_64/VT-x, Programming Skills in C++/STL and ARMv8 Assembly.
- **Forwarding** plane development with Intel DPDK and openVswitch. Forwarding Plane programming skills with Openflow and P4.
- **Development** of Broadcom SDK APIs and Deep packet Inspection regex programming.
- Master of Science (MS), Electrical Engineering, San Jose State University.

Significant Contributions

CISCO SYSTEMS INC

- Involved in development and support of Cisco Nexus Data center router platform.
 - Pioneered IEEE1588 1-step ptp design with kernel timestamping for L2, Vlan and L3 Multicast based boundary clocks.
 - Achieved less than 200 nano seconds with 1000+ ptp sessions with Broadcom Jericho based platform.
 - Designed mechanisms to profile longevity clock performances, and statistical analysis to determine PTP corrections and Time interval variance.
 - Achieved Class B Timing (<40ns) with integration of Microsemi Servo controller and Time synchronization algorithm.
 - Involved in 5G Timing integration for Telecom boundary clock (ITU 8275.1) solutions.

ERICSSON INC

- Involved in development of Ericsson Smart Service Edge Routers and Ericsson Virtual Routing platform.
 - Improved OpenVswitch/DPDK performance by 40% with hyperscaling PMD threads and rte ring buffers, CPU Pinning and NUMA awareness for Intel Niantic 10G and Fortville 25G.
 - Customized openstack neutron ovs plugin and ML2 plugin driver for Ericsson cloud platform.

- Optimized Exact match cache and megaflow cache with openflow ACLs.
- Developed Virtual Function (VF) and Physical Function (PF) interfaces for homogeneous access of Data plane fabric and FPGA components in Xen Hypervisor Dom0 platform.
- Bootstrap Control Plane Processor, Data Plane Spider NPU, and Switch Fabric of 40x10G/4x100G line card.
- Integration of uboot, mini-kernel, linux drivers, and Configuration of Non Transparent PCI Bridge, FPGA, core and serdes PLL, power and fantray modules.
- Hardware Configurations with Shmoo of DDR4 SDRAM, TLB Mapping of non-transparent PCI bridge slave devices, eTCAM Slice Configuration and Nor-flash Memory Map.
- Extend 12x10G PHY to 1x100G (4x25G) PHY configurations and SFI lane mappings.
- Integrate open source linux modules with third party SDK, and derive solutions to resolve namespace collisions and initialization sequences.
- Isolate hardware and software issues related to Core PLL, PCI Gen3 hot plug, I2C, GPIO, MDIO, Serdes and PHY.
- Resolve Packet drops, credit assignments and calendar resolution, and link partner negotiations.

BROADCOM CORPORATION

- Involved in development and support of Broadcom SDK interfaces and Silicon-On-Chip driver interfaces for 32x40G/100+x10G (BCM56850/Trident2), 240Gb/s Switch (BCM56640/Triumph3), HiGig2 Switch (bcm88732/shadow)
 - Design and implementation of chunked Memory support for efficient memory table reads and writes.
 - Add regex compiler optimizations and configurations of Deep Packet Inspection (DPI) flow table.
 - Design and Implementation of Wireless LAN CAPWAP Tunnel SDK Interfaces and support roaming configurations.
 - Design and Development of 1588 one-step and two-step time stamping and synchronization modules.
 - Development of L2 Tunneling Protocol interfaces for MAC-in-MAC, TRILL and GRE.
 - Maintenance of QOS, VLAN and PLL Programming interfaces.

WINDRIVER SYSTEMS

- Involved in WindRiver Linux platform framework and tools development.
 - Hash Algorithm and Memory optimizations for dynamic memory pool stack and replenishments.
 - Design and Implementation of x86_64 dynamic instrumentation (sensorpoint) manager, which includes trap and jmp instrumentation for linux kernel and VxWorks
 - Design and Development of MIPS Linux Kernel exception redirects.
 - Memory optimizations of data allocations and atomic operations.
 - Developed of exception redirect handler for PPC and X86_VT Hypervisor.
 - Developed MIPS and ARM static/shared library loader to load instrumented binary stubs.
 - Maintenance of ARM and MIPS stack walk, trace back mechanisms.

PAST PROJECTS

WIPRO TECHNOLOGIES - Development of 802.11b and WindRiver Vxworks Drivers.

- Developed Windriver Vxworks BSP for ARMv6 based network boards.
- Developed 802.11b wireless device stack and access point in Linux
- Design and Development of L2 switch and STP Protocol for Wireless LAN Access point.

EMBEDDED RESOURCES PRIVATE LIMITED - Development of Solaris, pSOS Network DPLI Drivers.

- Implemented Solaris and pSOS PNA+ Loop back network driver and DLPI STREAMS Driver, and added promiscuous and multicast features.

ACADEMIC PROJECTS

- Master's Project work involved Development of Zigbee Down conversion Receiver based on 45nm Technology. The project involved development of LNA, Filter, Balun and Mixer modules which operates between 2.4-2.483Mhz for channels 11-26.
- Bachelor's Project work involved Development of Fuzzy logic based temperature controller with inputs from industrial pH and temperature sensors.

OPEN SOURCE PROJECTS

- [Inspectshow](#) : Deep inspection of python internals.
- [Peekextn](#) : Dictionary of file extensions from sources.
- [CallTree](#) : API Call tree with sources.
- [apiParse](#) : Pattern based API parsing.