

Vadivel Murugan

Technical Lead Professional with 15+ years in networking, cloud and multi-core linux kernel

Github : [OpenSource Projects](#)
Masters, Electrical Engineering,
San Jose State University.

LinkedIn: [Vadivel](#)
vadivelmurugank@gmail.com
+1 (510) 386-5613, Newark, CA

Networking Experience in Software Development for Switches and Routers.

- Cisco nxos platform and time synchronization development for Broadcom Dune Fabric Jericho and Jericho2 ASICs
- Telecom profile and Ipv6 ptp multicast and unicast support for Cisco Cloudscale ASIC.
- Pioneered **1588 1-step ptp** design with kernel timestamping for L2, Vlan and L3 Multicast based boundary clocks.
- Broadcom SDK development for Broadcom Xgs pipelines, Trident2 and Triumph3 ASICs.
- Design and Implementation of **Wireless LAN CAPWAP Tunnel** SDK Interfaces.
- L2/L3 Overlay protocols with GRE, MIM, TRILL.
- PTP integration with **5G Timing for Telecom boundary clock** (ITU 8275.1)

Cloud Experience in Openstack and Docker Containers.

- Cloud experience with Ericsson Cloud Platform, **Docker Containers**, **Openstack neutron** and **Nova**.
- User Plane(UPF) development with **Data Plane Development Kit (DPDK)** for **Kubernetes** and **Openvswitch**.
- Development of **Virtual Function (VF)** interfaces using SR-IOV to access Data plane fabric.
- Hyperscale PMD threads with NUMA awareness for **Intel SmartNIC Forville** and **Mellanox ConnectX**.
- OpenStack Forwarding Plane programming skills with **SAI**, **Openflow** and **P4**.

Core Experience with Multicore platform and Linux Kernel

- **Linux Kernel Instrumentation** and **BSP** for ARM and X86_64 Multicore.
- Exception Redirect framework for **VxWorks Hypervisor**.
- Vxworks and WindRiver **Linux Multicore operating system** services.

Programming expertise in C, C++ and Python

- **OpenSource Project Contributions** in python and linux kernel.

Cisco Systems Inc, San Jose, CA — *Engineering Technical Leader*

June 2018 - Current

Accomplishments

- **Pioneered IEEE 1588 1-step ptp design** with kernel timestamping for **L2, Vlan and L3 Multicast** based boundary clocks.
- **Achieved < 200 nano seconds** with 1000+ ptp sessions with Broadcom Jericho based platform.
- **Achieved Class B Timing (<40ns)** with integration of Microsemi Servo controller and Time synchronization algorithm.

Contributions

- Designed mechanisms to profile longevity clock performances, and statistical analysis to determine PTP correction outliers.
- PTP Ipv6 Stack and Integration with **5G Timing for Telecom boundary clock** (ITU 8275.1)

PTP/1588v2, BMCA
ITU 8275.1, G.8262
T-GM, T-BC
CPRI, PRTC, vDU
FH-TOR, Edge, MBH

Jericho2 Dual Pipeline
L2/L3, 802.1Q
Multicast

PHY/MAC/Serdes
Microsemi Servo
Timestamping
DPLL

PDV and Corrections
SYNCE and 1PPS

C, Python, gdb
Ixia, Calnex, Microsemi

Ericsson Inc, Santa Clara, CA — <i>Technical Lead</i>	April 2013 – May 2018	User Plane(UPF) Pipeline
Accomplishments		Ericsson Cloud Platform OpenVswitch, DPDK Kubernetes, Docker, QEMU, KVM, SR-IOV
<ul style="list-style-type: none"> Improved OpenVswitch/DPDK performance with vEPG Apps by 40% with hyperscaling PMD threads and rte ring buffers. Aligning CPU Pinning and NUMA awareness for Intel Niantic 10G and Fortville 25G. Customized openstack neutron ovs plugin and ML2 plugin driver for Ericsson cloud platform. Provisioning of Kubernetes and openvswitch interfaces. Optimized Exact match cache and megaflow cache with openflow ACLs. Developed Virtual Function (VF) and Physical Function (PF) interfaces using SR-IOV to access Data plane fabric and FPGA in Xen Hypervisor Domo platform. 		Openstack Neutron and Nova, HEAT Engine
Contributions		vEPG Apps, NFV, DPI Service Chaining
<ul style="list-style-type: none"> Bootstrap Control Plane Processor, Data Plane Spider NPU, and Switch Fabric of 40x10G/4x100G line card. Integration of uboot, mini-kernel, linux drivers, and Configuration of Non Transparent PCI Bridge, FPGA, core and serdes PLL, power and fantray modules. Resolve Packet drops, credit assignments and calendar resolution, and link partner negotiations. 		FPGA, Serdes Linux, uboot
Broadcom Corporation Inc, San Jose, CA — Sr. Staff Engineer		October 2010 – April 2013
Accomplishments		Xgs, Trident2, Triumph3
<ul style="list-style-type: none"> Improved efficiency of memory table reads and writes with design and implementation of chunked Memory support. Add regex compiler optimizations and configurations of Deep Packet Inspection (DPI) flow table. 		BCM SDK MAC, PHY, Serdes PCI, Table DMA, TCAM
Contributions		Mac-in-MAC, TRILL GRE
<ul style="list-style-type: none"> Design and Implementation of Wireless LAN CAPWAP Tunnel SDK Interfaces and support roaming configurations. Design and Development of 1588 one-step and two-step time stamping and synchronization modules. Development of L2 Tunneling Protocol for MAC-in-MAC, TRILL and GRE. Maintenance of QOS, VLAN and PLL Programming interfaces. 		QOS, VLAN Wireless LAN CAPWAP Tunnel and Virtual Ports
		C, Shell Scripts Ixia, Workbench, Emulation
Wind River Systems, Alameda, CA — Sr. Software Engineer		December 2006 – October 2010
Accomplishments		WindRiver Linux Vxworks Eclipse
<ul style="list-style-type: none"> Design and Implementation of x86_64 dynamic instrumentation (sensorpoint) manager, which includes trap and jmp instrumentation for linux kernel and VxWorks Design and Development of MIPS Linux Kernel exception redirects. Memory optimizations for dynamic memory pool stack and replenishments Memory atomic operations and data allocations. 		Compiler and AST Sensor and Patch points
Contributions		Linux Kernel and exception redirects Hypervisor X86_64 and VT-x
<ul style="list-style-type: none"> Development of exception redirect handler for PPC and X86_VT Hypervisor. Development of MIPS and ARM static/shared library loader to load instrumented binary stubs. Maintenance of ARM and MIPS stack walk, trace back mechanisms. 		

Open Source Projects

[Github Projects](#)

- Inspectshow : Deep inspection of python internals.
- CallTree : API Call tree with sources.
- apiParse : Pattern based API parsing.

Python Inspect

Parsing and Call Tree

Past Projects

WIPRO Technologies, (May 2000 – Nov 2006), Bangalore, India

- Development of 802.11b and WindRiver Vxworks Drivers.
- Developed Windriver Vxworks BSP for ARMv6 based network boards.
- Design and Development of L2 switch, STP Protocol for Wireless LAN Access point.

TCP/IP
VxWorks BSP
L2 Switch and STP
Wireless LAN

MultiCore
Embedded Programming

Embedded Resources Private Limited, (Jan 1999 – May 2000), Pune, India

- Development of Solaris, pSOS Network DPLI Drivers.
- Implemented Solaris and pSOS PNA+ Loop back network driver and DLPI STREAMS Driver, and added promiscuous and multicast features

pSOS and DLPI Streams

Academic Projects

Master of Science (MS) Electrical Engineering, 2010 – 2012

San Jose State University, San Jose, CA

- Master's Project work involved Development of Zigbee Down conversion Receiver based on 45nm Technology. The project involved development of LNA, Filter, Balun and Mixer modules which operated between 2.4–2.483Mhz for channels 11–26.

ZigBee , LNA
Filter, Mixer

Bachelor of Electronics Engineering, 1994 – 1998

Shivaji University, Kolhapur, India

- Bachelor's Project work involved Development of Fuzzy logic based temperature controller with inputs from industrial pH and temperature sensors.

Fuzzy Logic
Industrial Automation