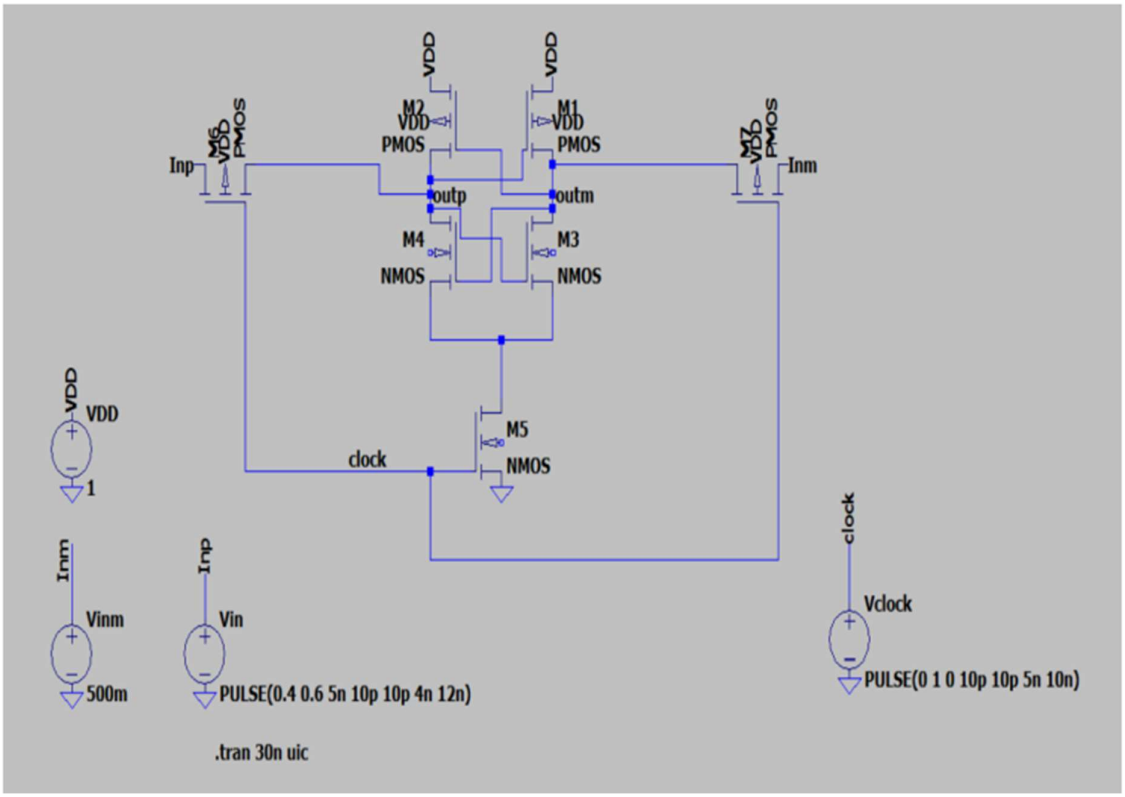
TOPIC : CLOCKED SENSE AMPLIFIER

AIM : To design and Simulate 'Clocked Sense Amplifier'

SOFTWARE : LTSpice

CIRCUIT DIAGRAM :



THEORY :

A Clocked Sense Amplifier (CSA) is a special circuit which is designed to detect small voltage differences between two inputs and amplify them to a full logic level. The use of a clock in its operation allows the amplifier to switch between different states in a controlled manner, ensuring high speed and also power efficiency. This approach enhances noise immunity by rejecting common-mode noise, ensuring reliable operation even in the noisy environments.

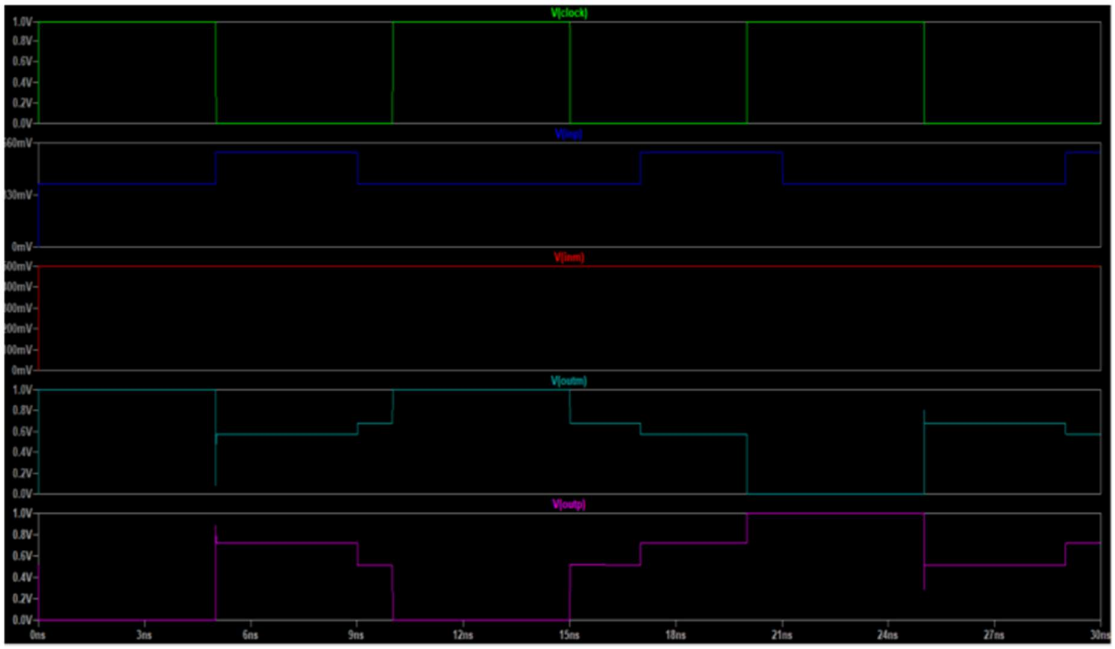
The clocked nature of the CSA allows it to operate efficiently in high-speed applications, consuming power only during the active phase. This makes it a best choice for modern memory technologies such as SRAM, where it is used to read stored data by amplifying the slight voltage variations between the bit lines connected to the memory cells.

Similarly, in DRAM, the CSA plays a vital role in amplifying the small charge differences that represent data stored in capacitors. Beyond memory, clocked sense amplifiers are integral to analog-to-digital converters (ADCs) and high-speed communication systems, where their speed and sensitivity are crucial for accurate signal processing and data recovery.

PROCEDURE :

1. Open a new schematic in ltspice.
2. We need 4 PMOS and 3 NMOS and place them as shown in the circuit diagram above.M1 and M2 are connected in cross conjugated configuration and M3 and M4 also.
3. M5 acts as switch controlled by clock.
4. Then select 4 voltage sources from components and give them values as shown above.
5. Place the ground to all 4 voltage sources and label them as VDD, Inp, Inm and Vclock.
6. Give dc values to VDD and Inm where as pulsating voltage to Vclock and Inp.
7. Connect the MOS with the help of wire as shown in the circuit.
8. Set the length and width of all PMOS as 50n and 1u respectively.
9. Set the length and width of all NMOS as 50n and 500n respectively.
10. In the transient analysis, set the stop time around 30n and skip the initial operation solution.
11. Run the circuit and observe the graphs.

OBSERVATION :



1. The clock signal appears as a square periodic wave alternating between high and low states controlling the operation of amplifier. It is active during high state and circuit resets when its low.
2. The input signal is a square pulse with reduced voltage swing.
3. The two outputs signals were seen which exhibit a differential nature with one signal increasing while other decreasing during active phase of clock.
4. When Inp>Inm, Outp is closer to Vdd and when Inp<Inm, Outm is closer to Vdd.

RESULT / CONCLUSION :

The clocked sensed amplifier was successfully designed and simulated using MOS transistors. This design utilizes clock signal to control its operation which is proved from the graphs. The main use of this circuit is in memory systems like SRAM and DRAM because it is essential for fast and power efficient memory readouts in static and dynamic RAM. Since its clock based operation, it can also be used in flip flops and latches.