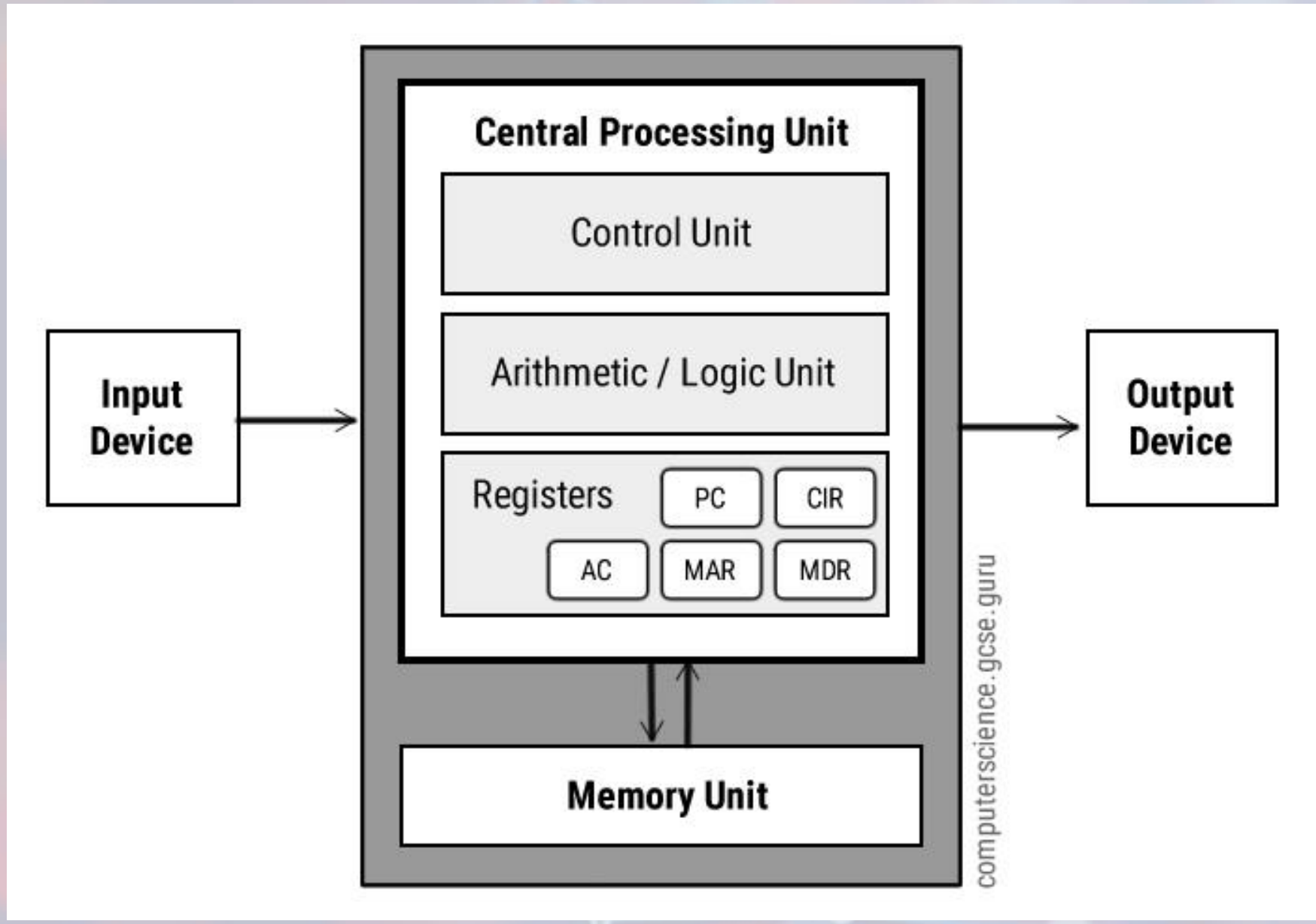
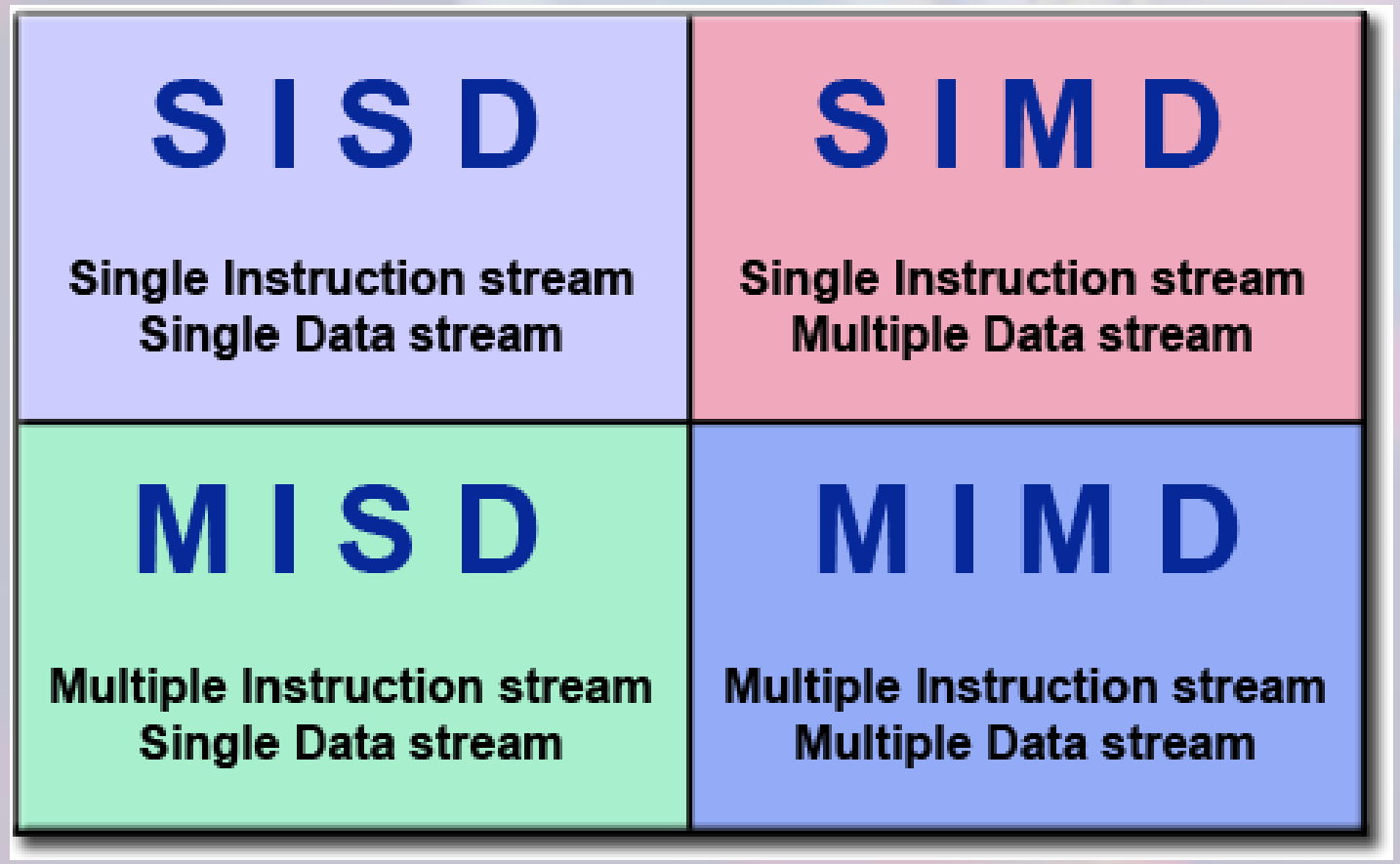
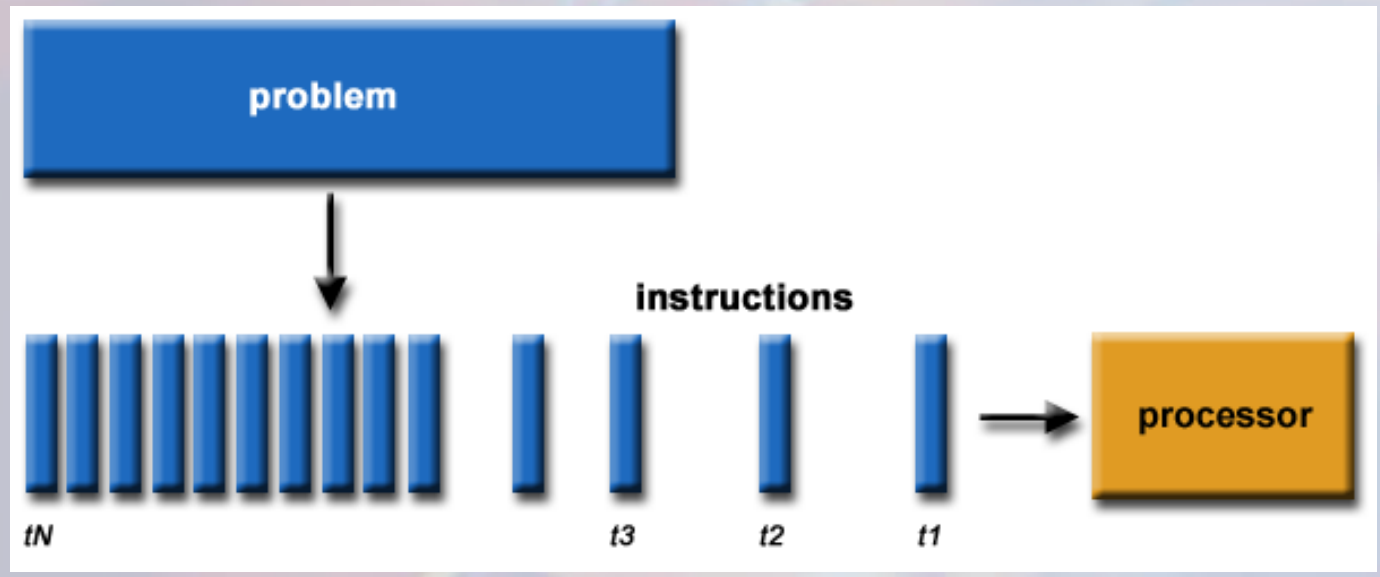
تئوری پردازش موازی

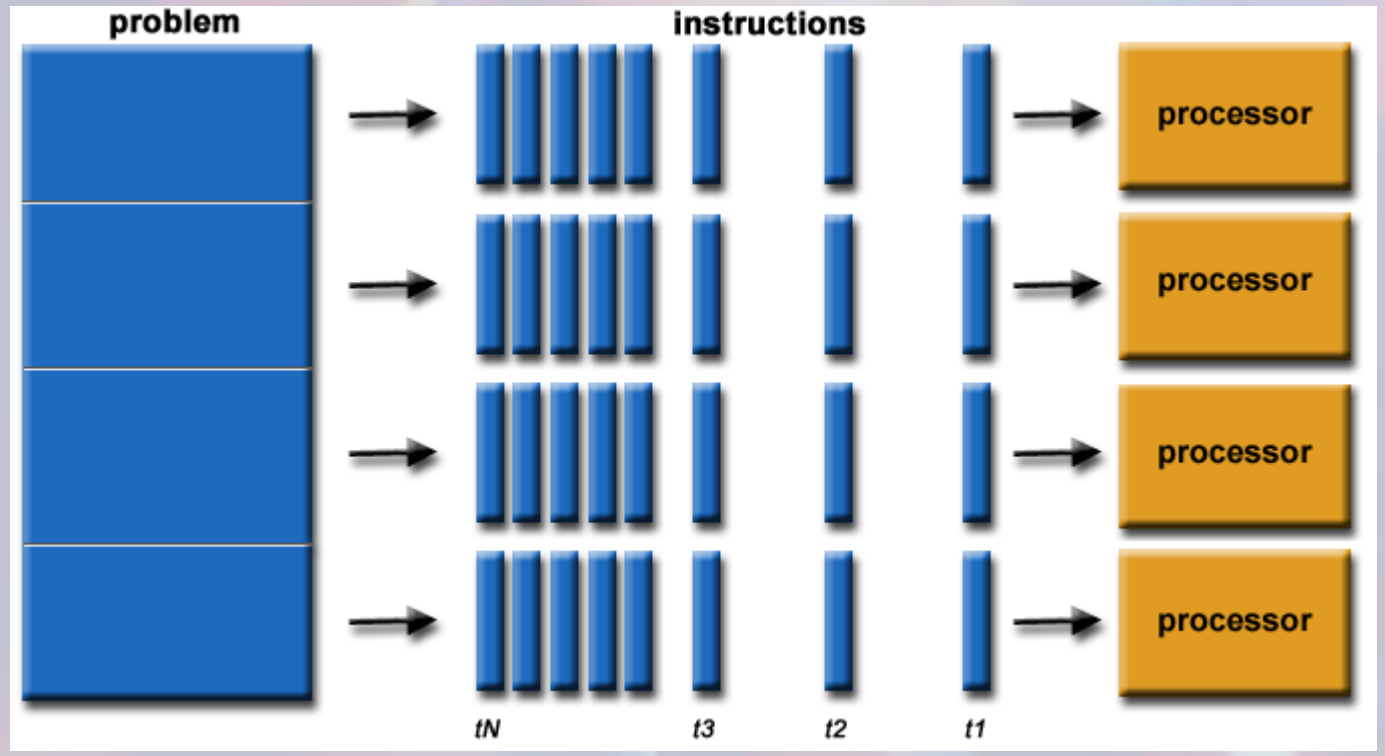
علیرضا وفائی صدر
پژوهشگاه دانش‌های بنیادی (IPM)

بهار ۹۷


Central Processing Unit
Control Unit
Arithmetic / Logic Unit
Registers
PC
CIR
AC
MAR
MDR
Input Device
Output Device
Memory Unit
computerscience.gcse.guru


S I S D
Single Instruction stream
Single Data stream
S I M D
Single Instruction stream
Multiple Data stream
M I S D
Multiple Instruction stream
Single Data stream
M I M D
Multiple Instruction stream
Multiple Data stream


problem
instructions
processor
tN
t3
t2
t1


problem
instructions
processor
processor
processor
processor
tN
t3
t2
t1

Data Hazards

- RAW Hazard

  ADD.D F3, F1, F2

  SUB.D F5, F6, F3 No Solution, normal property of programs

- WAW Hazard

  DIV.D F3, F1, F2

  SUB.D F3, F6, F5 This instruction will complete first Div writes wrong value later, hence stalls may be need for proper operation

- WAR Hazard

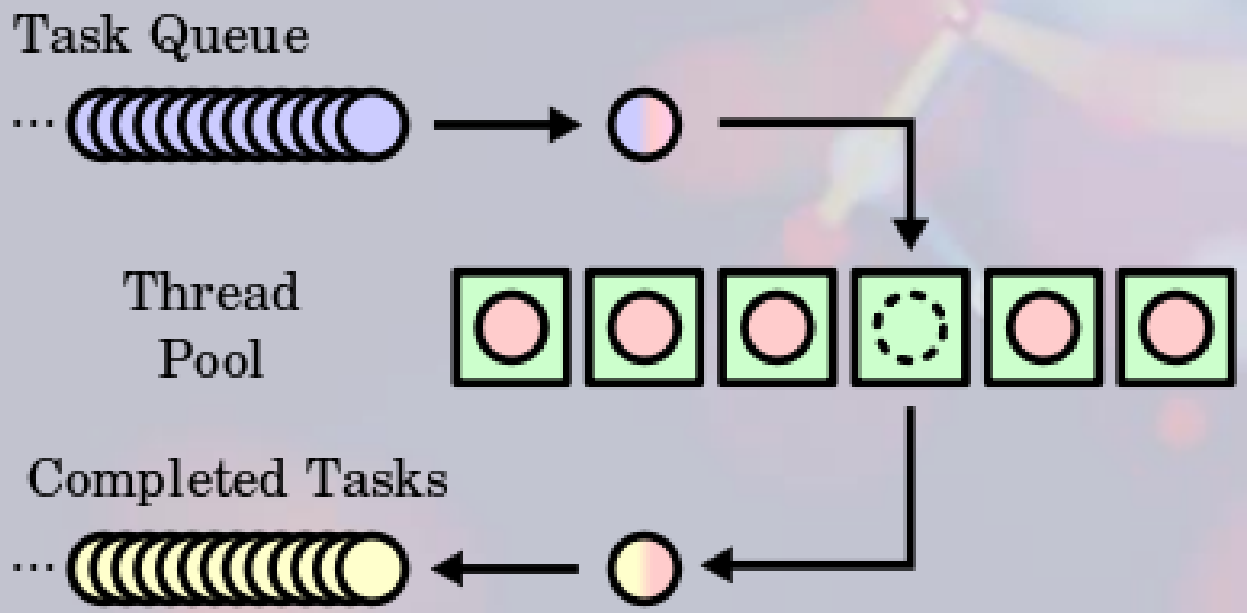
  DIV.D F3, F1, F2
  SUB.D F5, F6, F3
  ADD.D F3, F6, F7

  OR

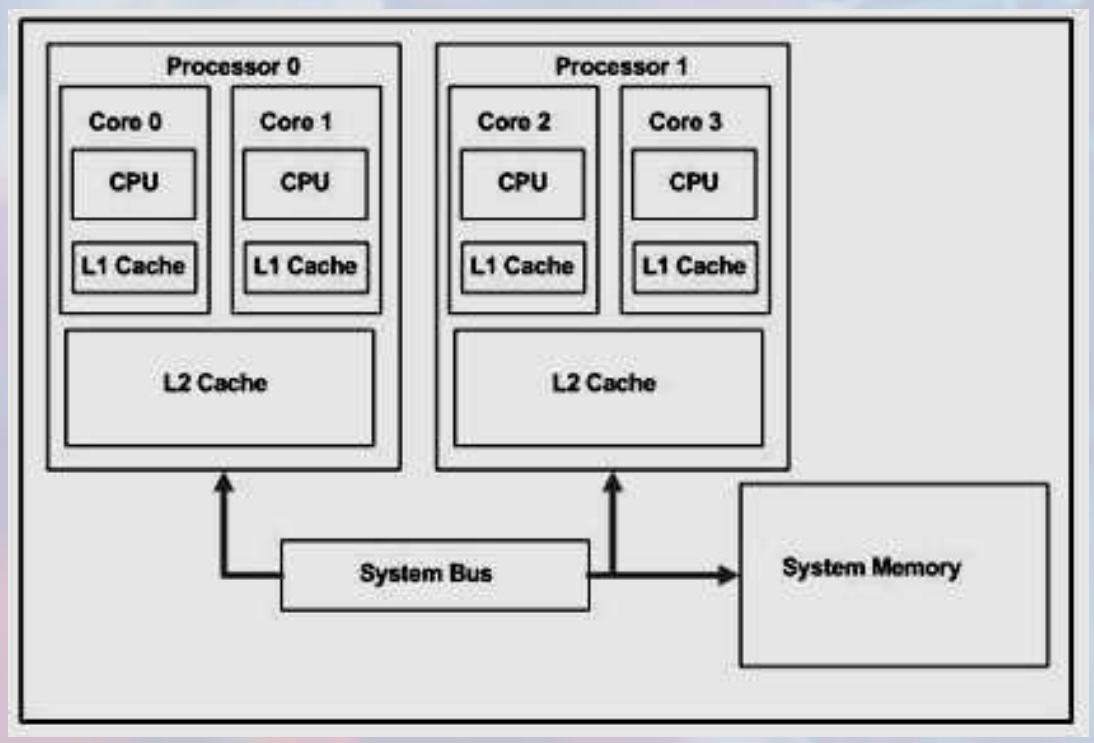
  DIV.D F3, F1, F2
  SUB.D F5, F6, F3
  ADD.D F6, F6, F7

  SUB.D reads wrong value of a register hence stalls may be need in some architectures not in FP pipeline on the next page.

instruction level parallelism

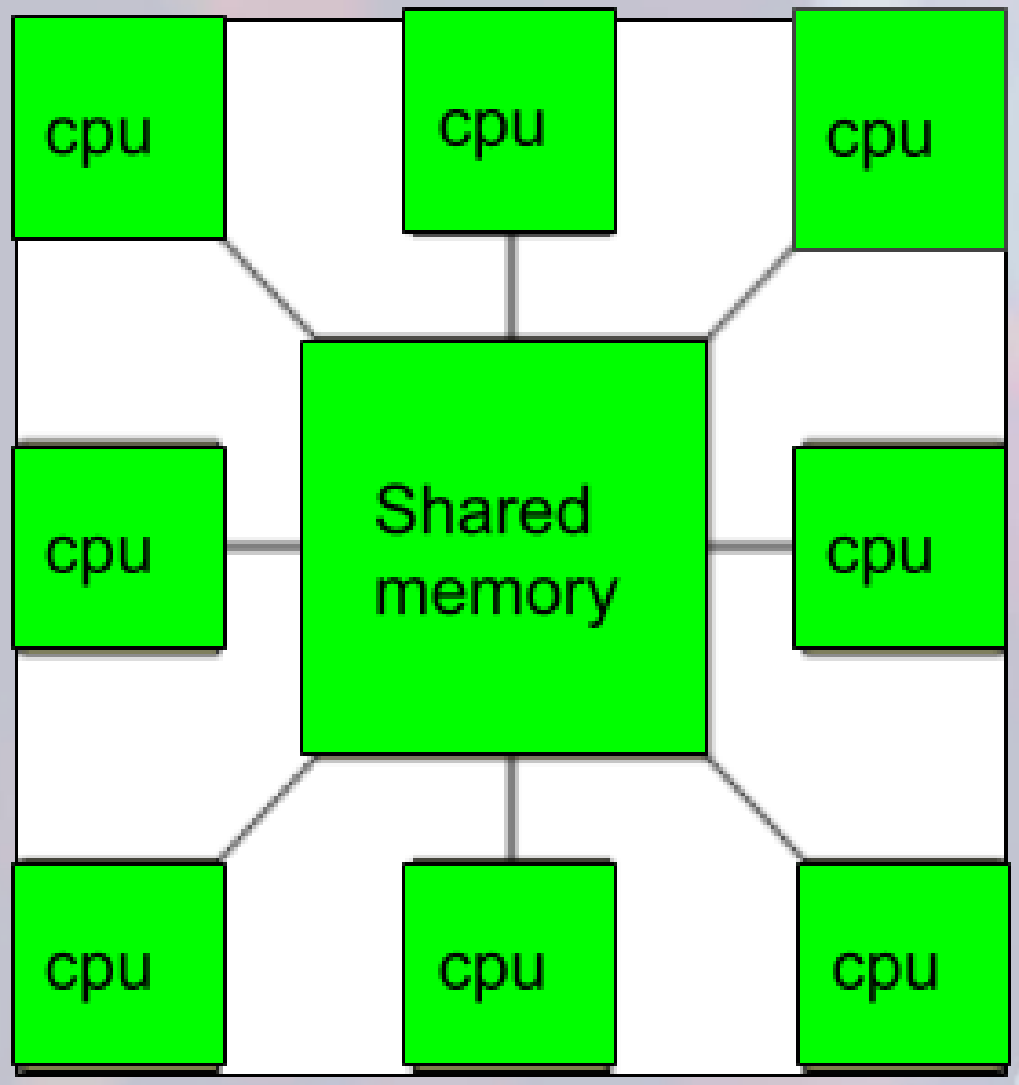


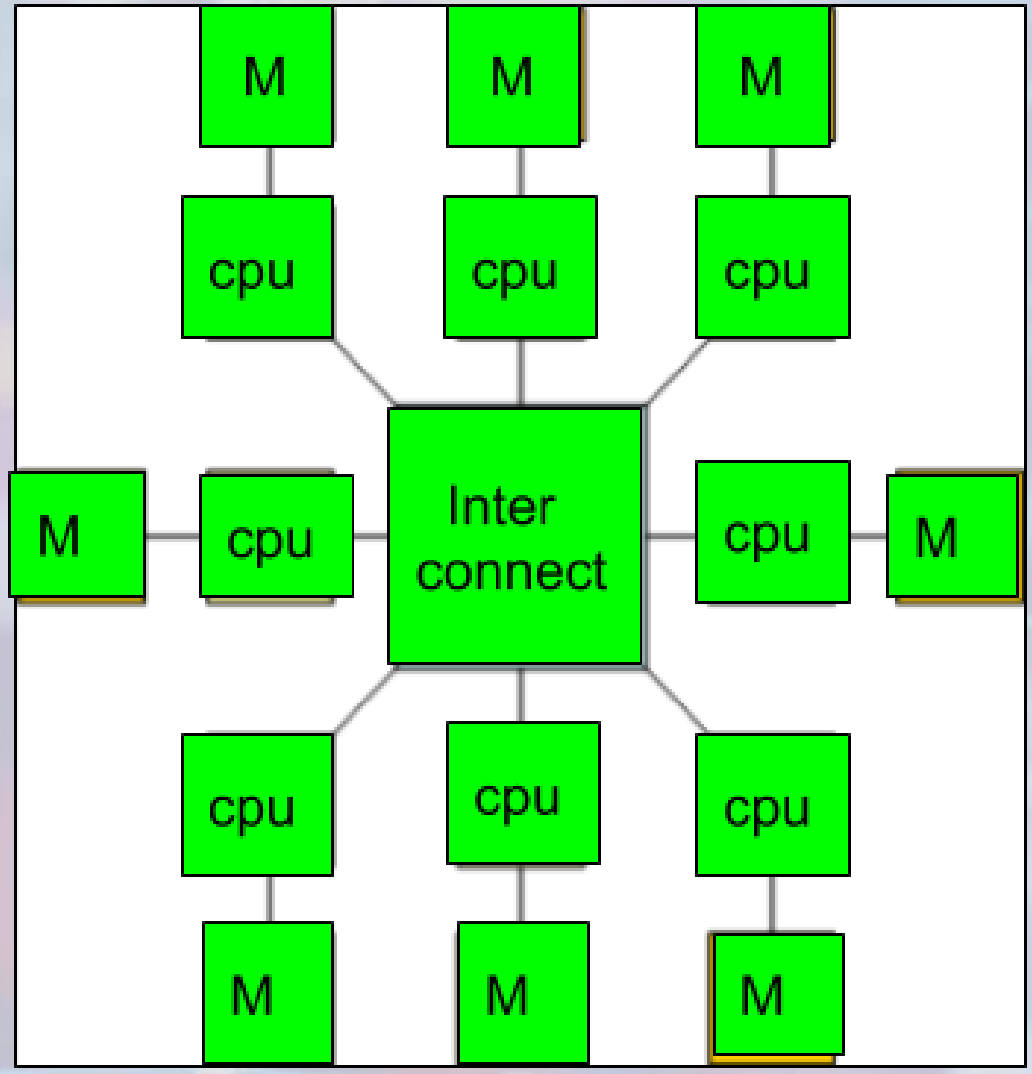
task level parallelism

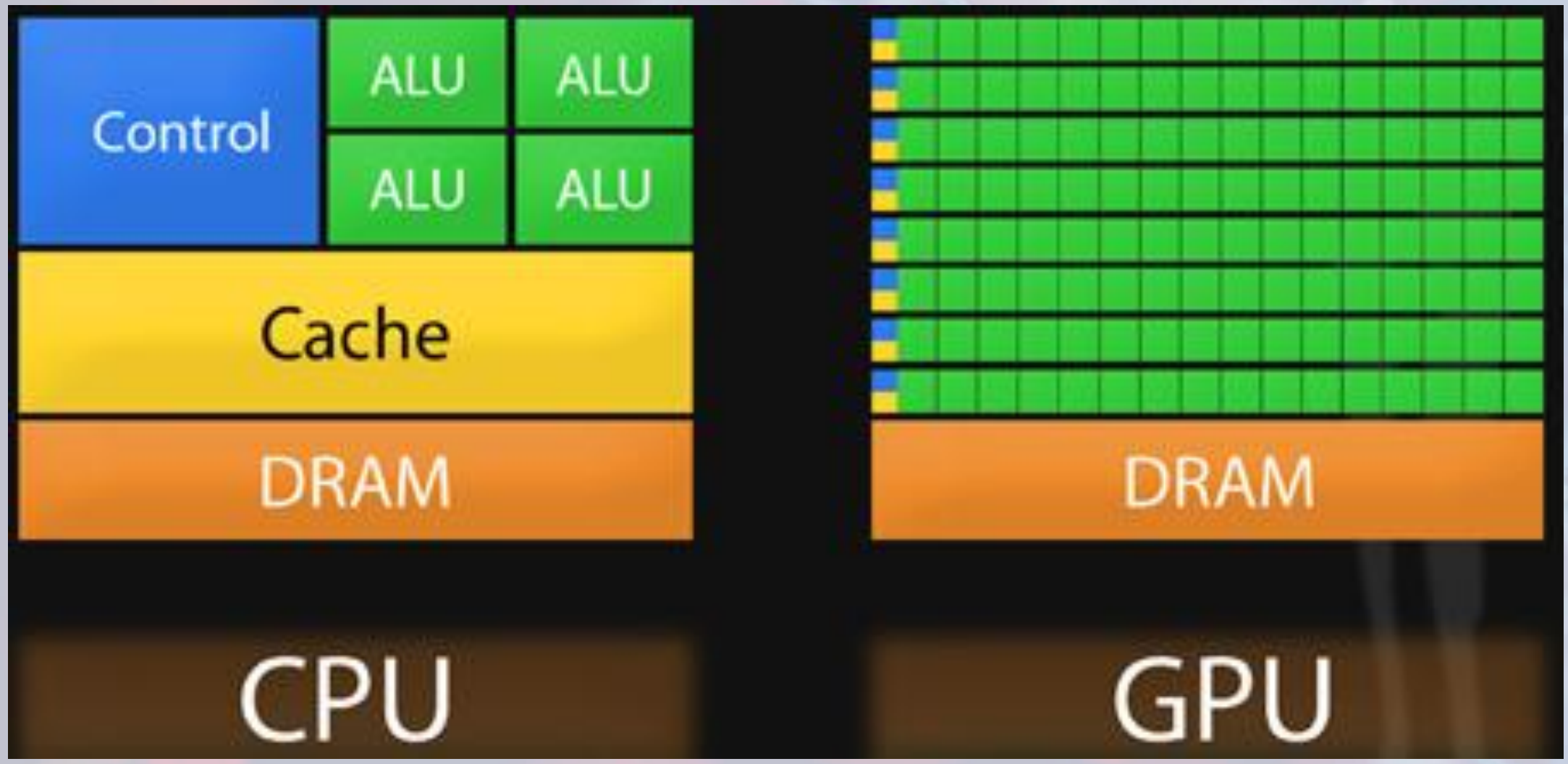


processor level parallelism

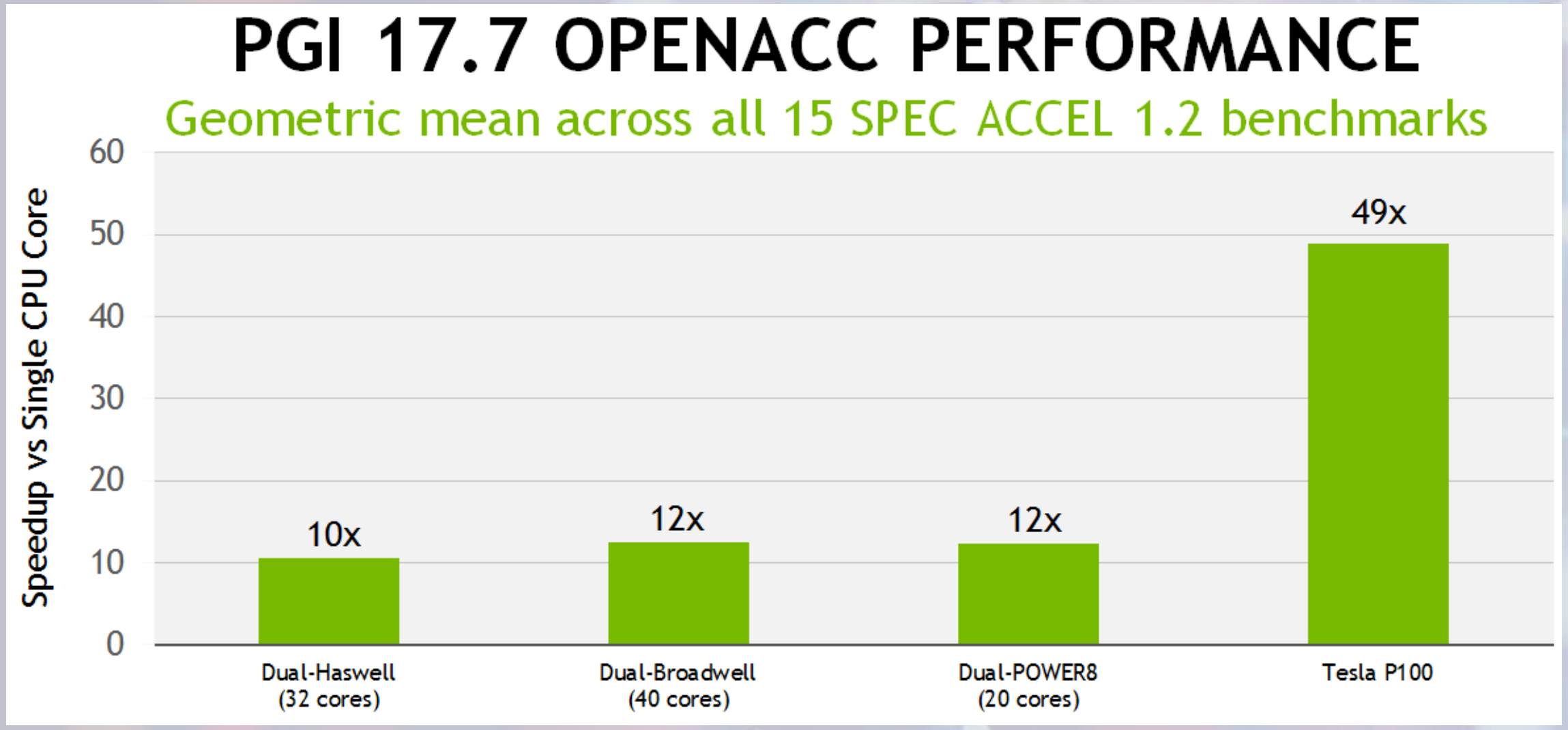
multiprocessor vs. multicomputer






Control
ALU
ALU
ALU
ALU
Cache
DRAM
CPU
DRAM
GPU

CPU vs GPU


PGI 17.7 OPENACC PERFORMANCE
Geometric mean across all 15 SPEC ACCEL 1.2 benchmarks
Speedup vs Single CPU Core
60
50
40
30
20
10
0
10x
12x
12x
49x
Dual-Haswell
(32 cores)
Dual-Broadwell
(40 cores)
Dual-POWER8
(20 cores)
Tesla P100

سپاس