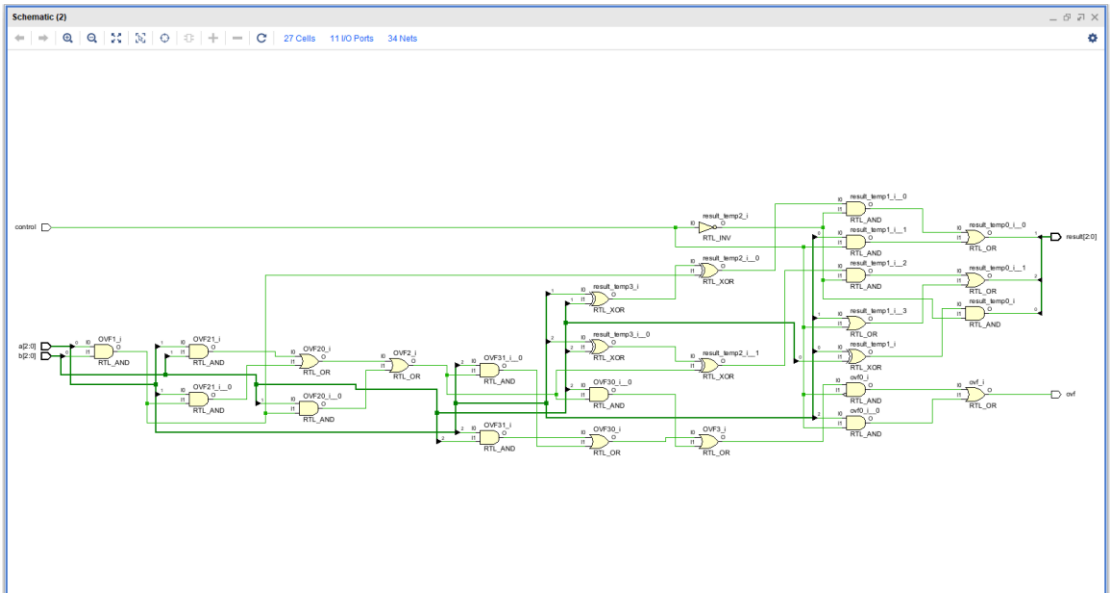
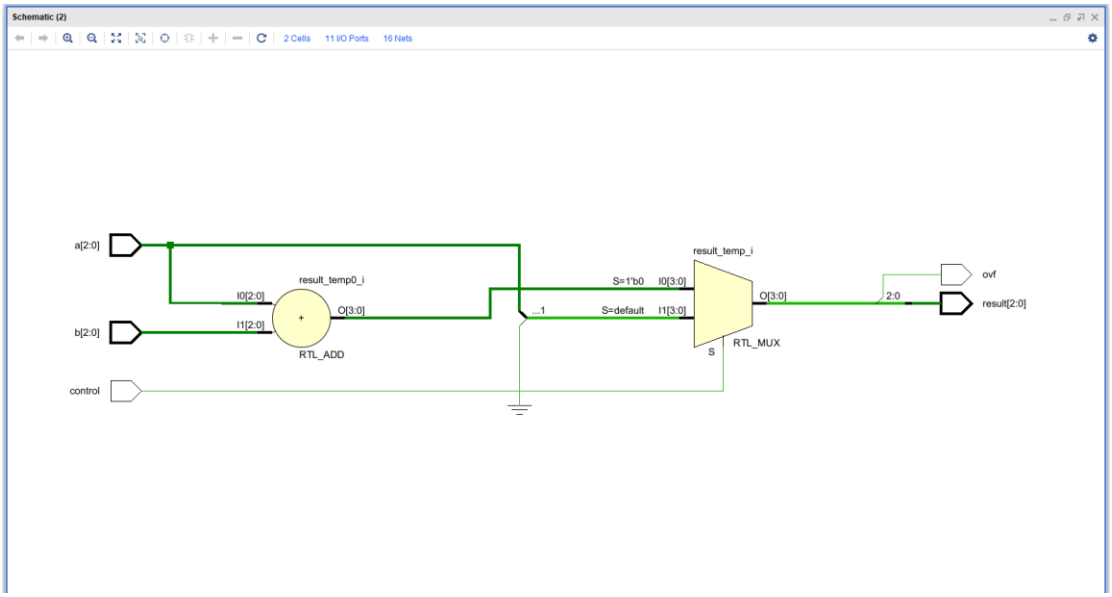
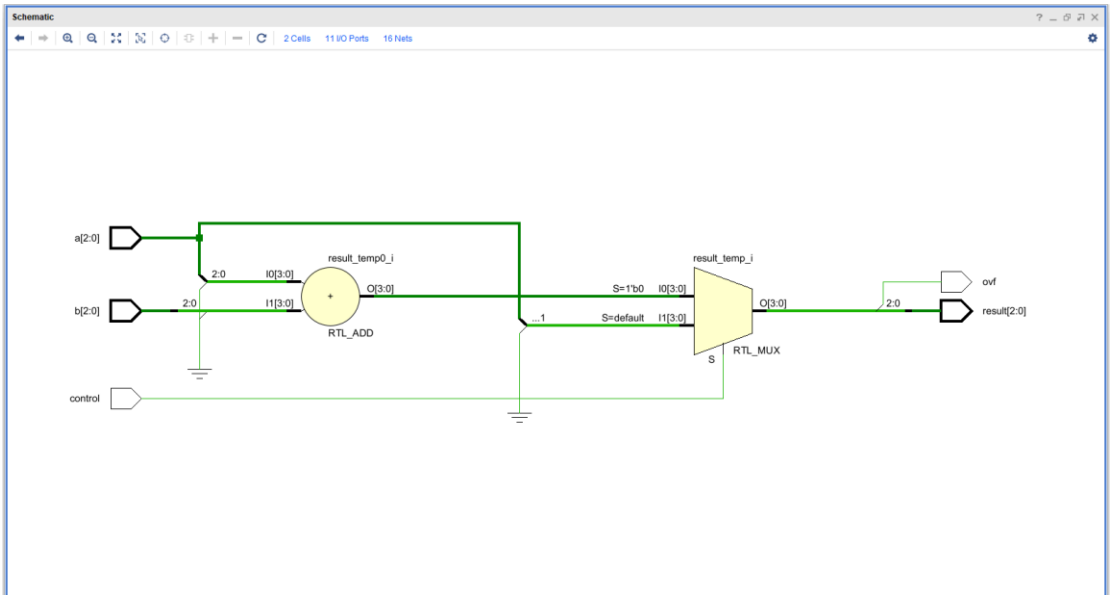


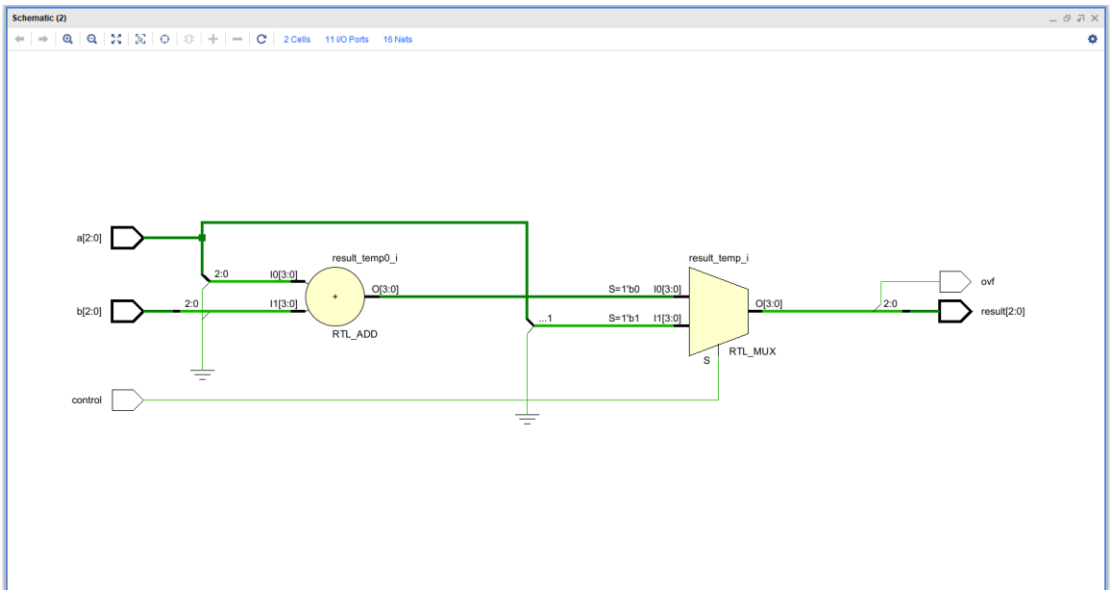
Εικόνα 1:RTL analysis schematic a



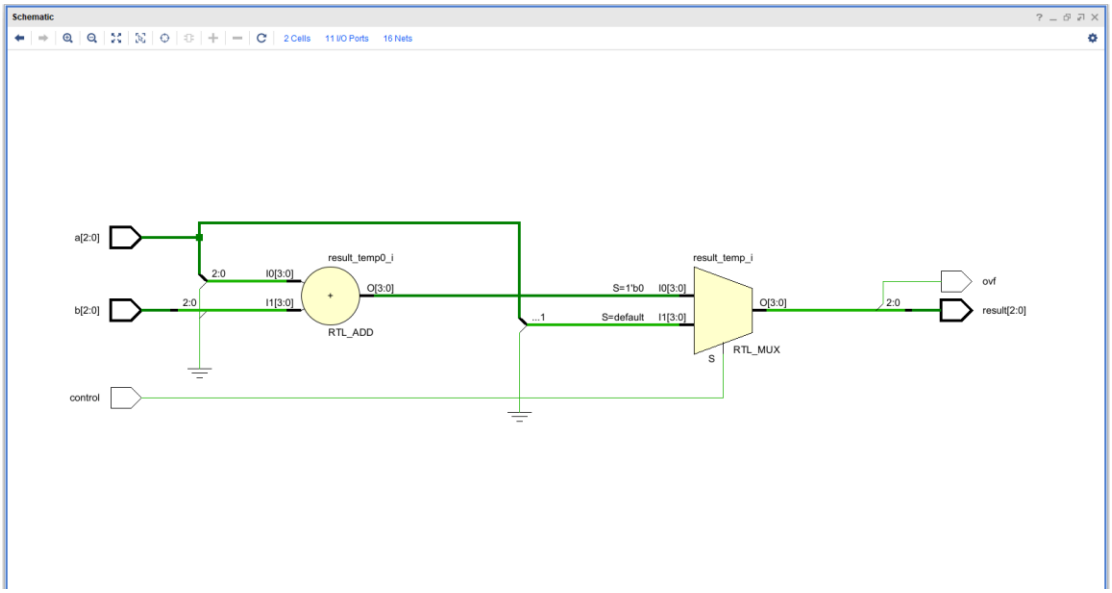
Εικόνα 2:RTL analysis schematic b



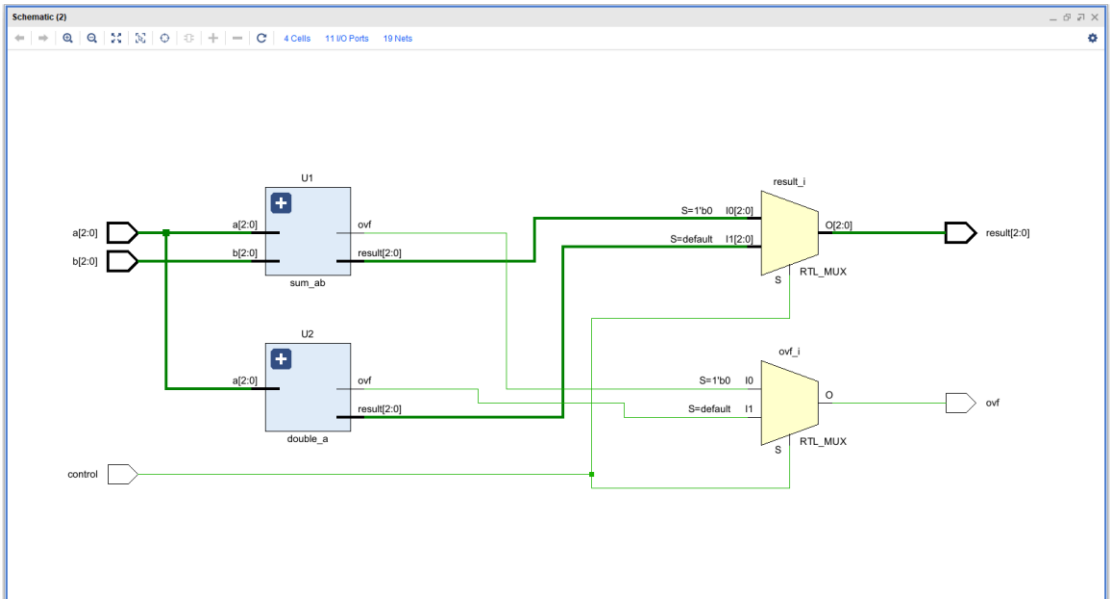
Εικόνα 3:RTL analysis schematic c



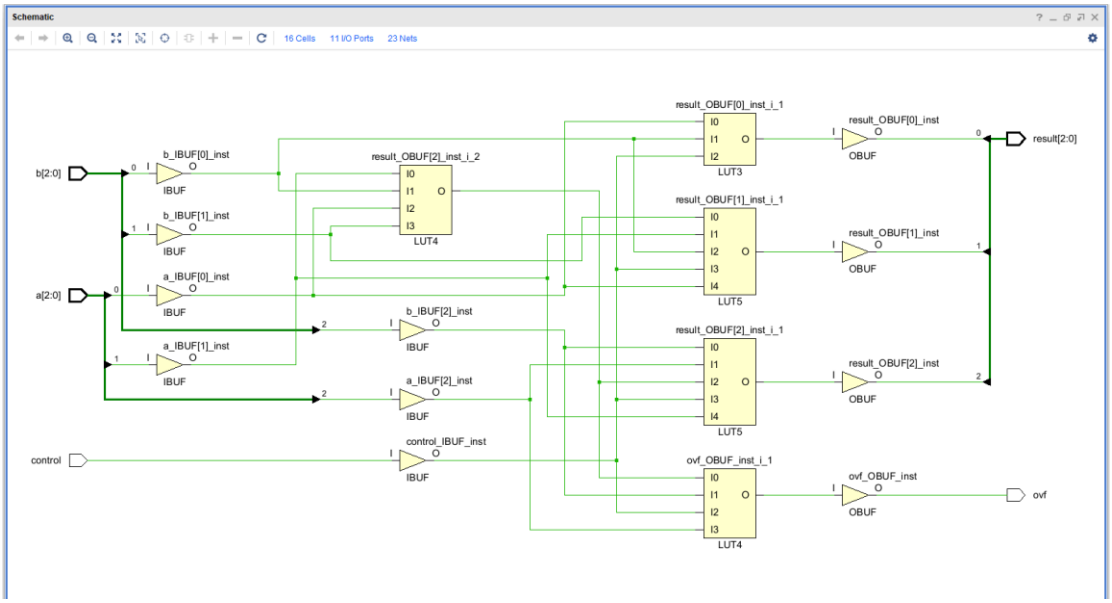
Εικόνα 4:RTL analysis schematic d



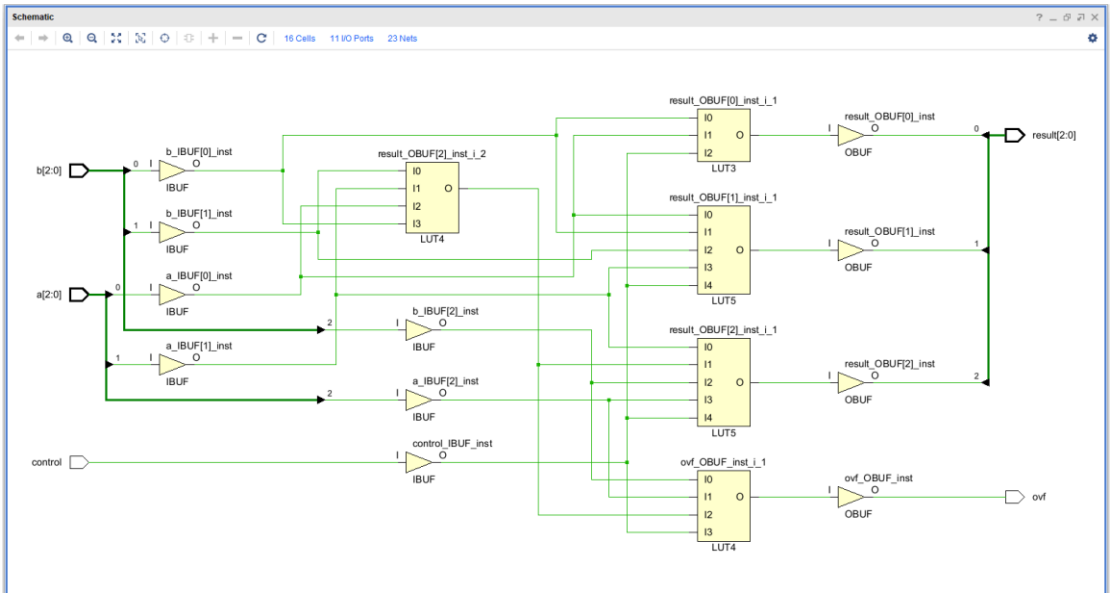
Εικόνα 5:RTL analysis schematic e



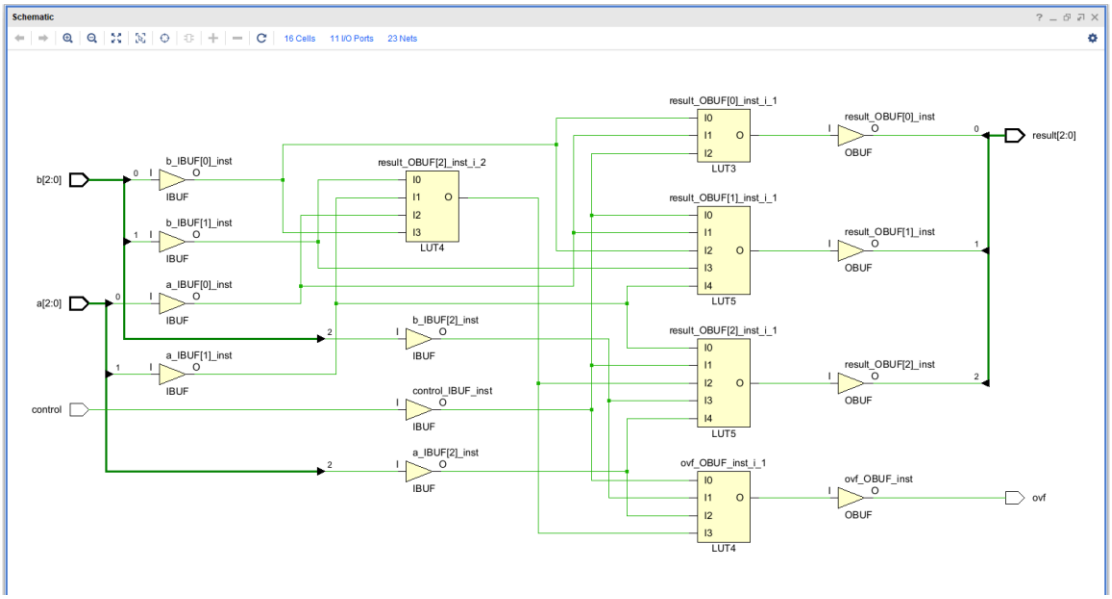
Εικόνα 6:RTL analysis schematic f



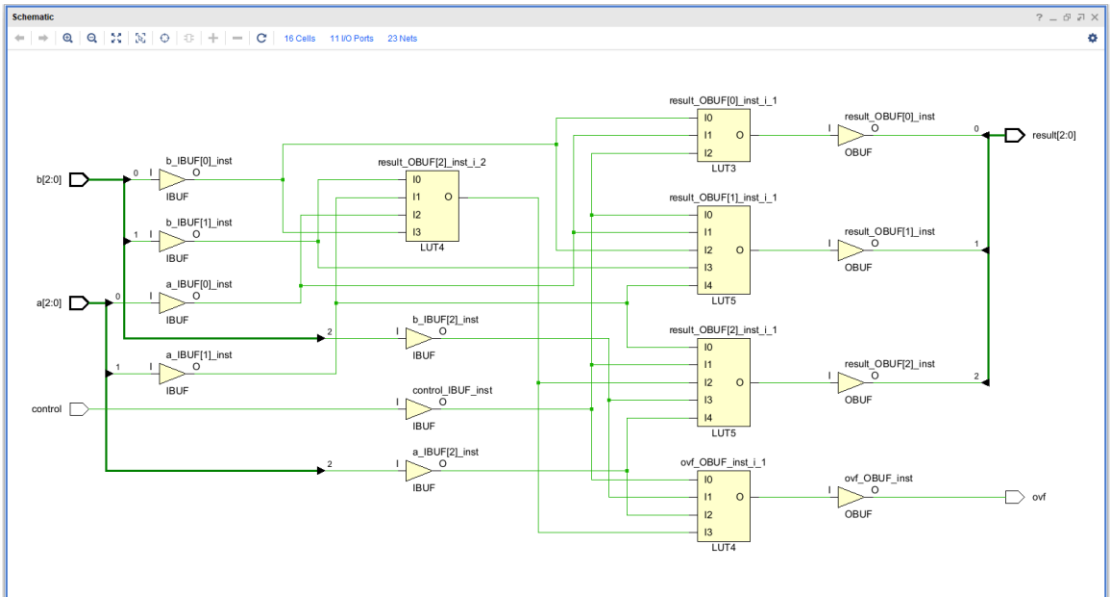
Εικόνα 7:Post-synthesis schematic a



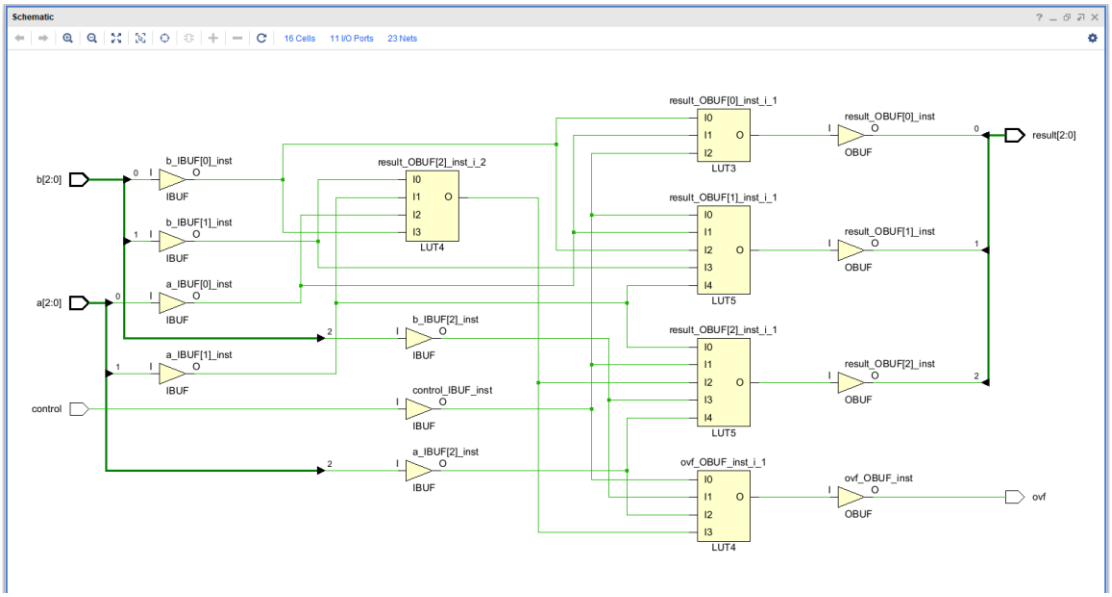
Εικόνα 8:Post-synthesis schematic b



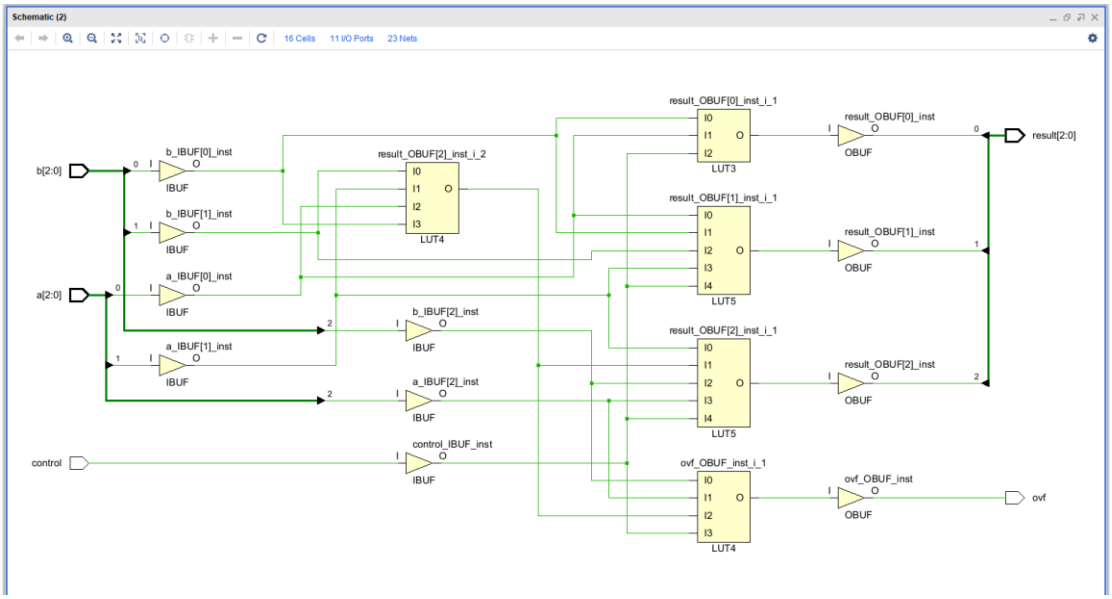
Εικόνα 9:Post-synthesis schematic c



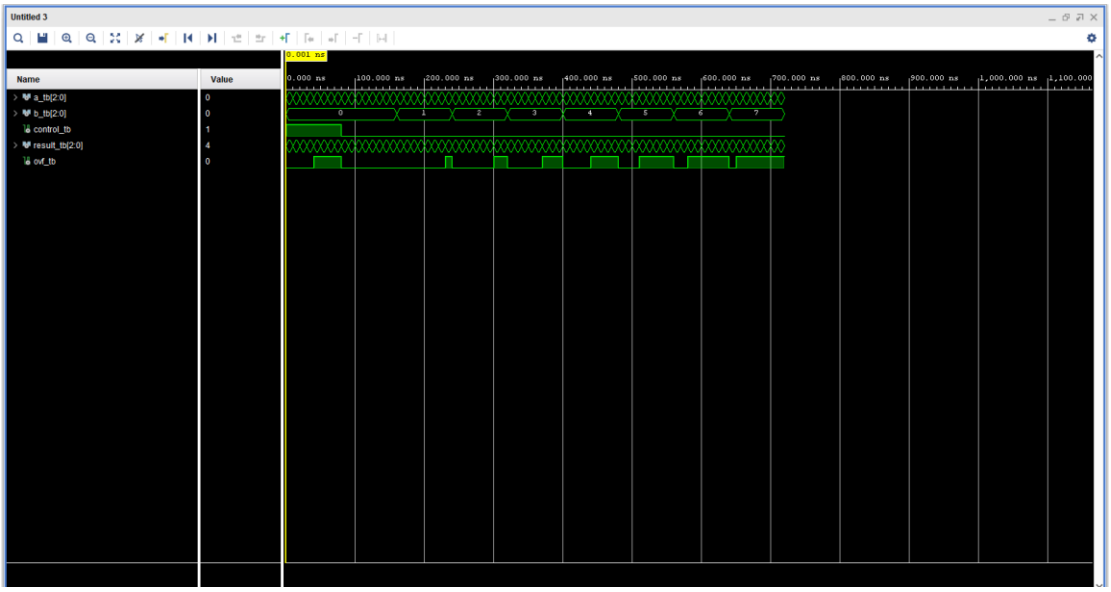
Εικόνα 10:Post-synthesis schematic d



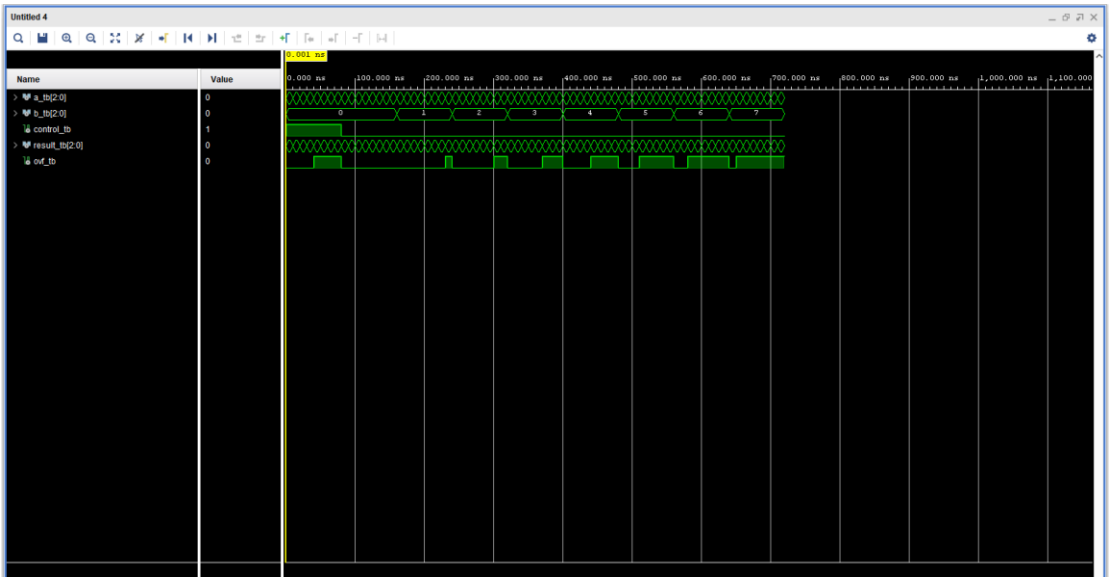
Εικόνα 11:Post-synthesis schematic e



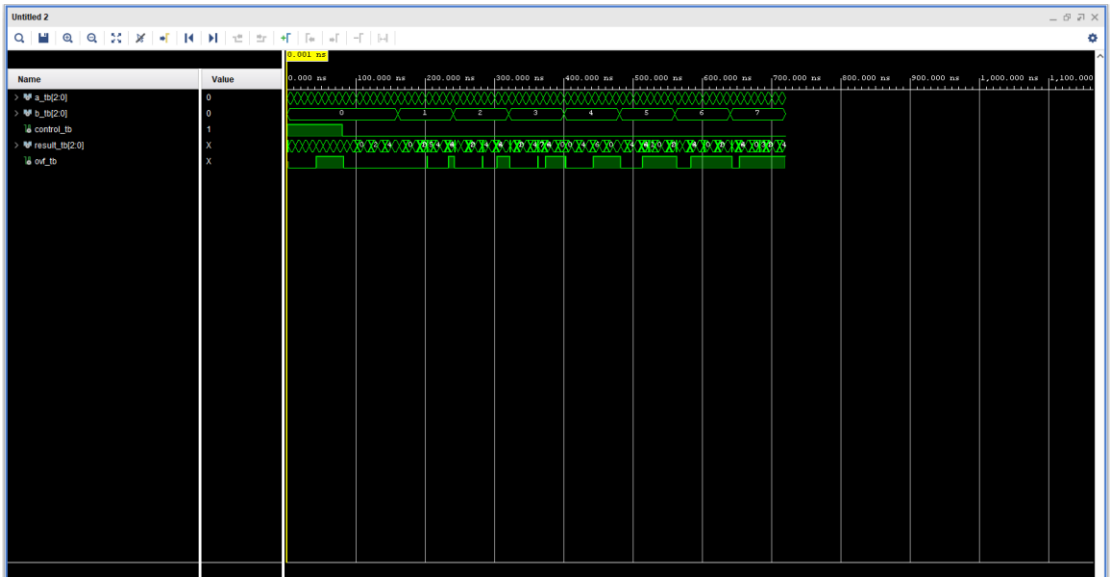
Εικόνα 12:Post-synthesis schematic f



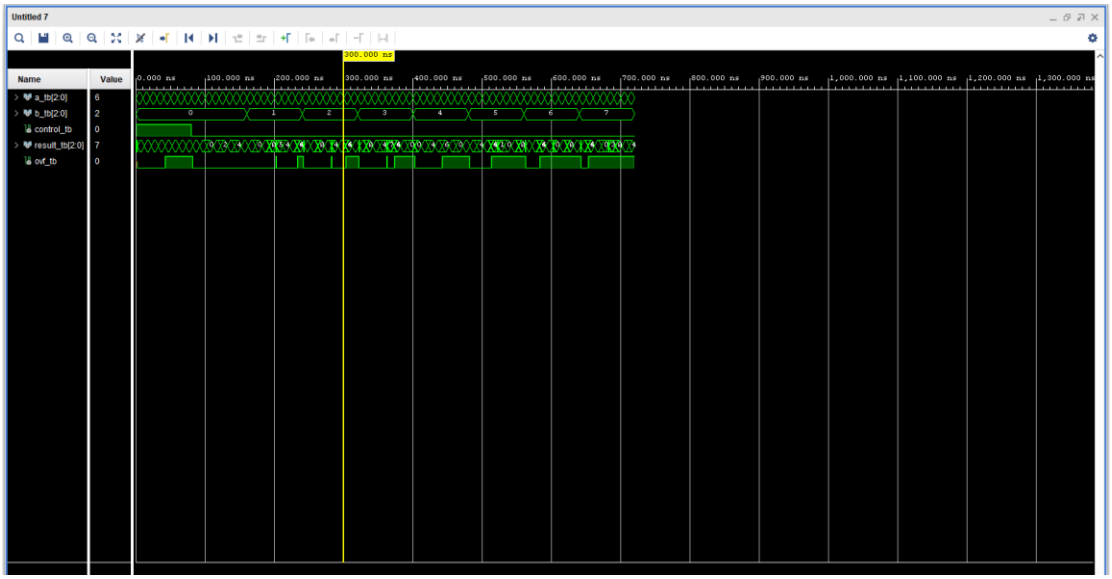
Εικόνα 13:Behavioral simulation για a,b,c,d,e,f



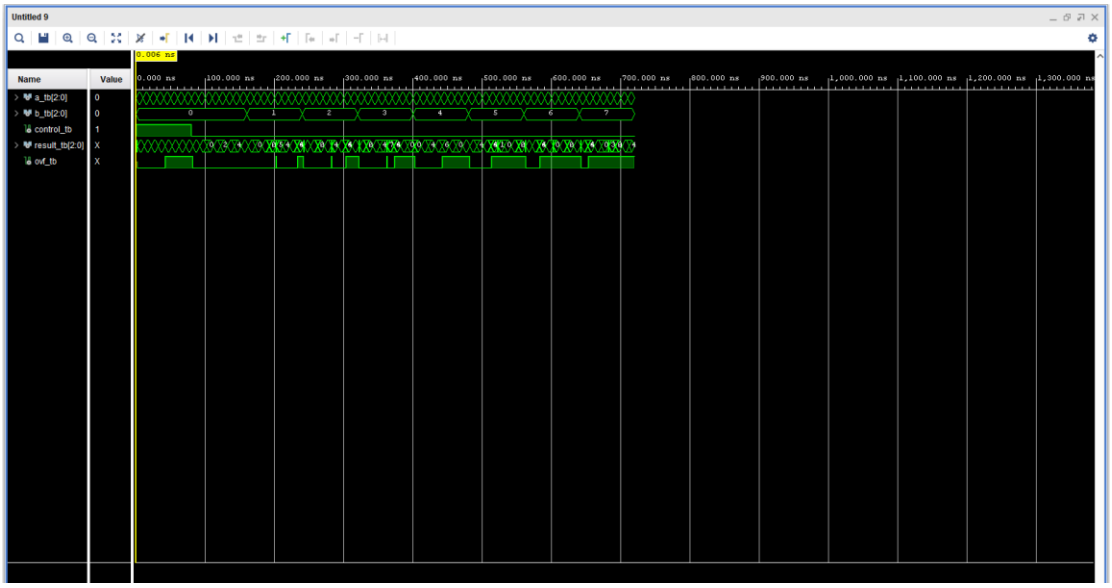
Εικόνα 14:Post-synthesis time simulation a



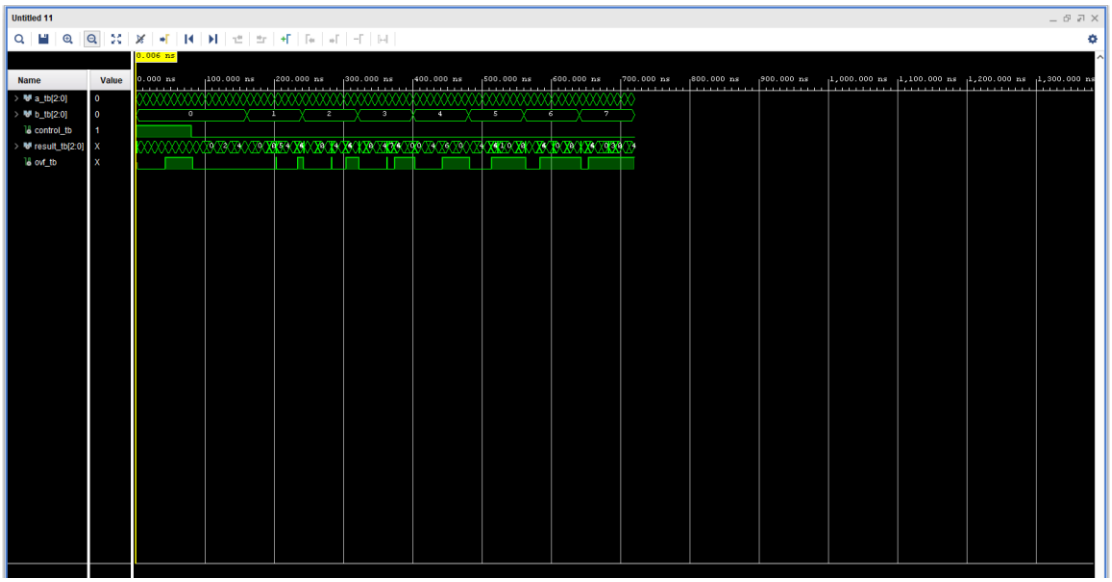
Εικόνα 15:Post-synthesis time simulation b



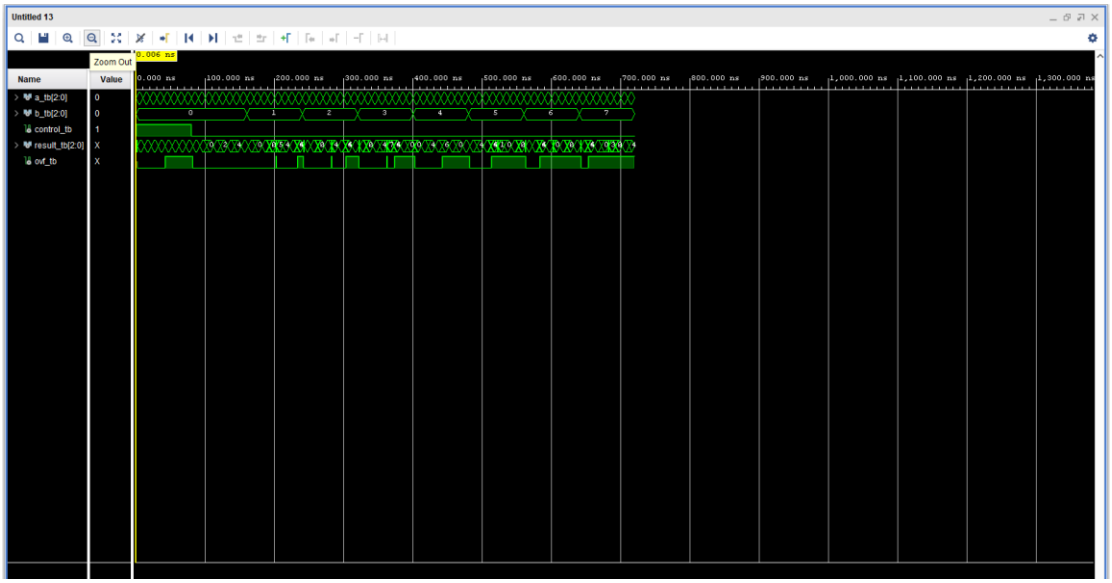
Εικόνα 16:Post-synthesis time simulation c



Εικόνα 17:Post-synthesis time simulation d



Εικόνα 18:Post-synthesis time simulation e



Εικόνα 19:Post-synthesis time simulation f