TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Computer Science Institute for Computer Engineering, Chair for VLSI-Design, Test and Architecture

Dresden, July 3, 2014

Summerschool

Modeling and Designing Dependable Embedded Systems

— Lab 5 —

All tasks are to be implemented in synthesizable VHDL code. The Quartus II synthesis tool is to be used to generate a configuration for the Altera DE0 Educational Board. All solutions must be demonstrated functional on this hardware.

Quartus II

User Interface

Project Navigator

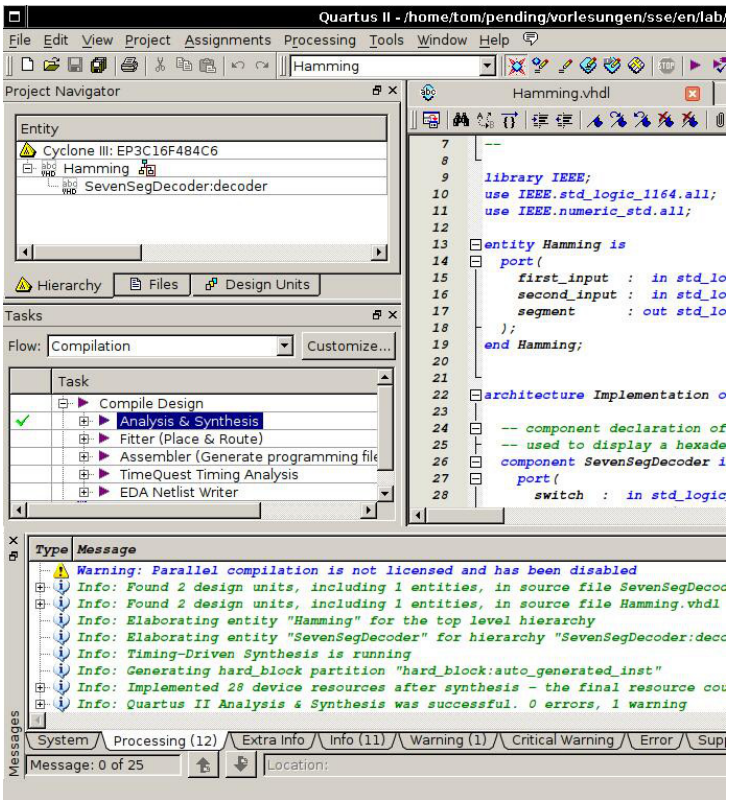
- design structure
- file selection

Task Window

- start synthesis
- progress display

Message Log

- process outputs



Editor / Report Window

Problem 1

(a) Implement a combinational circuit that recodes a 4-bit binary number into a 7-segment code.

(b) Synthesize this design for the DE0 board. Make sure to associate the ports of the top-level module with the appropriate I/O pins of slide switches and a digit of the 7-segment display.

(c) Demonstrate the correct operation of your design on the board.

Problem 2 Implement a sequential design that contains:

- a counter to derive a strobe signal that is asserted for one clock cycle once within a second assuming a clock frequency of 50 MHz, and
- a shift register, in which a single '1' rotates by one bit position on every strobe.

Demonstrate the correct operation of your design using the LED row of the DE0 board.

Problem 3 The push buttons of the prototyping board are not debounced. The bounce length is up to 3 ms. Implement an automaton that utilizes a timing counter to mask all bouncing state transitions until the button has reached a stable state again.

(a) Use this debouncing circuit to switch a LED safely between *on* and *off* with a state transition for each press of the button.

(b) Add a counter to your design that counts the button push events and output the counter value to the 7-segment display.