YUANLONG XIAO

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EDUCATION

Ph.D of Electrical and System Engineering, University of Pennsylvania, PA 2017.09-Expected 2022.05
• Accelerating FPGA incremental development (C to bitstreams) by partial reconfiguration, NoC overlay, high level-synthesis, RISC-V, and open source CAD tool. Advised by Prof. André DeHon.
• The Dean's Fellowship, The Ganster Engineering Fellowship.

Master of Microelectronics, Fundan University, Shanghai, P. R. China 2014.09 - 2017.06
• FPGA chip architecture design, silicon layout design, transistor size optimization automation.
• Published one journal paper and one conference paper.

Bachelor of Microelectronics, Sun Yat-sen University, Guangzhou, P. R. China 2010.09 - 2014.06
• Embedded system application design by CMU, ARM, CPLD or FPGA.
• 2014 Outstanding Graduate of Sun Yat-sen University(top 5%), National Scholarship (twice, top 2%).

SKILLS

• Knowledge: FPGA design from chip architecture, physical layout to Applications, Digital IC Design, System-on-Chip Architecture design, Digital Signal Processing, Semiconductor Theory, Machine Learning
• Specializations in FPGA Partial Reconfiguration (PR), Accelerate FPGA CAD Compile Time by PR Overlay, FPGA Silicon Layout Design
• Programming: Verilog, Python, C++, Matlab, tcl, RISC-V ISA, HTML
• Frameworks: Linux-Ubuntu, Peta Linux for Xilinx FPGA, SDSoC platform for Xilinx SoC
• Hardware Platform and Tools: familiar with Oscilloscope, Logic Analyzer ZCU102, Ultra96 Board, DE-2 Board
• Operating System: Linux-Ubuntu, Mac OS, Windows

PROJECTS

Accelerating FPGA Debugging by RISC-V Overlay Independent Developer 2020.08-present
• Use NoC to connect 8-32 partial reconfiguration (PR) blocks.
• Expand RISC-V ISA with streaming interface like Microbaze from Xilinx
• Map PR blocks with RISC-V or Hardware IPs
• Accelerating FPGA debugging

Symbiflow Partial Reconfiguration Expansion Main Developer 2020.05-present
• Expand the Symbiflow (Google) with Partial Reconfiguration Features.
• Defined Routing Graph Resources.
• Defined Partitions Pins for new P-blocks

Dataflow Incremental Refinement for C Group Leader 2020.01-2020.09
• Created a NoC overlay on top of a Zynq chip (FPGA fabric+quad ARM Cortex-A53
• Decomposed C/C++ applications to separate latency-insensitive operators, connected by stream interfaces.
• Virtualized Zynq on-chip memory as ring buffer.
• Mapped C/C++ operators to ARM within 10 seconds or to FPGA fabric within 20 minutes.

Reducing FPGA Compile Time with Separate Compilation Group Leader 2017.09-2019.09
• Developed a tool PRflow based on python that calls Vivado HLS, Vivado to generate partial bistreams and a packet-switched network overlay
Compile separate compile jobs on the cloud by Sun Grid Engine (qsub)
• Reduced compilation times reduce from 42 minutes to 12 minutes.
• Using Symbiflow (Project X-Ray/Yosys/VPR),reduce most compile times under 5 minutes.

Layout Implementation of FPGA Modules Independent Developer 2014.09-2015.02

• Designed a transistor-level register which can be configured as a latch or an edge-triggered flip-flop.
• Designed a 16-to-1interconnect multiplexer, adjusted the width to support proper drive strength.
• Increased the operating rate from 200MHz to 500MHz, decreased the area from 60um *70um to 30um*70um in 65nm process.

Built-in Self-test System for Setup/Hold Times of FPGAs Independent Developer 2015.12-2016.02

• Used Verilog HDL to implement the Built-in Self-test (BIST) system in the Virtex-5 FPGA with ISE software.
• Simulated the system with MODELSIM software and debugged the system in ML510 board of Xilinx.
• Measured the setup and hold times of CLB, DSP and BRAM to the accuracy of 13 pico-second without using external testers.

LEADERSHIP & EXTRA-CURRICULAR ACTIVITIES

Teaching Assistant **2010.09 - 2014.06**

• System-on-a-Chip Architecture, ESE532@Upenn: Developed SDSoC platform, bare metal multi-core platforms, Petalinux platform for Ultra96; Led office hours, hold emulation tutorials
• Digital Integrated Circuits AND VLSI Fundamentals, ESE570@Upenn, twice: Hold Cadence virtuoso tutorials,

Volunteer Leader of Chinese Physics Society 2012 Fall Meeting **2010.9**

• Led a team of 30 members to prepare for the meeting hall, maintain the order and provide service to the lecturers and audience.

PUBLICATIONS

• **Yuanlong Xiao**, Dongjoon Park, Andrew Butt, Hans Giesen, ZhaoyangHan, Rui Ding, Nevo Magnezi, Raphael Rubin, and André DeHon. Reducing FPGA compile time with separate compilation for FPGA building blocks. In *2019 International Conference on Field-Programmable Technology (ICFPT)*, pages 153–161. IEEE, 2019.
• Dongjoon Park, **Yuanlong Xiao**, Nevo Magnezi, and André DeHon. Case for fast fpga compilation using partial reconfiguration. In *2018 28th International Conference on Field Programmable Logic and Applications(FPL)*, pages 235–2353. IEEE, 2018.
• **Yuanlong Xiao**, Jian Wang, and Jinmei Lai. A universal automatic on-chip measurement of fpga's internal setup and hold times. *IEICE Electronics Express*, 13(23):20160810–20160810, 2016.
• Jian Wang, Yuanlong Xiao and Jinmei Lai, "A Setup/Hold Times Testing System and Method", Chinese Patent Publication Number: CN105759195A, epub.sipo.gov.cn/index.action.
• Zhengjie Li, **Yuanlong Xiao**, Yufan Zhang, Yunbing Pang, Jian Wang, and Jinmei Lai. Transistor-level optimization methodology for grm fpga interconnect circuits. In *Proceedings of the 2019 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pages 121–121, 2019.
• Zhengjie Li, **Yuanlong Xiao**, Yufan Zhang, Yunbing Pang, Chengyu Hu,Jian Wang, and Jinmei Lai. An automatic transistor-level tool for grm fpga interconnect circuits optimization. In *Proceedings of the 2019 onGreat Lakes Symposium on VLSI*, pages 93–98, 2019.
• **Yuanlong Xiao**, Jian Wang, and Jinmei Lai. A power efficient current-mode differential driver for fpgas. In *2015 IEEE 11th International Conference on ASIC (ASICON)*, pages 1–4. IEEE, 2015.