Silicon Piezoresistive Stress Sensors and Their Application in Electronic Packaging

Jeffrey C. Suhling, *Member, IEEE*, and Richard C. Jaeger, *Fellow, IEEE*

***Abstract*—Structural reliability of integrated circuit (IC) chips in electronic packages continues to be a major concern due to ever-increasing die size, circuit densities, power dissipation, operating temperatures, and the use of a wide range of low-cost packaging materials. A powerful method for experimental evaluation of silicon die stress distributions is the use of test chips incorporating integral piezoresistive sensors. In this paper, a review is made of the state-of-the-art in the area of silicon piezoresistive stress sensor test chips. Developments in sensor theory, calibration methods, and packaging applications are presented. In the absence of die failure, packaging-induced stresses result in changes in the parametric performance of circuitry on the die, and the theory discussed here can be used to predict such changes.**

***Index Terms*—Electronic packaging, piezoresistive, stress sensor, test chip.**

I. Introduction

STRESSES due to thermal and mechanical loadings are often produced in integrated circuit (IC) chips that are incorporated into electronic packages. They typically occur due to nonuniform thermal expansions resulting from mismatches between the coefficients of thermal expansion of the materials comprising the package and the semiconductor die. Additional thermally induced stresses can be produced from heat dissipated by high power density devices during operation. Finally, mechanical loadings can be transmitted to the package through contact with the printed circuit board to which the package is mounted. The combination of all of the above loadings can lead to two-dimensional (2-D) (biaxial) and three-dimensional (3-D) (triaxial) states of stress on the surface of the die. If high power density devices within the package are switched on and off, these stress states can be cyclic in time causing fatigue. All of these factors can lead to premature failure of the package due to such causes as fracture of the die, severing of connections, die bond failure, solder fatigue, and encapsulant cracking. In the absence of die failure, these stresses lead to parametric shifts that affect the performance and tolerances of both analog and digital integrated circuits, and the piezoresistive theory can be used to predict such changes.

Manuscript received September 18, 2000; revised February 15, 2001. This work was supported by the Semiconductor Research Corporation, the Alabama Microelectronics Science and Technology Center, and the Center for Commercial Development of Space Power and Advanced Electronics with funding from NASA, Auburn University, and its industrial partners. The associate editor coordinating the review of this paper and approving it for publication was Dr. Andre Bossche.

J. C. Suhling is with the Department of Mechanical Engineering, Auburn University, AL 36849 USA (e-mail: jsuhling@eng.auburn.edu).

R. C. Jaeger is with the Department of Electrical and Computer Engineering, Auburn University, AL 36849 USA (e-mail: jaeger@eng.auburn.edu).

Publisher Item Identifier S 1530-437X(01)04137-9.

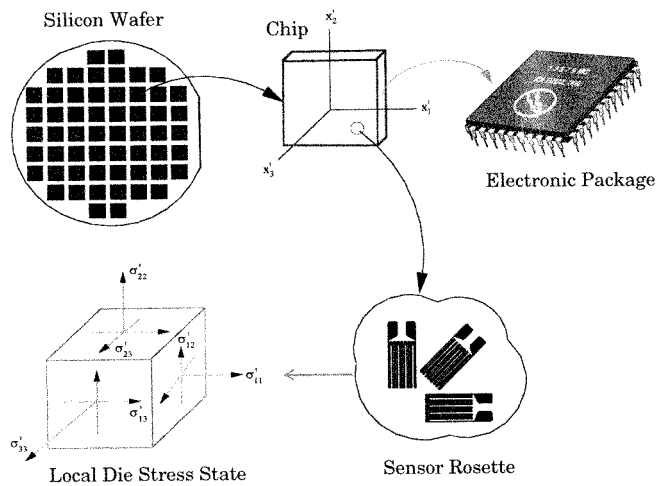

Fig. 1. Piezoresistive stress sensor concept.

The piezoresistive behavior (change of resistivity with stress) of semiconductors such as silicon has been studied extensively for many years [1]–[10]. However, the earliest applications of resistor sensors on IC chips for stress measurement in plastic encapsulated electronic packages were made at Texas Instruments in the early 1980s [11], [12], and numerous applications in electronic packaging have followed [13]–[20]. Many potential applications exist for piezoresistive sensors in the microelectronic packaging industry including qualifying of manufacturing processes, guiding material selection, and evaluating reliability. If the piezoresistive sensors are calibrated over a wide temperature range, thermally induced stresses can be measured [21]. Finally, a full-field mapping of the stress distribution over the surface of a die can be obtained using specially designed test chips, which incorporate an array of sensor rosettes.

In this paper, the state-of-the-art in the area of silicon piezoresistive stress sensor test chips is reviewed. Discussions are made of sensor theory, calibration methods, and packaging applications. Extensions of the theory to changes in MOS device behavior are also outlined and applications presented. Fig. 1 illustrates the basic application concepts. The structures of interest are semiconductor (e.g., silicon) chips that are incorporated into electronic packages. The sensors have most often been resistors, which are conveniently fabricated into the surface of the die using current microelectronic technology, although MOSFETs are now being employed. The sensors are not mounted on the surface in the manner of conventional metallic foil or semiconductor strain gages. Rather, they are an integral part of the structure (chip) to be analyzed by the way of the fabrication process (see Fig. 2). Electrical isolation between the doped surface re-

1530–437X/01$10.00 © 2001 IEEE

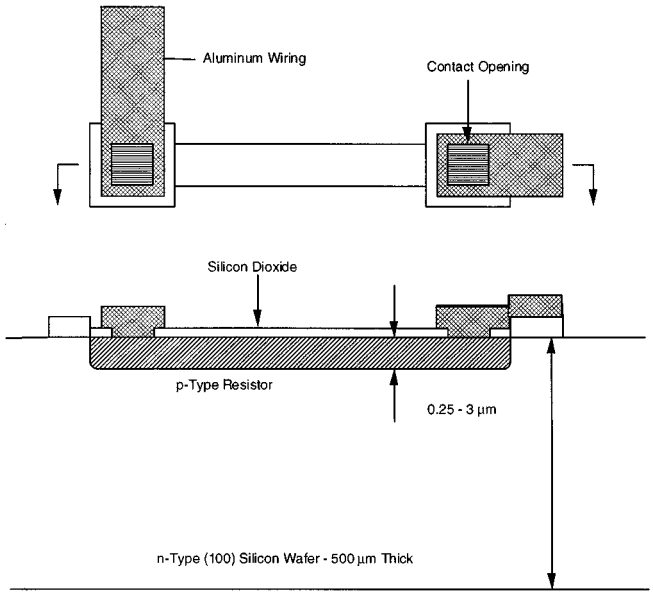

Fig. 2. Top and side views of a piezoresistive sensor.

sistor and the bulk of the chip is maintained using the diode characteristics of the p-n junction and proper reverse biasing of the resistor and substrate regions. The stresses in the chip produce measurable changes in the sensor resistance due to the piezoresistive effect. Therefore, the sensors are capable of providing nonintrusive measurements of surface stress states on a chip even within encapsulated packages where they are embedded sensors. The doped active region of a piezoresistive sensor is typically designed using a serpentine pattern, in order to achieve acceptable resistance levels for measurement (see Fig. 3).

II. Piezoresistivity Theory for Silicon

A. General Resistance Change Equations

Silicon is an anisotropic material (cubic crystal), and the behavior of a unidirectional piezoresistive sensor depends strongly on the wafer plane in which it is fabricated and the orientation of the sensor in that wafer plane. An arbitrarily oriented silicon filamentary conductor is shown in Fig. 4. In this work, the notation developed in [15] is followed. The unprimed axes $x_1 = [100]$, $x_2 = [010]$, and $x_3 = [001]$ are the principal crystallographic directions of the cubic (m3m) silicon crystal, whereas the primed coordinate system is arbitrarily rotated with respect to this unprimed crystallographic system. For this conductor, the normalized change in resistance can be expressed in terms of the off-axis (primed) stress components using

$$\begin{aligned}\frac{\Delta R}{R} &= \frac{R(\sigma, T) - R(0, 0)}{R(0, 0)} \\ &= (\pi'_{1\alpha}\sigma'_\alpha)l'^2 + (\pi'_{2\alpha}\sigma'_\alpha)m'^2 + (\pi'_{3\alpha}\sigma'_\alpha)n'^2 \\ &\quad + 2(\pi'_{4\alpha}\sigma'_\alpha)l'n' + 2(\pi'_{5\alpha}\sigma'_\alpha)m'n' + 2(\pi'_{6\alpha}\sigma'_\alpha)l'm' \\ &\quad + \left[\alpha_1 T + \alpha_2 T^2 + \cdots\right] \end{aligned} \tag{1}$$

where

$\pi'_{\alpha\beta}(\alpha, \beta = 1, 2, \ldots, 6)$ off-axis temperature dependent piezoresistive coefficients;

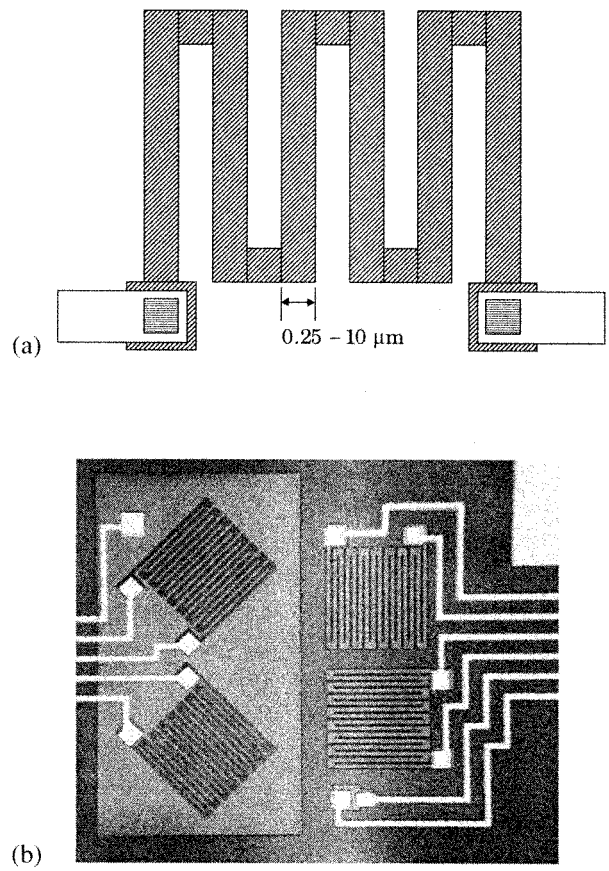

Fig. 3. (a) Serpentine pattern used in typical sensor applications. (b) Photomicrograph of resistor sensors.

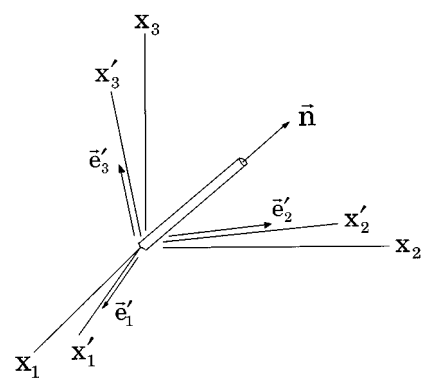

Fig. 4. Filamentary silicon conductor.

$\alpha_1, \alpha_2, \ldots$ temperature coefficients of resistance;

$T = T_m - T_{ref}$ difference between the measurement temperature and reference temperature [where the unstressed reference value of resistance $R(0, 0)$ is measured];

l', m', n' direction cosines of the conductor orientation with respect to the x'_1, x'_2, x'_3 axes, respectively.

Equation (1) assumes that geometrical changes and second-order piezoresistivity can be neglected and that the piezoresistive coefficients are independent of temperature,

although this later assumption can be removed [21]. In (1) and future indicial notation expressions, the summation convention is implied for repeated indices, and reduced index notation has been used for the stress components:

$$\begin{aligned}\sigma_1' &= \sigma_{11}',\ \sigma_2' = \sigma_{22}',\ \sigma_3' = \sigma_{33}' \\ \sigma_4' &= \sigma_{13}',\ \sigma_5' = \sigma_{23}',\ \sigma_6' = \sigma_{12}'.\end{aligned} \tag{2}$$

The 36 off-axis piezoresistive coefficients in (1) are related to the three unique on-axis piezoresistive coefficients $\pi_{11}, \pi_{12}, \pi_{44}$ (evaluated in the unprimed coordinate system aligned with the crystallographic axes) using the transformation

$$\pi_{\alpha\beta}' = T_{\alpha\gamma}\pi_{\gamma\delta}T_{\delta\beta}^{-1} \tag{3}$$

where

$$[\pi_{\alpha\beta}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{4}$$

is the on-axis piezoresistive coefficient matrix, and (5), as shown at the bottom of the page, is the 6×6 transformation matrix in which l_i, m_i and n_i are the direction cosines of the x_i' axis with respect to the x_1, x_2 and x_3 axes respectively.

When the primed axes are aligned with the unprimed (crystallographic) axes, the transformation matrix in (5) reduces to the 6×6 identity matrix. Thus, (3) reduces to $\pi_{\alpha\beta}' = \pi_{\alpha\beta}$ and (1) simplifies to

$$\begin{aligned}\frac{\Delta R}{R} = &[\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})]l^2 \\ &+ [\pi_{11}\sigma_{22} + \pi_{12}(\sigma_{11} + \sigma_{33})]m^2 \\ &+ [\pi_{11}\sigma_{33} + \pi_{12}(\sigma_{11} + \sigma_{22})]n^2 \\ &+ 2\pi_{44}[\sigma_{12}lm + \sigma_{13}\ln + \sigma_{23}mn] \\ &+ \left[\alpha_1 T + \alpha_2 T^2 + \cdots\right]\end{aligned} \tag{6}$$

where l, m, and n are the direction cosines of the conductor orientation with respect to the unprimed (crystallographic) axes. Equation (6) demonstrates that the resistance change of an arbitrarily oriented silicon resistor depends on all six stress components, the three unique piezoresistive coefficients and temperature. As will be shown below, resistive sensor rosettes can be fabricated in certain silicon wafer planes that take advantage of this property and allow several stress components to be extracted from monitoring of resistance changes.

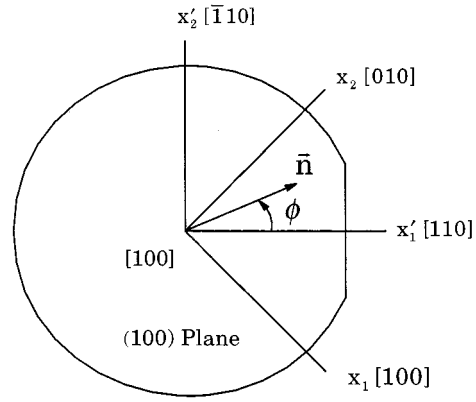

Fig. 5. The (100) silicon wafer.

B. Resistance Change Equations for Common Silicon Wafer Planes

For a given wafer orientation, (1) can be used to obtain the resistance change equation for an arbitrarily oriented in-plane resistor. Although silicon wafers can be obtained with many surface orientations, the (100) and (111) surfaces represent commonly utilized orientations.

1) (100) Silicon: In the current microelectronics industry, the vast majority of silicon devices are fabricated using (100) silicon wafers as depicted in Fig. 5. The surface of the wafer is a (100) plane, and the [100] direction is normal to the wafer plane. The axes of the natural wafer coordinate system $x_1' = [110]$ and $x_2' = [\bar{1}10]$ lie parallel and perpendicular to the primary wafer flat. These axes are chosen so that the individual normal stresses are resolved in directions parallel to the edges of standard IC chips, and they also correspond to the orientation of most resistors and transistors in integrated circuits. To use (1), the off-axis piezoresistive coefficients in the primed coordinate system must be evaluated using (3) by substitution of the unprimed values in (4) and the appropriate direction cosines. For the unprimed and primed coordinate systems shown in Fig. 5, the direction cosines are

$$[a_{ij}] = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{7}$$

$$[T_{\alpha\beta}] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & l_1n_3 + l_3n_1 & m_1n_3 + m_3n_1 & l_1m_3 + l_3m_1 \\ l_2l_3 & m_2m_3 & n_2n_3 & l_2n_3 + l_3n_2 & m_2n_3 + m_3n_2 & l_2m_3 + l_3m_2 \\ l_1l_2 & m_1m_2 & n_1n_2 & l_1n_2 + l_2n_1 & m_1n_2 + m_2n_1 & l_1m_2 + l_2m_1 \end{bmatrix} \tag{5}$$

Substitution of the off-axis piezoresistive coefficients calculated in the manner described above into (1) yields

$$\begin{aligned}\frac{\Delta R}{R} = &\left[\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{11}\right.\\ &\left.+\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{22}\right]\cos^2\phi\\ &+\left[\left(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}\right)\sigma'_{11}\right.\\ &\left.+\left(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}\right)\sigma'_{22}\right]\sin^2\phi\\ &+\pi_{12}\sigma'_{33}+(\pi_{11}-\pi_{12})\sigma'_{12}\sin 2\phi\\ &+\left[\alpha_1 T+\alpha_2 T^2+\cdots\right] \qquad (8)\end{aligned}$$

where $l' = \cos\phi$, $m' = \sin\phi$, and $n' = 0$ have been introduced, and ϕ is the angle between the x'_1-axis and the resistor orientation. Equation (8) indicates that the out-of-plane shear stresses σ'_{13} and σ'_{23} do not influence the resistances of stress sensors fabricated on (100) wafers. This means that a sensor rosette on (100) silicon can at best measure four of the six unique components of the stress tensor. All three of the unique piezoresistive coefficients for silicon (π_{11}, π_{12}, π_{44}) appear in (8); these parameters must be calibrated before stress component values can be extracted from resistance change measurements.

Typical room temperature values of the piezoresistive coefficient values appear in Table I for lightly doped silicon [3], [4]. As doping increases, the piezoresistive response decreases [5], [6], [9], and the coefficients can be substantially smaller than the Table I values for heavily doped resistors (ones made using FET source/drain regions for example). However, the tabulated values do provide important comparative information as well as upper bounds on the coefficients. On the (100) surface, π_{44} is the largest coefficient for p-type material whereas the values of π_{11} and π_{12} are very small. For n-type material, π_{44} is small, but the other two individual coefficients are relatively large. In (8), the parameters π_{11} and π_{12} always appear together in sum and difference terms, and we define the sum and difference of these coefficients as $\pi_S = \pi_{11}+\pi_{12}$ and $\pi_D = \pi_{11}-\pi_{12}$. Note from Table I that π_D has a very large value in n-type material.

2) (111) Silicon: The other common silicon crystal orientation used in semiconductor fabrication is the (111) surface. A general (111) silicon wafer is shown in Fig. 6. The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes $x_1 = [100]$, $x_2 = [010]$, and $x_3 = [001]$ no longer lie in the wafer plane and have not been indicated. As mentioned previously, it is convenient to work in an off-axis primed wafer coordinate system where the x'_1 and x'_2 axes are parallel and perpendicular to the primary wafer flat, and correspond to the edges of fabricated IC die. Using (1), the resistance change of an arbitrarily oriented in-plane sensor can be expressed in terms of the stress components resolved in this natural wafer coordinate system. The off-axis piezoresistive coefficients in the primed coordinate system must be first evaluated by substituting the unprimed values given in (4) and the appropriate direction cosines for the primed coordinate directions with respect to the unprimed (crystallographic) coordinate directions into the transformation relations given in (3) and (5). For the primed coordinate system indicated in Fig. 6, the appropriate direction cosines for the primed axes are

TABLE I
TYPICAL PIEZORESISTIVE COEFFICIENT VALUES FOR LIGHTLY DOPED SILICON $(\text{TPa})^{-1}$ [3], [4]

Piezoresistive Coefficient	n-type Silicon	p-type Silicon
π_{11}	-1022	66
π_{12}	534	-11
π_{44}	-136	1381
$\pi_S = \pi_{11} + \pi_{12}$	-488	55
$\pi_D = \pi_{11} - \pi_{12}$	-1556	77
B_1	-312	718
B_2	297	-228
B_3	61	-448

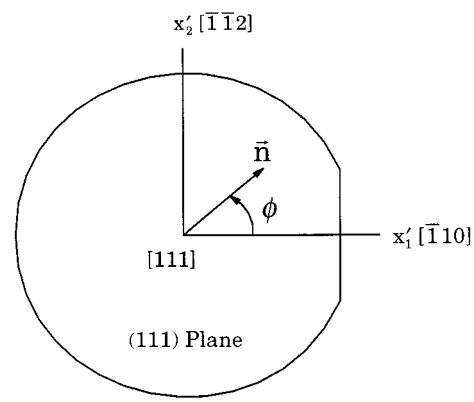

Fig. 6. The (111) silicon wafer.

$$[a_{ij}] = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & \frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix}. \qquad (9)$$

Substitution of the off-axis piezoresistive coefficients, calculated in the manner described above, into (1) yields

$$\begin{aligned}\frac{\Delta R}{R} = &\left[B_1\sigma'_{11}+B_2\sigma'_{22}+B_3\sigma'_{33}+2\sqrt{2}(B_2-B_3)\sigma'_{23}\right]\cos^2\phi\\ &+\left[B_2\sigma'_{11}+B_1\sigma'_{22}+B_3\sigma'_{33}-2\sqrt{2}(B_2-B_3)\sigma'_{23}\right]\sin^2\phi\\ &+\left[2\sqrt{2}(B_2-B_3)\sigma'_{13}+(B_1-B_2)\sigma'_{12}\right]\sin 2\phi\\ &+\left[\alpha_1 T+\alpha_2 T^2+\cdots\right] \qquad (10)\end{aligned}$$

where ϕ is again the angle between the x_1'-axis and the resistor orientation. The coefficients

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \qquad B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6}$$
$$B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3} \tag{11}$$

are a set of linearly independent temperature dependent combined piezoresistive parameters. These parameters must be calibrated before stress component values can be extracted from resistance change measurements. Typical values of the "B" coefficients for lightly doped material also appear in Table I. In n-type material, B_1 and B_2 are the largest coefficients whereas B_3 is quite small. B_1 and B_3 are the largest for p-type material, although all three coefficients have useful values. It is very important to note that the general resistance change expression in (10) is dependent on all six of the unique stress components. Therefore, the potential exists for developing a sensor rosette that can measure the complete 3-D state of stress at points on the surface of a die by using (111) silicon.

C. Rosette Design

From (8), the resistance change of an in-plane sensor fabricated on (100) silicon is observed to depend on four components of stress (σ_{11}, σ_{22}, σ_{33}, σ_{12}) and the orientation of the sensor. Likewise, from (10), the resistance change of an in-plane sensor fabricated on (111) silicon is found to depend upon all six stress components and the orientation of the sensor. Because of this, it is natural to assume that the potential exists to design a four-element rosette on (100) silicon capable of measuring four stress components, and a six-element rosette on (111) silicon capable of measuring all six stress components. However, it can also be proved theoretically that, when considering all possible resistor orientations at a point, there are only three unique (linearly independent) responses on any given silicon plane [15], [22], [23]. Therefore, it appears that it is not possible to design a rosette that can measure more than three stress components. The above discussion pertains to rosettes formed with identically doped sensing resistors. The full potential of multi-element sensor rosettes to measure up to six stress components can be achieved by using dual-polarity sensing elements fabricated with both n-type and p-type silicon. Since the piezoresistive coefficients of the n-type and p-type resistors are different, there can be up to six unique sensor responses in dual-polarity rosettes.

Besides the ability to measure two additional stress components, theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have other advantages relative to sensors fabricated using standard (100) silicon [21]–[23]. In particular, optimized sensors on (111) silicon are capable of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities. In this discussion, temperature compensated refers to the ability to extract the stress components directly from the resistance change measurements without the need to know the temperature change T. This is particularly important attribute, given the large errors which can be introduced into nontemperature compensated stress sensor data when the temperature change T is not precisely known [24], [25]. Furthermore, by using computer analysis with symbolic algebra to consider all possible silicon wafer orientations, it has been established that the (111) plane in fact offers the opportunity to measure the highest number (four) of stress components in a temperature compensated manner [22], [23]. The four stress components that can be measured in a temperature compensated manner are the three shear stress components and the difference of the in-plane normal stress components.

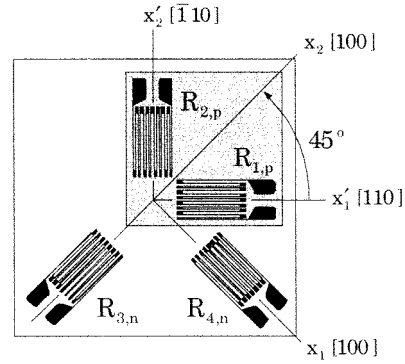

Fig. 7. Four-element rosette on (100) silicon.

D. Optimized Four-Element Rosette on (100) Silicon

A four-element dual-polarity sensor rosette on (100) is shown in Fig. 7. The rosette contains a 0–90° p-type resistor pair and a ±45° n-type resistor pair. This choice of sensor orientations minimizes thermally induced errors as well as those due to resistor misalignment relative to the true crystallographic axes [25], and permits accurate temperature compensated measurement of the values of the in-plane normal stress difference ($\sigma_{11}' - \sigma_{22}'$) and the in-plane shear stress σ_{12}' as outlined below.

Application of (8) to the four resistor orientations gives the following relations between the resistance changes and the stresses at the rosette site:

$$\frac{\Delta R_1}{R_1} = \frac{(\pi_S^p + \pi_{44}^p)}{2}\sigma_{11}' + \frac{(\pi_S^p - \pi_{44}^p)}{2}\sigma_{22}' + \pi_{12}^p\sigma_{33}' + \alpha_1^p T$$
$$\frac{\Delta R_2}{R_2} = \frac{(\pi_S^p - \pi_{44}^p)}{2}\sigma_{11}' + \frac{(\pi_S^p + \pi_{44}^p)}{2}\sigma_{22}' + \pi_{12}^p\sigma_{33}' + \alpha_1^p T$$
$$\frac{\Delta R_3}{R_3} = \frac{\pi_S^n}{2}(\sigma_{11}' + \sigma_{22}') + \pi_D^n\sigma_{12}' + \pi_{12}^n\sigma_{33}' + \alpha_1^n T$$
$$\frac{\Delta R_4}{R_4} = \frac{\pi_S^n}{2}(\sigma_{11}' + \sigma_{22}') - \pi_D^n\sigma_{12}' + \pi_{12}^n\sigma_{33}' + \alpha_1^n T \tag{12}$$

where $\pi_S = (\pi_{11} + \pi_{12})$ and $\pi_D = (\pi_{11} - \pi_{12})$ now appear, and superscripts n and p are used to denote the piezoresistive coefficients of the n-type and p-type resistors, respectively. The expressions in (12) can be inverted to yield equations for the four stress components σ_{11}', σ_{22}', σ_{33}', σ_{12}' in terms of the resistance changes of the sensing elements, the piezoresistive coefficients π_{11}^n, π_{12}^n, π_{44}^n, π_{11}^p, π_{12}^p and π_{44}^p, and the temperature change T. Direct combination of the expressions in (12) also leads to the

following two temperature compensated (i.e., independent of T) resistance-stress expressions

$$(\sigma'_{11} - \sigma'_{22}) = \frac{1}{\pi^p_{44}}\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right]$$
$$\sigma'_{12} = \frac{1}{2\pi^n_D}\left[\frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4}\right]. \quad (13)$$

The piezoresistive coefficients needed to solve for the stress components can be measured using a combination of uniaxial and hydrostatic pressure calibration testing [26], [27]. A photograph of a fabricated four-element dual-polarity rosette appears in Fig. 3. The choice of n- and p-type material for the four resistors is based upon the values of π^p_{44} and π^n_D in Table I.

E. Requirement for Temperature Compensated Measurements

The (100) sensor rosette in Fig. 7 provides a good example of the source and magnitude of the potential for thermally induced measurement errors which arise because silicon resistors have relatively large temperature coefficients, as high as 1000–2000 ppm/°C.

Assuming $\sigma'_{33} = 0$ and solving for σ'_{11} and σ'_{22} using the first two equations in (12) yields

$$\sigma'_{11} = \frac{\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2}\right]}{2\pi_S} + \frac{\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right]}{2\pi_{44}} - \frac{\alpha_1 T}{\pi_S}$$
$$\sigma'_{22} = \frac{\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_2}{R_2}\right]}{2\pi_S} - \frac{\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right]}{2\pi_{44}} - \frac{\alpha_1 T}{\pi_S}. \quad (14)$$

Using values of $\pi_s = 25 \times 10^{-12}$ Pa^{-1} and $\alpha_1 = 1000$ ppm/°C for p-type silicon, a 0.5 degree measurement error in the temperature change T corresponds to an error in each estimated stress component of 20 MPa. Typical measured values of stress range from zero to a few hundred MPa. Thus a miscalculation of 20 MPa can represent a significant error, particularly for low values of stress. As sensor doping increases, the value of π_s can become vanishingly small, further aggravating the problem. For a typical value of $\pi_s = 250 \times 10^{-12}$ Pa^{-1} for n-type silicon, the same 0.5 degree temperature measurement error corresponds to a stress component error of only 2 MPa. If one attempts to find σ'_{11} and σ'_{22} with a 0–90° resistor rosette, it is therefore best to utilize n-type sensors. However, the n-type resistor pair exhibits high sensitivity to rotational errors in sensor alignment to the true crystallographic directions, which result in corruption of the extracted stress values by the presence of shear stress [25].

It is important to understand the potential sources of thermal errors. Quantity T represents the difference between the temperature at the time the reference value $R(0, 0)$ was measured, and the temperature at the time the second measurement $R(\sigma, T)$ is taken. In many packaging applications, these measurements may be taken several months apart, and any of the following factors are equivalent to a temperature error:

i) actual temperature measurement errors;
ii) uncertainty in resistor measurements;
iii) instrument calibration drift between the times of the two sets of measurements;
iv) measurement of the values of $R(0, 0)$ and $R(\sigma, T)$ with different instruments with differing calibration errors.

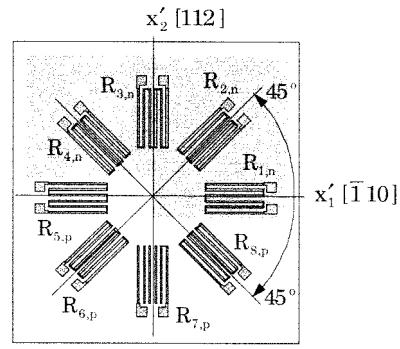

Fig. 8. Optimized eight-element rosette on (111) silicon.

As can be observed from (12) and (14), any attempt to resolve the individual normal stress components σ'_{11}, σ'_{22} or σ'_{33} will involve terms of the form $(\Delta R_i/R_i + \Delta R_j/R_j)$ and will thus contain temperature terms. Because of the stringent absolute temperature measurement requirements, past claims in the literature of stress measurements with accuracy of a few MPa or less are probably exaggerated. It is recommended that only temperature compensated stress calculations be used, unless a short-term, well-controlled set of experiments is utilized. These thermal errors also make accurate measurement of higher order piezoresistive coefficients [10], [28], [29] extremely difficult.

F. Optimized Eight-Element Rosette on (111) Silicon

The eight-element dual-polarity rosette on (111) silicon illustrated in Fig. 8 contains p-type and n-type sensor sets, each with resistor elements making angles of $\phi = 0, \pm 45, 90°$ with respect to the x'_1-axis. This sensor has been developed by the authors for measurement of the complete state of stress at points on the surface of a packaged semiconductor die. It has been optimized to measure four stress components in a temperature compensated manner, and the "B" coefficients can be readily calibrated using a combination of uniaxial and hydrostatic testing. A six-element rosette (without the $-45°$ resistors) can also be used to extract the complete stress state. However, including the two extra resistors allows for more convenient bridge measurements of the resistance changes and better stress measurement localization [22], [23].

Repeated application of (10) to each of the piezoresistive sensing elements leads to the following expressions for the stress-induced resistance changes:

$$\frac{\Delta R_1}{R_1} = B^n_1\sigma'_{11} + B^n_2\sigma'_{22} + B^n_3\sigma'_{33} + 2\sqrt{2}(B^n_2 - B^n_3)\sigma'_{23} + \left[\alpha^n_1 T + \alpha^n_2 T^2 + \cdots\right]$$
$$\frac{\Delta R_2}{R_2} = \left(\frac{B^n_1 + B^n_2}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B^n_3\sigma'_{33} + 2\sqrt{2} \cdot (B^n_2 - B^n_3)\sigma'_{13} + (B^n_1 - B^n_2)\sigma'_{12} + \left[\alpha^n_1 T + \alpha^n_2 T^2 + \cdots\right]$$

$$\begin{aligned}
\frac{\Delta R_3}{R_3} &= B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}\left(B_2^n - B_3^n\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^n T + \alpha_2^n T^2 + \cdots\right] \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^n \sigma'_{33} - 2\sqrt{2} \\
&\quad \cdot \left(B_2^n - B_3^n\right)\sigma_{13} - \left(B_1^n - B_2^n\right)\sigma'_{12} \\
&\quad + \left[\alpha_1^n T + \alpha_2^n T^2 + \cdots\right] \\
\frac{\Delta R_5}{R_5} &= B_1^p \sigma_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}\left(B_2^p - B_3^p\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \cdots\right] \\
\frac{\Delta R_6}{R_6} &= \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} + 2\sqrt{2} \\
&\quad \cdot \left(B_2^p - B_3^p\right)\sigma'_{13} + \left(B_1^p - B_2^p\right)\sigma'_{12} \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \cdots\right] \\
\frac{\Delta R_7}{R_7} &= B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}\left(B_2^p - B_3^p\right)\sigma'_{23} \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \cdots\right] \\
\frac{\Delta R_8}{R_8} &= \left(\frac{B_1^p + B_2^p}{2}\right)\left(\sigma'_{11} + \sigma'_{22}\right) + B_3^p \sigma'_{33} - 2\sqrt{2} \\
&\quad \cdot \left(B_2^p - B_3^p\right)\sigma'_{13} - \left(B_1^p - B_2^p\right)\sigma'_{12} \\
&\quad + \left[\alpha_1^p T + \alpha_2^p T^2 + \cdots\right]. \qquad (15)
\end{aligned}$$

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively.

For an arbitrary state of stress, these expressions can be inverted to solve for the six stress components in terms of the measured resistance changes, as shown in (16) at the bottom of the next page. In (16), only the first order temperature terms have been retained. From the expressions in (16), it is clear that the extraction of the three shear stresses σ'_{12}, σ'_{13}, σ'_{23} from the measured resistance changes is independent of T. Evaluation of the three normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change T experienced by the sensing elements. The temperature coefficients of resistance $\alpha_1, \alpha_2, \ldots$ must also be known for each doping type. They can be obtained using thermal cycling calibration experiments where the resistances of the sensing elements are monitored as a function of temperature. The measured resistance change versus temperature response is fit with a general polynomial to extract the temperature coefficients of resistance. Typically, only first and second order temperature coefficients are needed [27].

The difficulties in obtaining accurate temperature change values over the long time spans typical of measurements made with piezoresistive sensors (e.g., before and after die encapsulation) were mentioned in the previous section and they apply equally to the (111) sensors. If the overall coefficients dividing the $\alpha_1 T$ terms in (16) are calculated, one finds that they are relatively small, particularly for n-type resistors. Thus, it is again recommended to restrict measurement efforts to temperature compensated stress combinations where the temperature coefficient of resistance terms cancel in the stress extraction equations. Besides the three shear stresses, an additional temperature compensated quantity can be obtained by subtracting the expressions for the in-plane normal stresses σ'_{11} and σ'_{22} in (16):

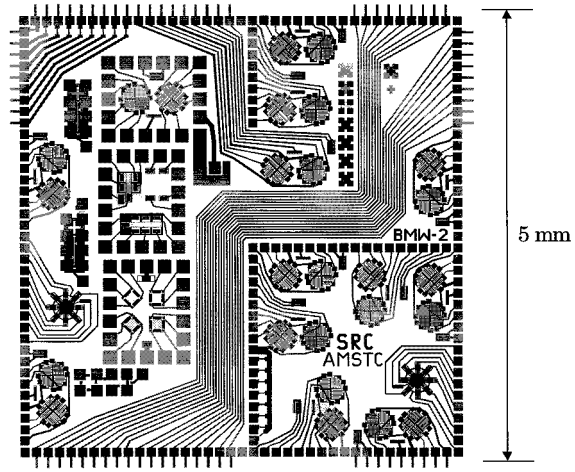

Fig. 9. The (111) silicon test chip for making stress measurements.

$$\sigma'_{11} - \sigma'_{22} = \frac{\left(B_3^p - B_2^p\right)\left[\dfrac{\Delta R_1}{R_1} - \dfrac{\Delta R_3}{R_3}\right] - \left(B_3^n - B_2^n\right)\left[\dfrac{\Delta R_5}{R_5} - \dfrac{\Delta R_7}{R_7}\right]}{\left[\left(B_2^p - B_1^p\right)B_3^n + \left(B_1^p - B_3^p\right)B_2^n + \left(B_3^p - B_2^p\right)B_1^n\right]}. \qquad (17)$$

The reason for the choice of eight resistors becomes apparent upon study of (16) and (17). The four temperature compensated terms each involve only four resistors, grouped in pairs of like doping type. This is required for temperature compensation since it would be unlikely that the temperature coefficients of the n- and p-type resistors are the same. In addition, only the 0–90 resistors appear in the expressions for $(\sigma'_{11} - \sigma'_{22})$ and σ'_{23}, whereas only the $\pm 45°$ degree resistors appear in the expressions for σ'_{12} and σ'_{13}.

III. Test Chip Designs

When piezoresistive sensors are used in experimental stress analysis studies of microelectronic packages, special test chips are typically designed and fabricated. The test chips have arrays of sensor rosettes and are used to replace the normal functional die used in a package of interest. In our recent research efforts, several generations of (111) stress sensor chips have been designed, fabricated, and characterized for use in packaging studies. These test die contain an array of the optimized eight-element dual polarity measurement rosettes shown in Fig. 8, and either perimeter pads suitable for wire bonding or area array pads for flip chip applications. In the fabrication processes, ion-implantation has been used to achieve the best possible resistor matching and uniformity. Careful layout techniques were also used to maximize resistance and stress sensitivity matching, and to minimize sensitivity to mask misalignment during fabrication.

The basic die image of a typical (111) silicon test chip (BMW-2) is shown in Fig. 9 [30], [31]. This 200×200 mil

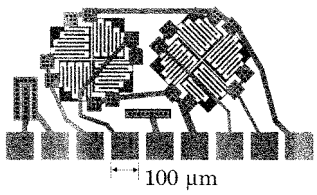

Fig. 10. Eight-element rosette layout as half bridges (BMW-2 test chip).

(5×5 mm) die contains 12 eight-element rosettes, diodes at each rosette site for temperature measurement, and additional calibration sites and process test structures. A typical rosette layout and its connection to the perimeter bond pads are shown in Fig. 10. The eight-element rosettes are interconnected as half-bridge circuits, which minimizes the number of pads needed to completely access all sensors in a given rosette. In the fabrication process, the doping concentration level for both resistor types was chosen to be approximately $10^{18}/\text{cm}^3$, and nominal resistor values of 12–15 kΩ were obtained.

With the BMW-2 chip design, the wafer can be cut into larger chips on any 5 mm increment in either direction. The repeated basic die images are interconnected through the kerf (scribe) areas on the wafer using the shorting bars extending from the pads in Fig. 9. These inter-chip connections provide access to interior sensors (from the outer perimeter pads) on larger composite die up to 30 mm on a side.

IV. Sensor Calibration

The unique piezoresistive coefficients which characterize the silicon resistive sensors must be calibrated before stress component values can be extracted from resistance change measurements using formulas such as appear in (12)–(17). Each of the (100) and (111) surfaces has its own set of required coefficient values as well as unique problems associated with obtaining these values.

A. Calibration of Sensors on the (100) Surface

For the optimized four-element rosette on the (100) surface, the values of π_{44}^p and π_D^n are needed. Based upon (12), it is clear that π_{44}^p can be easily determined through a controlled isothermal application of uniaxial stress to a sensor rosette while

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n\right]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n\right]}$$

$$\sigma'_{22} = -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2\left[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n\right]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n\right]}$$

$$\sigma'_{33} = \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2\left[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n\right]}$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{(B_2^p - B_1^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - (B_2^n - B_1^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-(B_2^p - B_1^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + (B_2^n - B_1^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

$$\sigma'_{12} = \frac{-(B_3^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + (B_3^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2\left[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n\right]} \tag{16}$$

monitoring the resulting resistance changes, and the uniaxial stress can easily be applied using the four-point-bending apparatus described in the next section. Unfortunately, it is difficult to apply a well-controlled shear stress that would be required to determine π_D^n. However, using the theory in Section II, the authors have shown that the individual values of π_{11}, π_{12}, π_{44}, π_S, and π_D can all be measured using the special three-element "off-axis" rosette in Fig. 11 [32]. Strips for calibration also must be cut from the wafer at a 22.5° angle, and applying uniaxial stress along the axis of this strip produces an equivalent shear stress when resolved in the coordinate system of the rosette. An additional advantage of this form of calibration is that the values of π_{44} and π_D are obtained in a temperature compensated measurement.

B. Calibration of Sensors on the (111) Surface

The expressions in (15)–(17) for the eight-element (111) silicon rosette in Fig. 8 indicate that a calibration procedure must be performed to determine all six of the combined piezoresistive parameters B_1^n, B_2^n, B_3^n, B_1^p, B_2^p, B_3^p prior to using the sensor rosette for stress measurements. From (15), which describe resistor variations on the (111) surface, it is apparent that values of B_1 and B_2 can be found from application of a uniaxial stress. For example, if a known uniaxial stress $\sigma'_{11} = \sigma$ is applied in the x'_1-direction, the expressions in (15) for the 0–90° oriented sensors yield the following resistance changes:

$$\frac{\Delta R_1}{R_1} = B_1^n\sigma + \alpha_1^n T, \qquad \frac{\Delta R_3}{R_3} = B_2^n\sigma + \alpha_1^n T$$
$$\frac{\Delta R_5}{R_5} = B_1^p\sigma + \alpha_1^p T, \qquad \frac{\Delta R_7}{R_7} = B_2^p\sigma + \alpha_1^p T. \quad (18)$$

From these expressions, it is clear that the constants B_1^n, B_2^n, B_1^p, B_2^p can be easily determined through a controlled isothermal application of uniaxial stress to a sensor rosette while monitoring the resulting resistance changes. However, the values of B_3 are more difficult to determine.

It can be observed in (15) that characterization of material constant B_3 for (111) sensors requires the die to be subjected to a controlled stress state that has nonzero out-of-plane normal or shear stresses. Hydrostatic calibration has proven to be the most expedient method to satisfy this condition. If a sensor rosette is subjected to hydrostatic pressure $(\sigma'_{11} = \sigma'_{22} = \sigma'_{33} = -p)$, the relations in (15) give

$$\frac{\Delta R_1}{R_1} = \frac{\Delta R_2}{R_2} = \frac{\Delta R_3}{R_3} = \frac{\Delta R_4}{R_4} = -[B_1^n + B_2^n + B_3^n]p + \alpha_1^n T$$
$$\frac{\Delta R_5}{R_5} = \frac{\Delta R_6}{R_6} = \frac{\Delta R_7}{R_7} = \frac{\Delta R_8}{R_8} = -[B_1^p + B_2^p + B_3^p]p + \alpha_1^p T. \quad (19)$$

Therefore, the combinations $(B_1^n + B_2^n + B_3^n)$ and $(B_1^p + B_2^p + B_3^p)$, referred to as the piezoresistive pressure coefficients, can be evaluated through a controlled isothermal application of a hydrostatic pressure to a sensor rosette while monitoring the resulting resistance changes. The individual values of B_3^n and B_3^p can then be obtained by combining the hydrostatic pressure calibration results with the uniaxial stress calibration results. From Table I, the values of the pressure coefficients are expected to be small for lightly doped material, and, from a practical point of view, it may often be acceptable to simply assume they are zero.

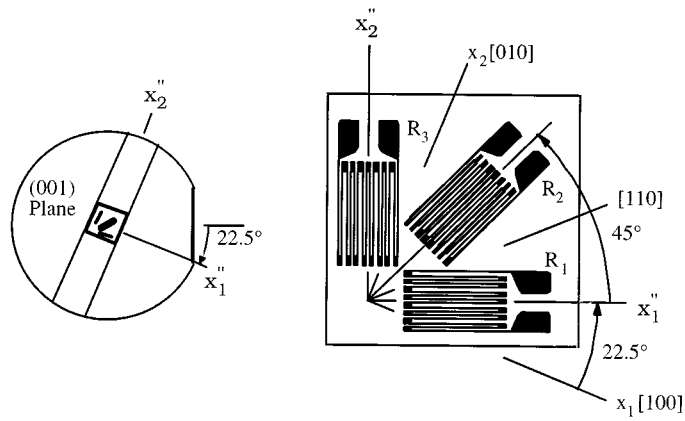

Fig. 11. Three-element 22.5° off-axis calibration rosette.

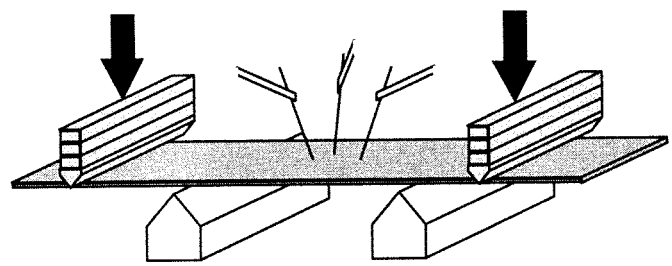

Fig. 12. Four-point bending calibration.

Four-point bending and pressure vessel testing have been used to generate the required uniaxial and hydrostatic calibration loadings. In the four-point-bending method, a rectangular strip containing a row of chips is cut from a wafer and is loaded in a four-point-bending beam fixture to generate uniaxial stress states (see Fig. 12) [26]. As observed in (15) and (18), this technique allows coefficients B_1 and B_2 to be measured for both the p-type and n-type resistors in the dual polarity eight-element rosette on (111) silicon. Sample four-point-bending calibration measurements for the p-type resistors on the BMW-2 test chip appear in Fig. 13. The linearity and orientation dependence of the resistor responses to stress are apparent in the figure. Similar results apply to n-type resistors and to calibration rosettes on (100) silicon.

In our hydrostatic testing procedure, a high-capacity pressure vessel has been used to subject a single die to triaxial compression [27]. As indicated by (19), temperature compensated hydrostatic measurements cannot be made, so that temperature changes occurring during testing represent a potential problem. It has been observed experimentally that the hydraulic fluid temperature change due to a 14 MPa pressure change is on the order of 0.8 °C. Because of the relatively large temperature coefficients of resistance of silicon, the temperature effects must be removed from hydrostatic calibration data before evaluating the piezoresistive pressure coefficient $\pi_p = -(B_1 + B_2 + B_3)$. To remove the temperature induced resistance changes, an accurate determination of the temperature coefficient of resistance

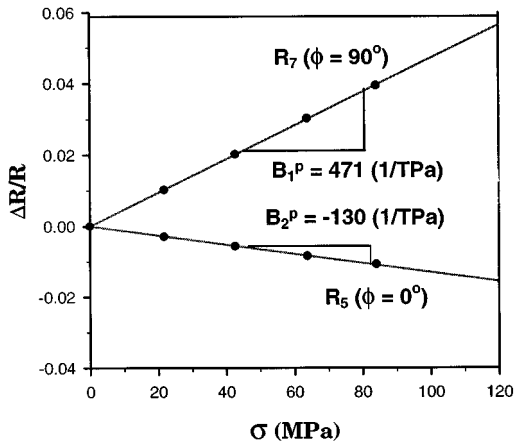

Fig. 13. Typical four-point bending results (p-type resistors, eight-element rosette).

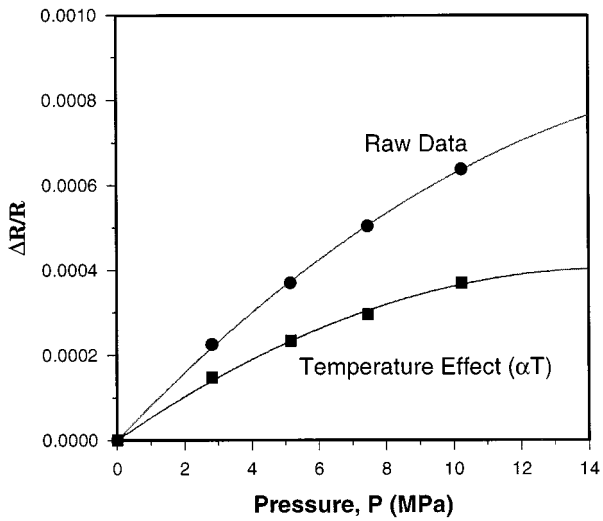

Fig. 14. Typical hydrostatic calibration data (p-type resistor).

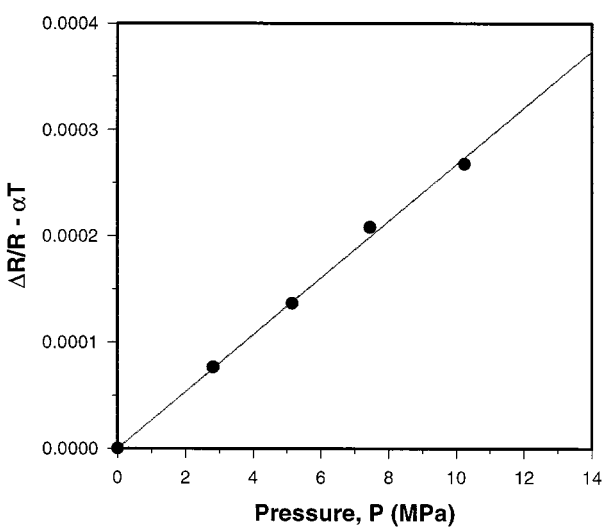

Fig. 15. Adjusted hydrostatic calibration data (p-type resistor).

(TCR) α_1 of a sensor must be done prior to pressure coefficient measurement.

TABLE II
TYPICAL PIEZORESISTIVE COEFFICIENT VALUES FOR BMW-2 TEST CHIPS $(\text{TPa})^{-1}$ [30]

Piezoresistive Coefficient	n-type Silicon	p-type Silicon
B_1	-230	507
B_2	207	-145
B_3	55	-399

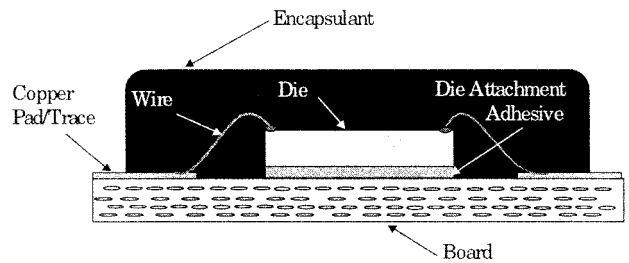

Fig. 16. Wire bonded chip-on-board packaging.

As an example, typical resistance change with temperature behavior for unstressed p-type resistors in the BMW-2 test chip were recorded using a computer temperature-controlled oven, and an average value of $\alpha_1^p = 2.11 \times 10^{-3}/°\text{C}$ was found. Once TCR measurements were completed, the die were subjected to hydrostatic pressure. During these tests, the resistances of the sensors and the fluid temperature were monitored at every load step. Typical resistance change with pressure behavior is depicted in Fig. 14. If the temperature of the fluid didn't change under pressure, the raw data curve in Fig. 14 should have been linear according to (19). Nonlinearity is present because of the nonlinear variation of the hydraulic fluid temperature during pressurization. Adjusted resistance versus pressure data were obtained by subtracting the temperature induced resistance change $(\alpha_1 T)$ from the total resistance change at each data point. As observed in Fig. 15, the adjusted resistance change data are linear with fluid pressure as expected. The slope of the curve in Fig. 15 is the piezoresistive pressure coefficient $\pi_p = -(B_1 + B_2 + B_3)$. Similar results are obtained for n-type resistors. Typical values of the measured B coefficients found for the BMW-2 test chips appear in Table II.

V. TEST CHIP PACKAGING APPLICATIONS

Test chips incorporating piezoresistive stress sensors can be used in a wide variety of ways to evaluate assembly and packaging technologies, and this section provides a sample of the possibilities. Stress test chips are useful for measuring processing induced die stress as a function of various manufacturing variables. In this role, they can be used to guide material selection processes (e.g., encapsulants). In addition, test chips can be used for *in-situ* stress measurements during processing or final end use of the electronic component. When using (111) silicon sensors, interfacial shear stresses between the die

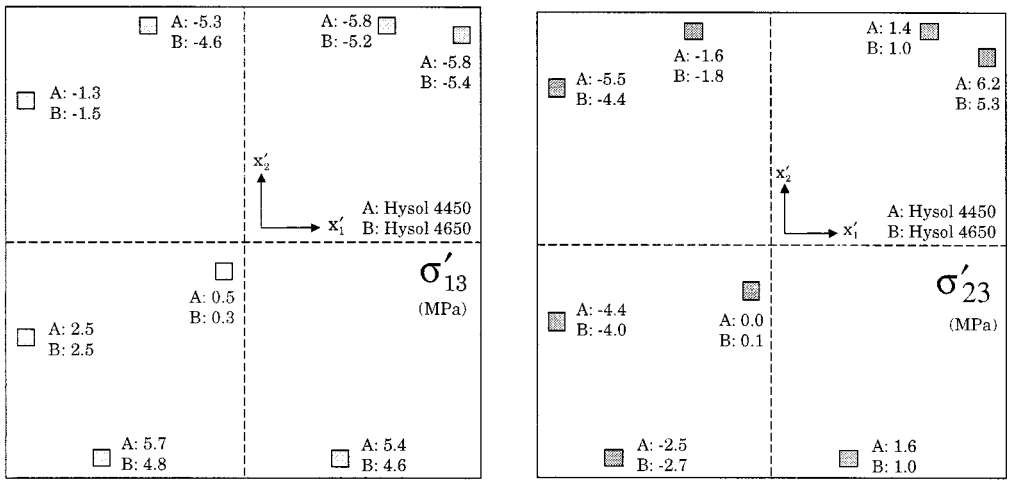

Fig. 17. Out-of-plane shear stress data in COB packages (room temperature—400×400 Mil Die).

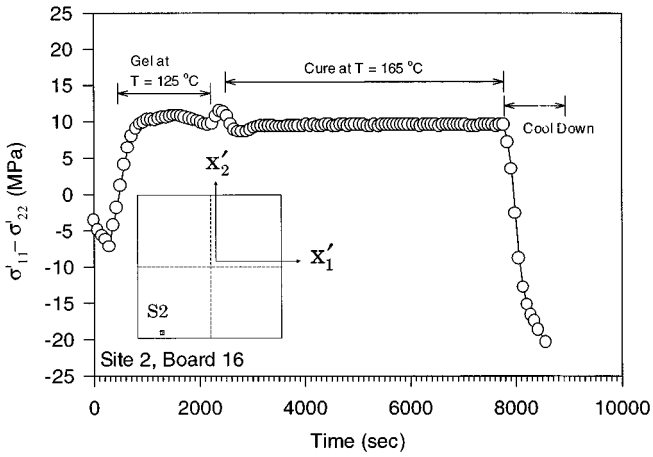

Fig. 18. Typical variation of die stress during the encapsulant cure cycle.

surface and encapsulant can be monitored as a tool for delamination detection and monitoring of interfacial crack growth. Finally, stress test chips can be used to measure the changes in die stresses occurring during various types of electronic packaging reliability testing such as thermal cycling, thermal aging, highly accelerated stress testing (HAST), and long-term moisture adsorption. In such applications, the changes in stress are often a direct indication of the damage that has occurred in the encapsulant or die attachment material contacting the chip.

In Section V-A-C, brief examples are provided of different applications of piezoresistive stress sensors to the assembly and packaging of microelectronics. In each case, an the experimental measurement approach is critical since it is very difficult if not impossible to accurately predict the mechanical response using numerical simulation methods (e.g., finite element analysis). The challenges with the finite element approach include such issues as unknown material constitutive behavior of the encapsulants during solidification, difficulty in predicting delamination initiation and 3-D crack growth, and lack of models for material damage and degradation of materials such as viscoplastic encapsulants and solders.

A. Die Stresses During Chip-on-Board Assembly

In chip-on-board (COB) technologies, semiconductor die are attached directly to a second level substrate (e.g., ceramic or organic circuit board). Such assemblies have become popular for multichip module (MCM) applications requiring reliable packaging with reasonable costs. In wire bonded COB (chip-and-wire), the chip level interconnect is done by wire bonding. The chip is attached to the substrate with a die attachment adhesive (e.g., silver-filled epoxy), and the outer leads are then bonded. Finally, the die is encapsulated using a "glob-top" liquid encapsulant (see Fig. 16).

In our work, a 2×2 array (a 10 mm $\times$ 10 mm die) of the (111) silicon test chips in Fig. 9 have been used to characterize the variation of die stress throughout the COB packaging process [30], [31]. The initial sensor resistances of all sensors were recorded when the test die were in wafer form. The rosettes were later characterized after die attachment, and throughout the cure cycle of the liquid encapsulant. Using the measured data and appropriate theoretical equations, the stresses at sites on the die surface have been calculated. Also, preliminary 3-D nonlinear finite element simulations of the chip on board packages were performed, and the stress predictions were correlated with the experimental test chip data. Fig. 17 shows typical room temperature data for the out-of-plane shear stress components and two different encapsulants. In this illustration, the small squares represent the size and locations of the sensor rosettes. From the data it is clear that encapsulant "B" provides final assemblies with lower interfacial shear stresses, leading to better reliability. In Fig. 18, a typical stress variation during the encapsulant cure process is shown. Several effects can be clearly seen including the cure shrinking that occurs during the hold at 165 °C, and the significant stress buildup that occurs during assembly cool down. The transient overshoot and relaxation of the stress value is also interesting since the oven temperature change was measured to be monotonic. Note that these measurements track differential changes in stress with time, and the resolution of the changes is a fraction of a MPa. These results are possible only using the temperature compensated measurement approach discussed earlier.

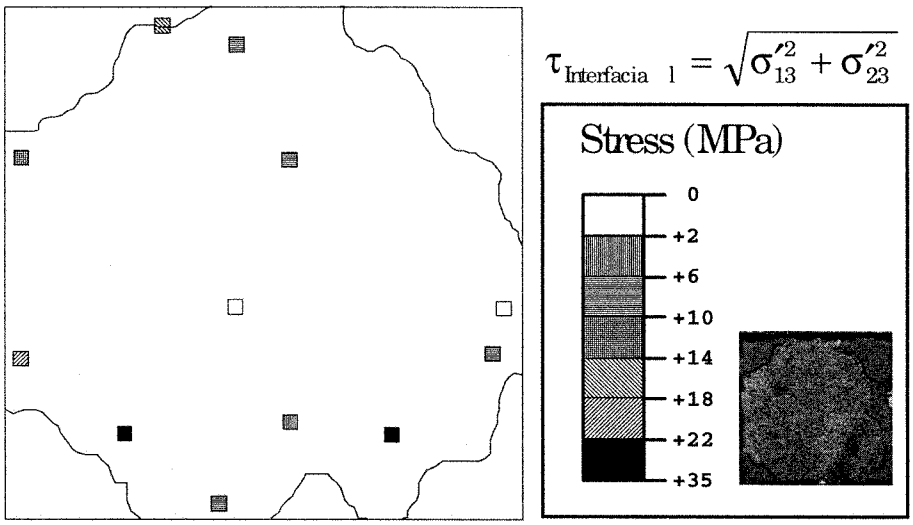

Fig. 19. Total out-of-plane shear stress data for a typical delaminated die (400×400 Mil).

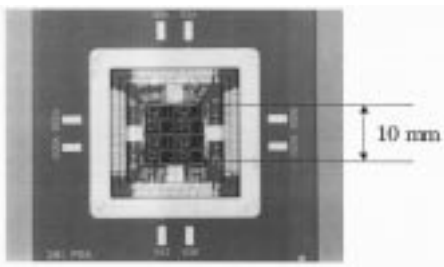

Fig. 20. PGA package with stress test chip.

B. Delamination in Plastic Encapsulated Packages

In conventional plastic encapsulated packages, chips are first attached to a metal lead frame using a silver filled epoxy adhesive. Small diameter gold wires are used to electrically interconnect the small bond pads on the silicon die to the thin metallic leads. The assembly is then encapsulated in an injection molding machine, and the metal legs are shaped in a forming die. Once assembled, several plastic encapsulated packages are typically surface mounted to a printed circuit board using solder.

In our plastic package studies, calibrated and characterized (100) and (111) test chips were encapsulated in 240 pin quad flat packs (QFPs) [33]. The post packaging room temperature resistances of the sensors were then recorded, and the stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. The presence of delaminations between the die surface and the encapsulant was explored using C-mode scanning acoustic microscopy (C-SAM). Stress test chips fabricated with (111) silicon have shown great potential for detecting delaminations and for aiding the understanding of stress distributions in delaminated packages. For example, Fig. 19 shows the distribution of the total out-of-plane shear stress on the die surface of a partially delaminated QFP. The delaminations begin at the four corners of the die, and the delamination boundary (as determined via C-SAM) is shown as a curved line. In nondelaminated die, the out-of-plane (interfacial) shear stresses σ'_{13} and σ'_{23} are relatively small, except very near the die edges. For example, in our measurements in chip on board packages shown in Fig. 17, the measured magnitudes of these stresses were typically in the range of 0–6 MPa. However, in the delaminated QFPs, the magnitudes of these stresses became very high (up to 50 MPa). This was especially true at nondelaminated rosette sites that were very near the edge of the delamination region. Rosettes in the delaminated regions were found to have failed completely (open circuits) due to the delamination damage.

C. Stress Changes in Pin Grid Array Packages Due to Reliability Testing

In a ceramic pin grid array (PGA) package, a silicon chip is bonded within the cavity of a multilayer ceramic package with metal pin leads using a die attachment adhesive. Fine aluminum wires are used to provide the interconnections from the die bond pads to the metal traces on the PGA housing, and the cavities are typically sealed using Kovar lids and an Au–Sn eutectic preform. Fig. 20 shows a photograph of a typical PGA package (lid removed) with attached (111) silicon stress test chip.

In this investigation, 10 mm $\times$ 10 mm test chips were attached to the PGA packages using six high-temperature die attachment adhesives designed for avionic applications [34]. The adhesive systems included silver filled glasses, polyimide pastes, thermoplastic films, and gold germanium adhesives. The resistances of the sensors were recorded at room temperature before and after die attachment. The induced thermal stresses at sites on the die surface have been calculated using the measured resistance changes and piezoresistive theory. A comparison of the room temperature die stresses caused by the different die-attachment materials has been made.

After the initial stress measurements, thermal aging and thermal cycling tests were conducted on the packages. The thermal aging consisted of subjecting the packages to 2000 hours of exposure at 260 °C. The thermal cycling experiments consisted of exposure to 1000 thermal cycles from -55 to 260 °C. The various die attachment materials were further evaluated by observing the changes in stress that occurred during these reliability tests. For example, the thermal aging

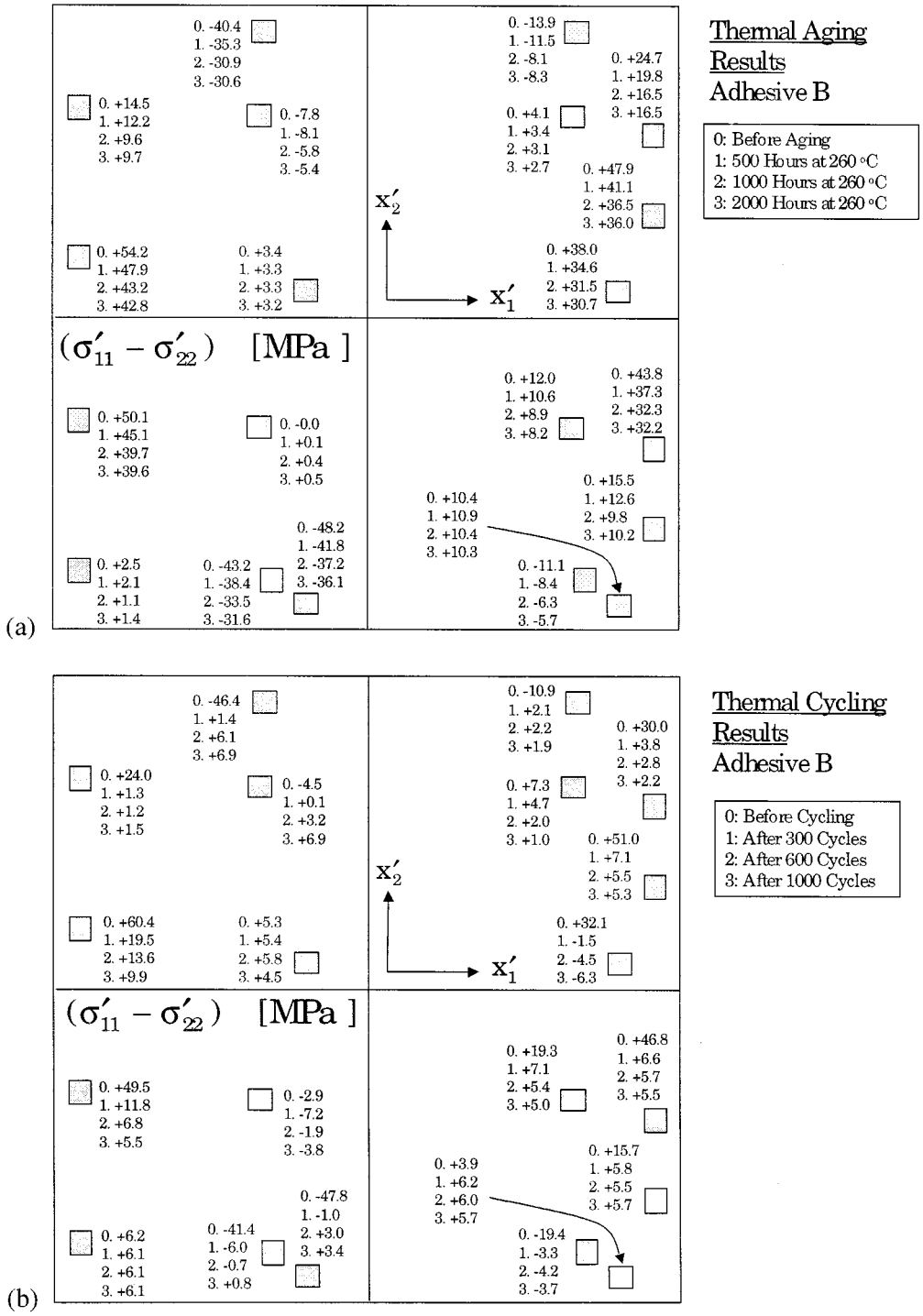

Fig. 21. Effects of (a) thermal aging and (b) cycling on die surface stresses (in-plane normal stress difference in MPa).

and thermal cycling test results for one of the die attachment adhesives are shown in Fig. 21. From the data, it is seen that this adhesive survived the thermal aging tests but experienced gradual damage (stresses reduced gradually during the aging process). However, the same material failed the thermal cycling tests (stresses quickly changed to zero indicating loss of adhesion). In both sets of tests, the primary failure mode was observed to be die attachment adhesive cracking.

VI. Device and Circuit Parametric Shifts Due to Stress

Packaging induced die stresses change the effective hole and electron mobilities observed at semiconductor device terminals, and thus directly affect the characteristics of both analog and digital circuits on IC chips [35]–[40]. Because of this problem, various research groups have extensively characterized the response of FETs to stress [40]–[45] for a wide range of operating

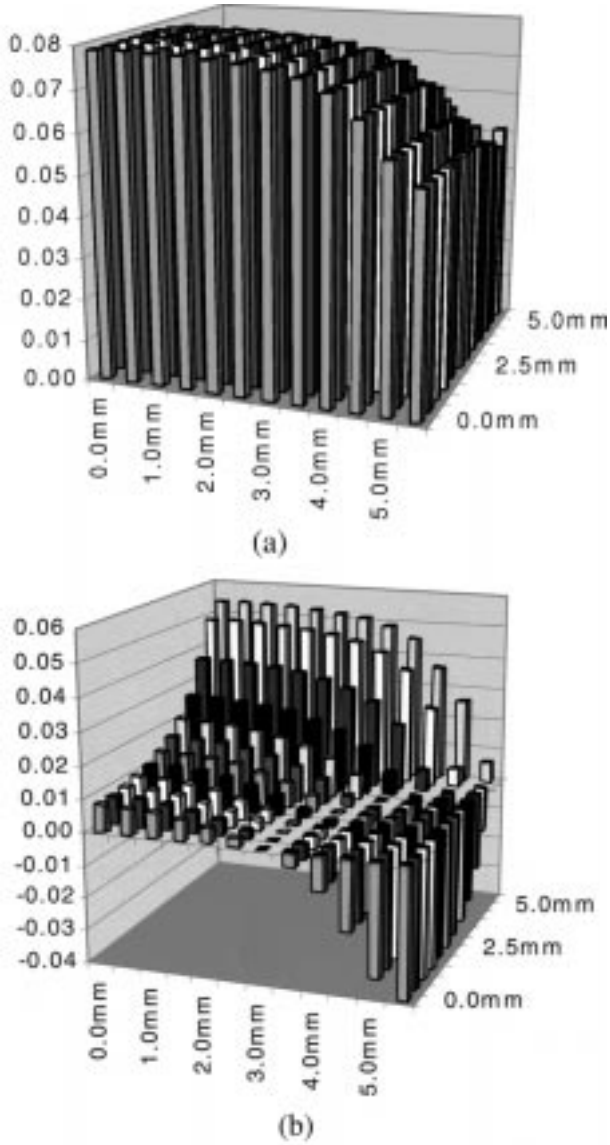

Fig. 22. (a) Calculated stress-induced NMOS drain current variation across one quadrant of a 10 mm × 10 mm plastic encapsulated die. (b) Corresponding variation in PMOS drain current.

conditions. For FETs operating in strong inversion, the piezoresistive theory in (12) can be readily extended to describe the behavior of MOS field-effect transistors in strong inversion.

A. MOSFET Drain Current Variation

For example, the drain current of MOSFETs with channels oriented at 0 and 90° on the (100) surface can be expressed as

$$\left.\frac{\Delta I_D}{I_D}\right|_0 = \frac{\Pi_S}{2}(\sigma'_{11}+\sigma'_{22}) + \frac{\Pi_{44}}{2}(\sigma'_{11}-\sigma'_{22}) + \Pi_{12}\sigma'_{33}$$
$$\left.\frac{\Delta I_D}{I_D}\right|_{90} = \frac{\Pi_S}{2}(\sigma'_{11}+\sigma'_{22}) - \frac{\Pi_{44}}{2}(\sigma'_{11}-\sigma'_{22}) + \Pi_{12}\sigma'_{33} \tag{20}$$

in which the Π_{ij} represent the piezoresistive coefficients of the FET channel resistance. The magnitudes of these coefficients approach the lightly doped values of resistor π_{ij} presented in Table I, but have the opposite signs since a change in conductivity is being modeled rather than a change in resistivity. Based upon these values, one can expect n-channel devices to be most affected by the value of the in-plane normal stress sum $(\sigma'_{11} + \sigma'_{22})$, which is relatively high across most of the surface in a large plastic encapsulated die for example. On the other hand, PMOS devices will have the strongest dependence upon $(\sigma'_{11} - \sigma'_{22})$, which can be high and also changes sign across the die surface. An example of the calculated affects of stress are presented in Fig. 22, which shows the drain current enhancement in one quadrant of a 400 mil × 400 mil plastic encapsulated die. The NMOS devices exhibit an 8% increase in mobility over most of the die surface, because the die is under a large biaxial compressive stress. At the same time, the PMOS devices show a wide (almost 10%) spread in values because of the large magnitude and changing sign of the $(\sigma'_{11} - \sigma'_{22})$ term. These device changes will translate directly into changes and spreads in the performance distribution of analog and digital circuits fabricated on similar IC chips.

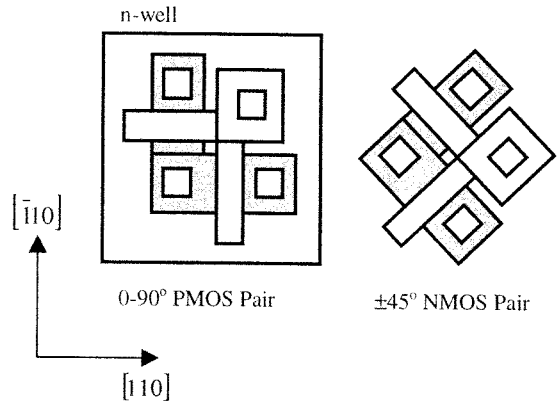

Fig. 23. CMOS sensor rosette on (100) silicon. Such a rosette could occupy an area of 250 μm^2 or less.

B. MOSFETs as Stress Sensors

As stress sensors, CMOS FETs offer a number of advantages [46]–[49]. First they can be made very small in size to provide a highly localized stress measurement. In addition, large sensor arrays can be fabricated to fully map the stress field. The light doping in the MOS channel leads to high stress sensitivity, and MOSFETs are known to operate well from high temperatures down to cryogenic temperatures below 77K. Fig. 23 provides an example of the layout of a CMOS stress sensor rosette on (100) silicon which consists of a 0–90° pair of PMOS transistors and a ±45° pair of NMOS transistors. The PMOS pair produces an output proportional to $(\sigma'_{11} - \sigma'_{22})$ and the NMOS pair is used to measure σ'_{12}. Since FETs can be made extremely small, large numbers of the rosettes in Fig. 23 can potentially be placed in the area occupied by a single bonding pad in the chip in Fig. 9!

An example application of CMOS stress sensors appears in Fig. 24, which displays the results of die stress measurements in a small (2×2 mm) die over the range of 420K to 90K [50], [51]. The difference of the in-plane normal stresses versus temperature is plotted for a high stress site near the edge of the die, and the shear stress versus temperature is plotted for a high stress site near the die corner. The stress variation with temperature is

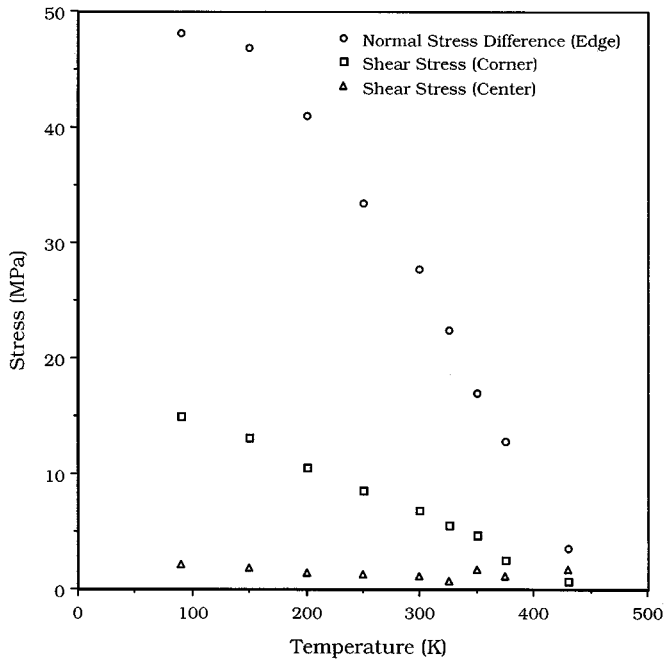

Fig. 24. Extracted normal stress difference $(\sigma'_{11} - \sigma'_{22})$ for edge sensor and in-plane shear stress σ'_{12} for corner and line of symmetry sensors versus temperature.

also shown for a low stress location on a line of symmetry at the die center. This sensor output should be nearly zero as is measured, indicating that the temperature compensation is in fact working properly.

VII. Summary and Conclusions

The use of piezoresistive sensors for experimental stress measurements in electronic packages has been reviewed, and sensor theory has been presented in detail. Optimized resistive sensor rosettes designed for application on both the commonly available (100) and (111) silicon surfaces were discussed, and the importance of performing temperature compensated measurements was emphasized. Sensor rosettes fabricated on (111) silicon have several advantages, including the ability to measure the complete state of stress (six stress components) and the ability to measure four temperature compensated stress components. Sensor calibration methods were presented. An "off-axis" rosette can be utilized for calibration purposes on the (100) surface. On the (111) surface, the six piezoresistive coefficients can be completely determined from the measurement rosettes using a combination of uniaxial and hydrostatic calibration experiments.

Example applications of piezoresistive test chips to chip-on-board assemblies, plastic encapsulated packages, and pin grid array packages were presented. These examples demonstrated the ability of test chip stress sensors to evaluate *in-situ* processing induced stresses, detect delaminations, and characterize material damage during reliability testing. Although beyond the scope of this paper, the results presented here are equally applicable to other forms of piezoresistive sensors including pressure sensors, accelerometers, microphones, etc.

Piezoresistive theory can also be extended directly to the resistive channel region of MOSFETs operating in strong inversion, and an example extension of stress theory to the prediction of parametric device and circuit changes in packaged integrated circuits was included in this paper. As stress sensors, CMOS FETs can provide highly localized stress measurements, and large sensor arrays can be fabricated to fully map the stress field. The light doping in the MOS channel leads to high stress sensitivity, and MOSFETs are known to operate well from high temperatures down to cryogenic temperatures below 77K. An example of where stress measurements were made from 420K to 77K was presented here.

Although this paper has focused on the use of piezoresisitive sensors in electronic packaging applications, they have also found wide application in MEMS devices including accelerometers and pressure sensors, and the theoretical development presented here is directly applicable to many areas beyond the scope of this presentation.

References

[1] P. W. Bridgeman, "The effect of homogenous mechanical stress on the electrical resistance of crystals," *Phys. Rev.*, vol. 42, pp. 858–863, 1932.

[2] P. W. Bridgman, "The effect of pressure on the electrical resistance of certain semiconductors," *Proc. Amer. Acad. Arts Sci.*, vol. 79, no. 3, pp. 125–179, 1951.

[3] C. S. Smith, "Piezoresistance effect in silicon and germanium," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, 1954.

[4] W. P. Mason and R. N. Thurston, "Use of piezoresistive materials in the measurement of displacement, force, and torque," *J. Acoust. Soc. Amer.*, vol. 29, no. 10, pp. 1096–1101, 1957.

[5] W. G. Pfann and R. N. Thurston, "Semiconducting stress transducers utilizing the transverse and shear piezoresistance effects," *J. Appl. Phys.*, vol. 32, no. 10, pp. 2008–2019, 1961.

[6] O. N. Tufte and E. L. Stelzer, "Piezoresistive properties of heavily doped n-type silicon," *Phys. Rev.*, vol. 133, pp. A1705–A1716, 1964.

[7] W. Paul and G. L. Pearson, "Pressure dependence of the resistivity of silicon," *Phys. Rev.*, vol. 98, pp. 1755–1757, 1955.

[8] F. J. Morin, T. H. Geballe, and C. Herring, "Temperature dependence of the piezoresistance of high-purity silicon and germanium," *Phys. Rev.*, vol. 105, no. 2, pp. 525–539, 1957.

[9] Y. Kanda, "A graphical representation of the piezoresistive coefficients in silicon," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 64–70, Jan. 1982.

[10] K. Yamada *et al.*, "Nonlinearity of the piezoresistance effect of p-type silicon diffused layers," *IEEE Trans. Electron Devices*, vol. ED–29, pp. 71–77, Jan. 1982.

[11] J. L. Spencer, W. H. Schroen, G. A. Bednarz, J. A. Bryan, T. D. Metzgar, R. D. Cleveland, and D. R. Edwards, "New quantitative measurements of IC stress introduced by plastic packages," in *Proc. 19th IEEE Annu. Reliability Phys. Symp.*, New York, 1981, pp. 74–80.

[12] D. R. Edwards, G. Heinen, G. A. Bednarz, and W. H. Schroen, "Test structure methodology of IC package material characterization," in *Proc. 33rd IEEE Electron. Components Conf.*, New York, 1983, pp. 386–393.

[13] D. R. Edwards, K. G. Heinen, J. E. Martinez, and S. Groothuis, "Shear stress evaluation of plastic packages," in *Proc. 37th IEEE Electron. Components Conf.*, New York, 1987, pp. 84–95.

[14] S. A. Gee, W. F. van den Bogert, and V. R. Akylas, "Strain-gauge mapping of die surface stresses," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 12, no. 4, pp. 587–593, 1989.

[15] D. A. Bittle, J. C. Suhling, R. E. Beaty, R. C. Jaeger, and R. W. Johnson, "Piezoresistive stress sensors for structural analysis of electronic packages," *J. Electron. Packag.*, vol. 113, no. 3, pp. 203–215, 1991.

[16] L. T. Nguyen, S. A. Gee, and W. F. van den Bogert, "Effects of configuration on plastic package stress," *J. Electron. Packag.*, vol. 113, no. 4, pp. 397–404, 1991.

[17] J. N. Sweet and D. W. Peterson, "High accuracy die mechanical stress measurement with the ATC04 assembly test chip," in *Proc. IEEE Int. Reliability Workshop*, pp. 1–8.

[18] H. Miura, M. Kitano, A. Nishimura, and S. Kawai, "Thermal stress measurement in silicon chips encapsulated in IC plastic packages under thermal cycling," *J. Electron. Packag.*, vol. 115, no. 1, pp. 9–15, 1993.

[19] J. N. Sweet, "Die stress measurement using piezoresistive stress sensors," in *Thermal Stress and Strain in Microelectronics Packaging*, J. Lau, Ed. New York: Von Nostrand Reinhold, 1993, pp. 221–271.

[20] R. van Gestel, "Reliability related research on plastic IC packages: A test chip approach," Ph.D. dissertation, Delft Technical Univ., The Netherlands, 1994.

[21] J. C. Suhling, R. E. Beaty, R. C. Jaeger, and A. W. Johnson, "Piezoresistive stress sensors for measurement of thermally-induced stresses in microelectronics," in *Proc. Spring Conf. Soc. Experimental Mechanics*, Milwaukee, WI, June 10–13, pp. 683–694.

[22] R. A. Cordes, J. C. Suhling, Y. Kang, and R. C. Jaeger, "Optimal temperature compensated piezoresistive stress sensor Rosettes," in *Proc. Symp. Applicat. Experimental Mechanics Electron. Packaging, ASME, EEP*, vol. 13, 1995, pp. 109–116.

[23] J. C. Suhling, R. C. Jaeger, B. M. Wilamowski, S. T. Lin, A. K. M. Mian, and R. A. Cordes, "Design and calibration of optimized (111) silicon stress sensing test chips," in *Proc. INTERpack,*, Kohala, HI, June 15–19, 1997, pp. 1721–1729.

[24] R. C. Jaeger, J. C. Suhling, and R. Ramani, "Thermally induced errors in the application of silicon piezoresistive stress sensors," in *Advances in Electronic Packaging —Proc. ASME Int. Electron. Packaging Conf.*, Binghamton, NY, Sept. 29–Oct. 2, 1993, pp. 457–470.

[25] R. C. Jaeger, J. C. Suhling, and R. Ramani, "Errors associated with the design, calibration of piezoresistive stress sensors in (100) silicon," *IEEE Trans. Compon., Packag., Manufact. Technol. B*, vol. 17, pp. 97–107, Feb. 1994.

[26] R. C. Jaeger, R. E. Beaty, J. C. Suhling, R. W. Johnson, and R. D. Butler, "Evaluation of piezoresistive coefficient variation in silicon stress sensors using a four-point bending test fixture," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. 15, pp. 904–914, 1992.

[27] Y. Kang, A. K. M. Mian, J. C. Suhling, R. C., and Jaeger, "Hydrostatic response of piezoresistive stress sensors," in *Application of Experimental Mechanics to Electronic Packaging*. Dallas, TX: ASME, Int. Mech. Eng. Congr. Expo., November 16–21, 1997, vol. 22, pp. 29–36.

[28] H. J. McSkimin, W. L. Bond, E. Buehler, and G. K. Teal, "Measurement of the elastic constants of silicon single crystals and their thermal coefficients," *Phys. Rev.*, vol. 83, p. 1080, 1951.

[29] H. J. McSkimin and P. Andreatch, "Measurement of third-order moduli of silicon and germanium," *J. Appl. Phys.*, vol. 35, no. 11, pp. 3312–3319, 1964.

[30] Y. Zou, J. C. Suhling, R. W. Johnson, and R. C. Jaeger, "Complete stress state measurements in chip on board packages," in *Proc. Int. Conf. Multichip Modules High Density Packaging,*, Denver, CO, April 15–17, 1998, pp. 425–435.

[31] Y. Zou, J. C. Suhling, R. W. Johnson, R. C. Jaeger, and A. K. M. Mian, "*In-situ* stress state measurements during chip-on-board assembly," *IEEE Trans. Electron. Packag. Manufact.*, vol. 22, pp. 38–52, Jan. 1999.

[32] R. C. Jaeger, J. C. Suhling, M. T. Carey, and R. W. Johnson, "Off-axis piezoresistive sensors for measurement of stress in electronic packaging," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. 16, pp. 925–931, Aug. 1993.

[33] Y. Zou, J. C. Suhling, R. C. Jaeger, and H. Ali, "Three-dimensional die surface stress measurements in delaminated and nondelaminated plastic packaging," in *Proc. 48th Electron. Compon. and Technol. Conf.,*, Seattle, WA, May 25–28, 1998, pp. 1223–1234.

[34] Y. Zou, S. T. Lin, J. C. Suhling, R. C. Jaeger, J. T. Benoit, and R. R. Grzybowski, "Die surface stress variation during thermal cycling and thermal aging reliability tests," in *Proc. 49th Electron. Compon. Technol. Conf.*, San Diego, CA, June 1–4, 1999, pp. 1249–1260.

[35] S. Gee, T. Doan, and K. Gilbert, "Stress related offset voltage shift in a precision operational amplifier," in *IEEE ECTC Dig.*, 1993, pp. 755–764.

[36] H. Miura and A. Nishimura, "Device characteristic changes caused by packaging stress," *ASME AMD*, vol. 195, pp. 101–109, 1994.

[37] R. C. Jaeger, R. Ramani, and J. C. Suhling, "Effects of stress-induced mismatches on CMOS analog circuits," in *Proc. Int. VLSI TSA Symp.*, Taipei, Taiwan, R.O.C., May 1995, pp. 354–360.

[38] J. Bastos, M. Steyaert, B. Graindourze, and W. Sansen, "Influence of die attachment on MOS transistor matching," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Sept. 1996, pp. 27–31.

[39] H. Ali, "Stress-induced parametric shift in plastic packaged devices," *IEEE Trans. Compon., Packag. Manufact. Technol. B*, vol. 20, Nov. 1997.

[40] R. C. Jaeger, A. T. Bradley, J. C. Suhling, and Y. Zou, "FET mobility degradation and device mismatch due to packaging induced die stress," in *Proc. 23rd Eur. Solid-State Circuits Conf.,*, Sept. 1997, pp. 272–275.

[41] D. Colman, R. T. Bate, and J. P. Mize, "Mobility anisotropy and piezoresistance in silicon p-type inversion layers," *J. Appl. Phys.*, pp. 1923–1931, Mar. 1968.

[42] A. P. Dorey and T. S. Maddern, "The effect of strain on MOS transistors," *Solid-State Electron.*, vol. 12, pp. 185–189, 1969.

[43] H. Mikoshiba, "Stress-sensitive properties of silicon-gate MOS devices," *Solid-State Electron.*, vol. 24, pp. 221–232, 1981.

[44] A. Hamada, T. Furusawa, and E. Takeda, "A new aspect of mechanical stress effects in scaled MOS devices," in *Proc. Symp. VLSI Techn. Conf.*, June 1990, pp. 113–114.

[45] Z. Z. Wang, J. Suski, D. Collard, and E. Dubois, "Piezoresistivity effects in N-MOSFET devices," in *Proc. Int. Conf. Solid-State Sensors and Actuators,*, 1991, pp. 1024–1027.

[46] A. P. Dorey, "A high sensitivity semiconductor strain sensitive circuit," *Solid-State Electron.*, vol. 18, pp. 295–299, 1975.

[47] J. Neumeister, G. Schuster, and W. von Munch, "A silicon pressure sensor using MOS ring oscillators," *Sens. Actuators*, vol. 7, pp. 167–176, 1985.

[48] R. C. Jaeger, R. Ramani, J. C. Suhling, and Y. Kang, "CMOS stress sensor circuits using piezoresistive field-effect transistors (PIFET's)," in *1995 Symp. VLSI Circuits Dig. Tech. Papers*, June 1995, pp. 43–44.

[49] H. Takao, Y. Matsumoto, and M. Ishida, "A monolithically integrated three-axis accelerometer using CMOS compatible stress-sensitive differential amplifiers," *IEEE Trans. Electron. Devices*, vol. 46, pp. 109–116, Jan. 1999.

[50] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and J. Xu, "CMOS stress sensors on (100) silicon," *IEEE J. Solid-State Circuits*, vol. 35, pp. 85–95, Jan. 2000.

[51] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and Y. Zou, "Die stress characterization using arrays of CMOS sensors," *IEEE Trans. Adv. Packag.*, submitted for publication.

Jeffrey C. Suhling (M'94) was born in Wisconsin in 1958. He received the B.S. degree in applied mathematics, engineering, and physics (with Distinction) in 1980, and the M.S. and Ph.D. degrees in engineering mechanics in 1981 and 1985, respectively, all from the University of Wisconsin, Madison.

He currently a Professor with the Department of Mechanical Engineering, Auburn University, Auburn, AL. His initial appointment at Auburn was in 1985. His research interests include the application of analytical, numerical, and experimental methods of solid mechanics to problems in electronic packaging. He has authored over 125 technical publications and advised over 40 graduate students. He and his co-workers have attracted over $13 000 000 in externally funded research projects to Auburn University.

Dr. Suhling is a member of the IEEE CPMT Society, the American Society of Mechanical Engineers (ASME), the Society for Experimental Mechanics (SEM), the International Microelectronics and Packaging Society (IMAPS), and the Technical Association of the Pulp and Paper Industry (TAPPI). His currently serves on the Executive Board of the Electrical and Electronic Packaging Division of ASME and has served as a Technical Track Chair for the InterPACK '99 Conference. He is a member of the Phi Beta Kappa, Phi Kappa Phi, and Sigma XI honorary societies. From 1980 to 1983, he received a National Science Foundation Graduate Fellowship. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students at Auburn during 1990 and received the College of Engineering Birdsong Superior Teaching Award in 1994.

Richard C. Jaeger (F'86) was born in New York, NY, on September 2, 1944. He received the B.S. and M.E. degrees in electrical engineering in 1966 and the Ph.D. degree in 1969, all from the University of Florida, Gainesville.

From 1969 to 1974, he was with the IBM Corporation, Boca Raton, FL, working on technology for precision data acquisition systems and small computer architecture. In 1974, he became a Research Staff Member at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His interests included analog integrated circuits, I^2L, low temperature MOS device behavior, and microprocessor design. In 1976, he returned to IBM, where he continued work on understanding the behavior of MOS devices at low temperatures and studying architectural alternatives for small computer systems. He holds three patents and received two Invention Achievement Awards from the IBM Corporation. In 1979, he joined Auburn University, Auburn, AL, where he is now Distinguished University Professor in the Electrical Engineering Department. He was instrumental in founding the Alabama Microelectronics Science and Technology Center in 1984 and led its activities through 2000. He has published over 200 technical papers and articles, served as Principal Investigator on more than $8M in research contracts, and authored or co-authored three textbooks: *Introduction to Microelectronic Fabrication* (Reading, MA: Addison Wesley, 1988); *Microelectronic Circuit Design* (New York: McGraw-Hill, 1997), and *Computerized Circuit Analysis Using SPICE Programs*, with B. M. Wilamowski (New York: McGraw-Hill, 1997).

Dr. Jaeger was Program Chairman for the 1993 International Solid-State Circuits Conference and Chairman of the 1990 International VLSI Circuits Symposium. He was a Member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving as its President during 1990 and 1991, and completed a three-year term as Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 1998. From 1980 to 1982, he was founding Editor-in-Chief of *IEEE MICRO* and subsequently received an Outstanding Contribution Award from the IEEE Computer Society for development of that magazine. He later became a Member of the Governing Board of the IEEE Computer Society and was selected a Member of the IEEE Computer Society Golden Core in 1996. He received the 1998 IEEE Education Society McGraw-Hill/Jacob Millman Award for "Development of a Modern and Innovative Design-Oriented Electronic Circuits Text." He was appointed to the Distinguished University Professorship by Auburn University in 1990. He received the Birdsong Merit Teaching Award from the College of Engineering in 1991 and was selected as the Outstanding EE Faculty Member by the undergraduate students in 1993. He has been listed in *Who's Who in America* since 1990.