
# CU Plane Test report

| Hw S. No. | Product Name | RU Mac | SW Version |
|---|---|---|---|
| 2403348700002 | LPRU_v7 | 98:ae:71:01:91:7b | 3.0.6 |

# Test Report

| Test Case | Verdict |
|---|---|
| Base_DL_UL | Fail |
| Extended_DL_UL | Pass |
| 16_QAM_Comp_14_bit_DL_UL | Pass |
| 256_QAM_DL_64_QAM_UL_Comp_12_bit | Fail |

# Test Report DL

**Test purpose :**

The test purpose is to verify the DL test.

**Test environment :**

Normal test conditions.

| Test Case | Channel No | Channel Frequency [GHz] | BS Channel Bandwidth [MHz] | Measured EVM (RMS) [%] | EVM Limit [%] | Output Power [dBm] | Limit Low [dBm] | High Low [dBm] | Verdict |
|---|---|---|---|---|---|---|---|---|---|
| Base_DL_UL | 2 | 3.700005 | 100 | 2.62 | 3.5 | 24.33 | 23.0 | 24.7 | Pass |
| Extended_DL_UL | 2 | 3.700005 | 100 | 2.41 | 3.5 | 24.35 | 23.0 | 24.7 | Pass |
| 16_QAM_Comp_14_bit_DL_UL | 3 | 3.54234 | FR1_100M | 3.45 | 5.0 | 24.29 | 23 | 24.99 | Pass |
| 256_QAM_DL_64_QAM_UL_Comp_12_bit | 3 | 3.54234 | FR1_100M | verify_result_and_capture_screenshot VI_ERROR_CON Error : The specified for the given | 3 | session | 23 | 24.99 | has |

# Base_DL_UL CH2 CRC Table

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|
| #6317395Channel | Slot | CRC Passed | Bit Length |
| PDSCH 1 | 0 | True | 84240 |
| PDSCH 1 | 1 | True | 84240 |
| PDSCH 1 | 2 | True | 84240 |
| PDSCH 1 | 3 | True | 84240 |
| PDSCH 1 | 4 | True | 84240 |
| PDSCH 1 | 5 | True | 84240 |
| PDSCH 1 | 6 | True | 84240 |
| PDSCH 1 | 10 | True | 84240 |
| PDSCH 1 | 11 | True | 84240 |
| PDSCH 1 | 12 | True | 84240 |
| PDSCH 1 | 13 | True | 84240 |
| PDSCH 1 | 14 | True | 84240 |
| PDSCH 1 | 15 | True | 84240 |
| PDSCH 1 | 16 | True | 84240 |
| PDSCH 2 | 0 | True | 792 |
| PDSCH 2 | 1 | True | 792 |
| PDSCH 2 | 2 | True | 792 |
| PDSCH 2 | 3 | True | 792 |
| PDSCH 2 | 4 | True | 792 |
| PDSCH 2 | 5 | True | 792 |
| PDSCH 2 | 6 | True | 792 |
| PDSCH 2 | 10 | True | 792 |
| PDSCH 2 | 11 | True | 792 |
| PDSCH 2 | 12 | True | 792 |
| PDSCH 2 | 13 | True | 792 |
| PDSCH 2 | 14 | True | 792 |
| PDSCH 2 | 15 | True | 792 |
| PDSCH 2 | 16 | True | 792 |
| PDSCH 3 | 7 | True | 35640 |
| PDSCH 3 | 17 | True | 35640 |
| PDSCH 4 | 7 | True | 252 |
| PDSCH 4 | 17 | True | 252 |
| PDCCH 1 | 0 | True | 108 |
| PDCCH 1 | 1 | True | 108 |

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|
| PDCCH 1 | 2 | True | 108 |
| PDCCH 1 | 3 | True | 108 |
| PDCCH 1 | 4 | True | 108 |
| PDCCH 1 | 5 | True | 108 |
| PDCCH 1 | 6 | True | 108 |
| PDCCH 1 | 7 | True | 108 |
| PDCCH 1 | 10 | True | 108 |
| PDCCH 1 | 11 | True | 108 |
| PDCCH 1 | 12 | True | 108 |
| PDCCH 1 | 13 | True | 108 |
| PDCCH 1 | 14 | True | 108 |
| PDCCH 1 | 15 | True | 108 |
| PDCCH 1 | 16 | True | 108 |
| PDCCH 1 | 17 | True | 108 |

**CRC PASS : 48 || CRC FAIL : 0**

# Extended_DL_UL CH2 CRC Table

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|
| #6317395Channel | Slot | CRC Passed | Bit Length |
| PDSCH 1 | 0 | True | 84240 |
| PDSCH 1 | 1 | True | 84240 |
| PDSCH 1 | 2 | True | 84240 |
| PDSCH 1 | 3 | True | 84240 |
| PDSCH 1 | 4 | True | 84240 |
| PDSCH 1 | 5 | True | 84240 |
| PDSCH 1 | 6 | True | 84240 |
| PDSCH 1 | 10 | True | 84240 |
| PDSCH 1 | 11 | True | 84240 |
| PDSCH 1 | 12 | True | 84240 |
| PDSCH 1 | 13 | True | 84240 |
| PDSCH 1 | 14 | True | 84240 |
| PDSCH 1 | 15 | True | 84240 |
| PDSCH 1 | 16 | True | 84240 |
| PDSCH 2 | 0 | True | 792 |
| PDSCH 2 | 1 | True | 792 |
| PDSCH 2 | 2 | True | 792 |
| PDSCH 2 | 3 | True | 792 |
| PDSCH 2 | 4 | True | 792 |
| PDSCH 2 | 5 | True | 792 |
| PDSCH 2 | 6 | True | 792 |
| PDSCH 2 | 10 | True | 792 |
| PDSCH 2 | 11 | True | 792 |
| PDSCH 2 | 12 | True | 792 |
| PDSCH 2 | 13 | True | 792 |
| PDSCH 2 | 14 | True | 792 |
| PDSCH 2 | 15 | True | 792 |
| PDSCH 2 | 16 | True | 792 |
| PDSCH 3 | 7 | True | 35640 |
| PDSCH 3 | 17 | True | 35640 |
| PDSCH 4 | 7 | True | 252 |
| PDSCH 4 | 17 | True | 252 |
| PDCCH 1 | 0 | True | 108 |
| PDCCH 1 | 1 | True | 108 |

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|
| PDCCH 1 | 2 | True | 108 |
| PDCCH 1 | 3 | True | 108 |
| PDCCH 1 | 4 | True | 108 |
| PDCCH 1 | 5 | True | 108 |
| PDCCH 1 | 6 | True | 108 |
| PDCCH 1 | 7 | True | 108 |
| PDCCH 1 | 10 | True | 108 |
| PDCCH 1 | 11 | True | 108 |
| PDCCH 1 | 12 | True | 108 |
| PDCCH 1 | 13 | True | 108 |
| PDCCH 1 | 14 | True | 108 |
| PDCCH 1 | 15 | True | 108 |
| PDCCH 1 | 16 | True | 108 |
| PDCCH 1 | 17 | True | 108 |

**CRC PASS : 48 || CRC FAIL : 0**

# 16_QAM_Comp_14_bit_DL_UL CH3 CRC Table

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|
| #6335013Channel | Slot | CRC Passed | Bit Length |
| PDSCH 1 | 0 | True | 89856 |
| PDSCH 1 | 1 | True | 89856 |
| PDSCH 1 | 2 | True | 89856 |
| PDSCH 1 | 3 | True | 89856 |
| PDSCH 1 | 4 | True | 89856 |
| PDSCH 1 | 5 | True | 89856 |
| PDSCH 1 | 6 | True | 89856 |
| PDSCH 1 | 10 | True | 89856 |
| PDSCH 1 | 11 | True | 89856 |
| PDSCH 1 | 12 | True | 89856 |
| PDSCH 1 | 13 | True | 89856 |
| PDSCH 1 | 14 | True | 89856 |
| PDSCH 1 | 15 | True | 89856 |
| PDSCH 1 | 16 | True | 89856 |
| PDSCH 4 | 7 | True | 38016 |
| PDSCH 4 | 17 | True | 38016 |
| PDCCH 1 | 0 | True | 108 |
| PDCCH 1 | 1 | True | 108 |
| PDCCH 1 | 2 | True | 108 |
| PDCCH 1 | 3 | True | 108 |
| PDCCH 1 | 4 | True | 108 |
| PDCCH 1 | 5 | True | 108 |
| PDCCH 1 | 6 | True | 108 |
| PDCCH 1 | 7 | True | 108 |
| PDCCH 1 | 10 | True | 108 |
| PDCCH 1 | 11 | True | 108 |
| PDCCH 1 | 12 | True | 108 |
| PDCCH 1 | 13 | True | 108 |
| PDCCH 1 | 14 | True | 108 |
| PDCCH 1 | 15 | True | 108 |
| PDCCH 1 | 16 | True | 108 |
| PDCCH 1 | 17 | True | 108 |

**CRC PASS : 32 || CRC FAIL : 0**

## 256_QAM_DL_64_QAM_UL_Comp_12_bit CH3 CRC Table

| Channel | Slot | CRC Passed | Bit Length |
|---|---|---|---|

**CRC PASS : 0 || CRC FAIL : 0**

ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Base_DL_UL\VXT_capture.png
ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Extended_DL_UL\VXT_capture.png
ScreenShot not append for C:\Automation\FH_Testing/Results/CUPLANE/LPRU_v2/1.0.19/22082142000036/FR1_100M/EAXCID3/16_QAM_Comp_14_bit_DL_UL/capture.png
ScreenShot not append for been

# Test Report UL

**Test purpose :**

The test purpose is to verify the UL test.

**Test environment :**

Normal test conditions.

| Test Case | Channel No | Channel Frequency [GHz] | BS Channel Bandwidth [MHz] | Measured EVM (RMS) [%] | EVM Limit [%] | Verdict |
|---|---|---|---|---|---|---|
| Base_DL_UL | 2 | 3.700005 | 100 | 1.744832992553711 | 3.5 | Fail |
| Extended_DL_UL | 2 | 3.700005 | 100 | 1.7345576286315918 | 3.5 | Pass |
| 16_QAM_Comp_14_bit_DL_UL | 3 | 3.54234 | FR1_100M | 1.632390022277832 | 3 | Pass |
| 256_QAM_DL_64_QAM_UL_Comp_12_bit | 3 | 3.54234 | FR1_100M | 1.6181265115737915 | 3 | Pass |

# Base_DL_UL CH2 CRC Table

PUCCH Decoder : Off
PUSCH Decoder : On
PUSCH_0_IE : PUSCH Index=0, CarrierIndex=0, BWPIndex=0
PUSCH_F0_IE : Codeword=0, SlotIndex=08, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F1_IE : Codeword=0, SlotIndex=09, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F2_IE : Codeword=0, SlotIndex=18, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F3_IE : Codeword=0, SlotIndex=19, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_1_IE : PUSCH Index=1, CarrierIndex=0, BWPIndex=0
PUSCH_F4_IE : Codeword=0, SlotIndex=07, RV Index=0, EffectiveCodeRate=0.6776, CRC=Pass , Number Of Code Blocks: 1
PUSCH_F5_IE : Codeword=0, SlotIndex=17, RV Index=0, EffectiveCodeRate=0.6776, CRC=Pass , Number Of Code Blocks: 1

## CRC PASS : 6 || CRC FAIL : 0

# Extended_DL_UL CH2 CRC Table

PUCCH Decoder : Off
PUSCH Decoder : On
PUSCH_0_IE : PUSCH Index=0, CarrierIndex=0, BWPIndex=0
PUSCH_F0_IE : Codeword=0, SlotIndex=08, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F1_IE : Codeword=0, SlotIndex=09, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F2_IE : Codeword=0, SlotIndex=18, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F3_IE : Codeword=0, SlotIndex=19, RV Index=0, EffectiveCodeRate=0.6616, CRC=Pass , Number Of Code Blocks: 2
PUSCH_1_IE : PUSCH Index=1, CarrierIndex=0, BWPIndex=0
PUSCH_F4_IE : Codeword=0, SlotIndex=07, RV Index=0, EffectiveCodeRate=0.6776, CRC=Pass , Number Of Code Blocks: 1
PUSCH_F5_IE : Codeword=0, SlotIndex=17, RV Index=0, EffectiveCodeRate=0.6776, CRC=Pass , Number Of Code Blocks: 1

## CRC PASS : 6 || CRC FAIL : 0

# 16_QAM_Comp_14_bit_DL_UL CH3 CRC Table

PUCCH Decoder : Off
PUSCH Decoder : On
PUSCH_0_IE : PUSCH Index=0, CarrierIndex=0, BWPIndex=0
PUSCH_F0_IE : Codeword=0, SlotIndex=08, RV Index=0, EffectiveCodeRate=0.6448, CRC=Pass , Number Of Code Blocks: 3
PUSCH_F1_IE : Codeword=0, SlotIndex=09, RV Index=0, EffectiveCodeRate=0.6448, CRC=Pass , Number Of Code Blocks: 3
PUSCH_F2_IE : Codeword=0, SlotIndex=18, RV Index=0, EffectiveCodeRate=0.6448, CRC=Pass , Number Of Code Blocks: 3
PUSCH_F3_IE : Codeword=0, SlotIndex=19, RV Index=0, EffectiveCodeRate=0.6448, CRC=Pass , Number Of Code Blocks: 3
PUSCH_1_IE : PUSCH Index=1, CarrierIndex=0, BWPIndex=0
PUSCH_F4_IE : Codeword=0, SlotIndex=07, RV Index=0, EffectiveCodeRate=0.6481, CRC=Pass , Number Of Code Blocks: 1
PUSCH_F5_IE : Codeword=0, SlotIndex=17, RV Index=0, EffectiveCodeRate=0.6481, CRC=Pass , Number Of Code Blocks: 1

## CRC PASS : 6 || CRC FAIL : 0

# 256_QAM_DL_64_QAM_UL_Comp_12_bit CH3 CRC Table

PUCCH Decoder : Off
PUSCH Decoder : On
PUSCH_0_IE : PUSCH Index=0, CarrierIndex=0, BWPIndex=0
PUSCH_F0_IE : Codeword=0, SlotIndex=08, RV Index=0, EffectiveCodeRate=0.9231, CRC=Pass , Number Of Code Blocks: 6
PUSCH_F1_IE : Codeword=0, SlotIndex=09, RV Index=0, EffectiveCodeRate=0.9231, CRC=Pass , Number Of Code Blocks: 6
PUSCH_F2_IE : Codeword=0, SlotIndex=18, RV Index=0, EffectiveCodeRate=0.9231, CRC=Pass , Number Of Code Blocks: 6
PUSCH_F3_IE : Codeword=0, SlotIndex=19, RV Index=0, EffectiveCodeRate=0.9231, CRC=Pass , Number Of Code Blocks: 6
PUSCH_1_IE : PUSCH Index=1, CarrierIndex=0, BWPIndex=0
PUSCH_F4_IE : Codeword=0, SlotIndex=07, RV Index=0, EffectiveCodeRate=0.9325, CRC=Pass , Number Of Code Blocks: 2
PUSCH_F5_IE : Codeword=0, SlotIndex=17, RV Index=0, EffectiveCodeRate=0.9325, CRC=Pass , Number Of Code Blocks: 2

## CRC PASS : 6 || CRC FAIL : 0

ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Base_DL_UL/VSA_Screenshot_1.gif
ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Base_DL_UL/VSA_Screenshot_2.gif
ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Extended_DL_UL/VSA_Screenshot_1.gif
ScreenShot not append for C:\Automation\radi_bn28\ORAN-Automation\CUPLANE\Results\LPRUD_4T4R\2.0.7\EAXCID2\Extended_DL_UL/VSA_Screenshot_2.gif
ScreenShot not append for C:\Automation\FH_Testing/Results/CUPLANE/LPRU_v2/1.0.19/22082142000036/FR1_100M/EAXCID3/16_QAM_Comp_14_bit_DL_UL/VSA_Screenshot_1.gif
ScreenShot not append for C:\Automation\FH_Testing/Results/CUPLANE/LPRU_v2/1.0.19/22082142000036/FR1_100M/EAXCID3/16_QAM_Comp_14_bit_DL_UL/VSA_Screenshot_2.gif
ScreenShot not append for C:\Automation\FH_Testing/Results/CUPLANE/LPRU_v2/1.0.19/22082142000036/FR1_100M/EAXCID3/256_QAM_DL_64_QAM_UL_Comp_12_bit/VSA_Screenshot_1.gif
ScreenShot not append for C:\Automation\FH_Testing/Results/CUPLANE/LPRU_v2/1.0.19/22082142000036/FR1_100M/EAXCID3/256_QAM_DL_64_QAM_UL_Comp_12_bit/VSA_Screenshot_2.gif