S.E / com / Sem - III

Com. Org. & Architecnr.

59-p3-upq-Con No. File

Con. 5577–10. **(REVISED COURSE)** **GT–6237**

(3 Hours) **[Total Marks : 100**

Instructions :

- Q. 1 is compulsory.
- Attempt any four out of remaining Questions.

Q.1 A] Main memory has 3 pages and the processor requires pages from virtual memory in the following order.
2 3 2 1 5 2 4 5 3 2 5 2 show the implementation of FIFO, LRU, LFU. [10]
B] Explain SPARC Processor in detail. Draw and explain n bit windows architecture of SPARC processor. [10]

Q.2 A] Explain systolic processor with suitable examples . [10]
B] What is cache memory ? explain cache coherence strategies in single and multiprocessor systems . [10]

Q.3 A] Compare & contrast DMA, Programmed I/O . & interrupt driven I/O. [10]
B] What is RAID ? Explain different RAID levels in detail. [10]

Q.4 A] Explain different bus arbitration schemes with suitable diagrams . [10]
B] What is pipelining? Explain six stage instruction pipeline with suitable diagram [10]

Q.5 A] Explain with suitable example booth's algorithm. [10]
B] Explain microinstructions, micro operations , micro-program in detail. [10]

Q.6 A] Explain RISC and CISC architectures in detail. [10]
B] explain Flynn's classifications with suitable diagrams . also comment on design issues of pipeline architecture . [10]

Q.7 Write short notes on: ANY FOUR [20]

1. PCI Bus
2. Memory characteristics
3. Micro instruction sequencing and execution.
4. loop buffer
5. interleaved memory