TE/Com/SemVI/Rev
AMP

137 : 2ndhf10Bmk

Con. 5550-10. (REVISED COURSE) GT-7554

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** question.
(3) **Each** question having **20 marks**.

1. (a) Explain Intel's Net Burst Micro-architechture with neat schematic. **10**
(b) Explain the protection mechanism of X86 intel family microprocessor. **10**
(c) Explain how the Linear Pipelining Working. **10**

2. (a) Differentiate between real mode and protected mode of X86 family. **10**
(b) State and explain operating modes of X86 family of processor. Show the mode transition diagram highlighting important features. **10**
(c) Explain segment translation mechanism of X86 processor with flow chart. Also explain segment descriptor field. **10**

3. (a) Explain different stages of integer pipeline and floating point pipeline of Pentium processor. **10**
(b) Explain Cache organisation of Pentium. **10**
(c) Explain with block diagram how superscalar operation is carried out in pentium processor. **10**

4. (a) Write the features of Pentium IV processor. **10**
(b) Explain Itanium processor with respect to instruction format, core pipeline stages and the functionality. **10**
(c) Explain the architecture of Super SPARC microprocessor with the help of neat diagram. **10**

5. (a) Data type supported by SPARC. **5**
(b) Register file of SPARC architecture. **5**
(c) Write short note on Ultra SPARC Processor. **5**
(d) Branch Prediction Logic. **5**

6. (a) Explain EFAG bits of pentium. **10**
(b) Explain the state transition diagram for pentium processor bus cycle. **10**
(c) Differentiated RISC and CISC. **10**

7. Write short notes on following :—
(a) IDE **5**
(b) VESA **5**
(c) EISA **5**
(d) USB. **5**