```
pixel_1 [7:0]
p clk
                                pixel_2 [7:0]
p_resetn
                                pixel_3 [7:0]
address_in_valid
                                pixel_4 [7:0]
dx_in
                                     dx_out
dy_in
                                     dy_out
Χ
                              pixel_out_valid
                                     irq_out
                             go_incremental
p_wb_CYC_I
                                   tile_ready
p_wb_STB_I
p_wb_LOCK_I
                         p_wb_DAT_O [31:0]
p_wb_SEL_I [3:0]
                                p_wb_RTY_O
p_wb_WE_I
                                p_wb_ACK_O
p_wb_ADR_I [31:0]
                                p_wb_ERR_O
p_wb_DAT_I [31:0]
                                p_wb_CYC_O
                                p_wb_STB_O
p_wb_DAT_I [31:0]
                               p_wb_LOCK_O
p_wb_RTY_I
                           p_wb_SEL_O [3:0]
p_wb_ACK_I
                                 p_wb_WE_O
p_wb_ERR_I
                         p_wb_ADR_O [31:0]
                          p_wb_DAT_O [31:0]
```

Coprocessor Buffer Management