```
p_clk
                                          irq
p_resetn
                       module register [31:0]
raise_irq
                                   initialized
                                     Written
p_wb_CYC_I
p_wb_STB_I
p_wb_LOCK_I
                          p_wb_DAT_O [31:0]
p_wb_SEL_I [3:0]
                                p_wb_RTY_O
p_wb_WE_I
                                p_wb_ACK_O
p_wb_ADR_I [31:0]
                                p_wb_ERR_O
p wb DAT I [31:0]
```

## Slave reg module