```
dx
p_clk
                                          Χ
p_resetn
                                         dy
enable
                                      valid
start
                                   finished
p_wb_CYC_I
p_wb_STB_I
                         p_wb_DAT_O [31:0]
p_wb_LOCK_I
                               p_wb_RTY_O
p_wb_SEL_I [3:0]
                               p_wb_ACK_O
p_wb_WE_I
                               p_wb_ERR_O
p_wb_ADR_I [31:0]
p_wb_DAT_I [31:0]
                               p_wb_CYC_O
                               p_wb_STB_O
p_wb_DAT_I [31:0]
                              p_wb_LOCK_O
p_wb_RTY_I
                           p_wb_SEL_O [3:0]
p_wb_ACK_I
                                p_wb_WE_O
p_wb_ERR_I
                         p_wb_ADR_O [31:0]
                         p_wb_DAT_O [31:0]
```

Coprocessor incremental module