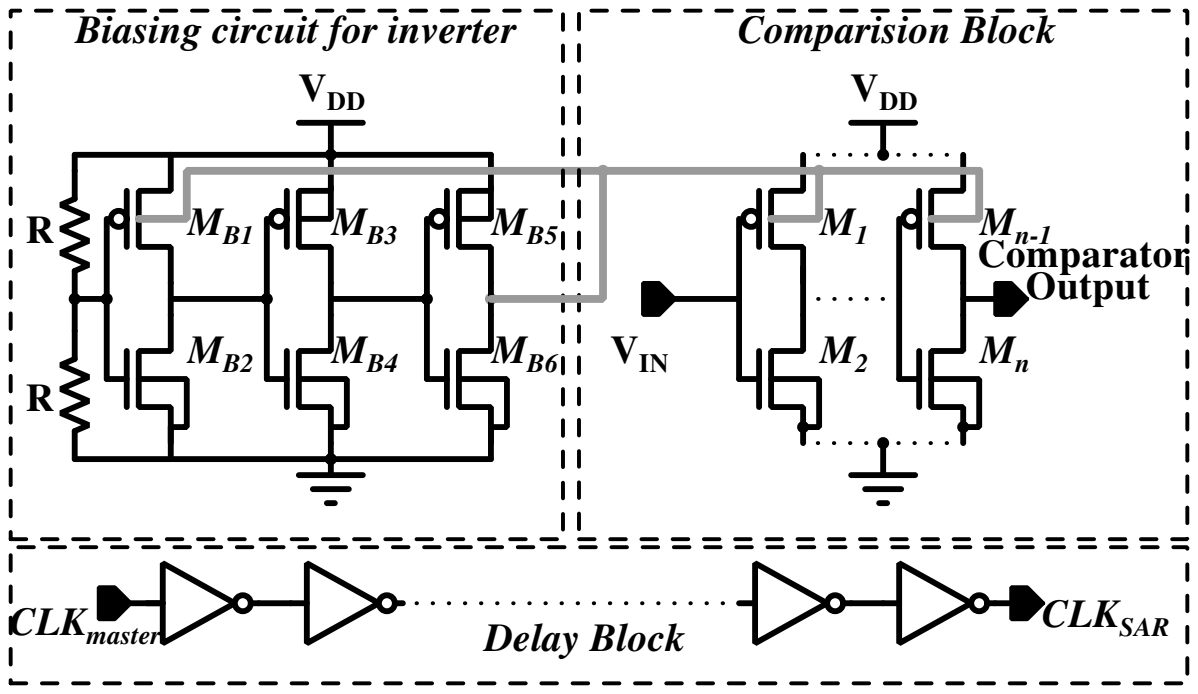
Biasing circuit for inverter
Comparision Block
V_DD
V_DD
R
R
M_B1
M_B2
M_B3
M_B4
M_B5
M_B6
M_1
M_2
M_n-1
M_n
V_IN
Comparator Output
CLK_master
Delay Block
CLK_SAR