

**WRITE THESIS TITLE ONLY IN CAPITAL**

**MAJOR TECHNICAL PROJECT (DP 401P)**

*to be submitted by*

**YOUR NAME IN CAPITAL LETTERS ONLY**

*for the partial fulfilment of the degree*

*of*

**BACHELOR OF TECHNOLOGY IN  
ELECTRICAL ENGINEERING**

*under the supervision of*

**GUIDE NAME**



**SCHOOL OF COMPUTING AND ELECTRICAL ENGINEERING**

**INDIAN INSTITUTE OF TECHNOLOGY MANDI**

**KAMAND-175005, INDIA**

**JUNE, 2019**







*Dedicated*

*To*

*WHOM YOU WANT TO DEDICATE*



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I hereby declare that the entire work embodied in this thesis is the result of investigations carried out by me in the School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, under the supervision of GUIDE NAME, and that it has not been submitted elsewhere for any degree or diploma. In keeping with the general practice, due acknowledgments have been made wherever the work described is based on finding of other investigators.

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# Acknowledgements

**Your name**



# ABSTRACT

Write an abstract here. **Keywords:** *Add only IEEE keyword.*





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# Abbreviations

SAR	- Successive approximation register
ADC	- Analog-to-digital converter
DAC	- Digital-to-analog converter
T-to-B	- Thermometric code to Binary code
ENOB	- Effective number of bits
SNR	- Signal-to-noise ratio
SNDR	- Signal-to-noise-and-distortion ratio
DR	- Dynamic range
SFDR	- Spurious free dynamic range
s.t.	- such that



# Chapter 1

## Introduction

### 1.1 Background and Literature Survey

??

### 1.2 Thesis Organisation

This work is organised in 7 chapters.

- Chapter 1 introduces the topic, providing a brief overview of available ADC architectures. Further, the chapter discusses the objective and scope of the work presented in the thesis.
- Chapter ?? provides a brief about the conventional architectures of flash and SAR ADCs. Then this chapter further elaborates similarities and differences between the conventional architectures and the flash-SAR hybrid ADC architecture.
- Chapter ?? discusses various CDAC topologies. This chapter also elaborates on the type of the ‘switches’, an integral part of the DAC design. Further, the implementation of the CDAC is elaborated in this chapter.
- Chapter ?? provides a comparison of the static and dynamic comparator architectures. A glimpse is given about the inverter based comparators and how they can replace the conventional comparators in the flash and SAR ADCs.



- Chapter ?? discusses the digital logic and control circuitry for the flash-SAR ADC. It discusses various topologies and their advantages and disadvantages. Further, it describes the logic used in this work.
- Chapter ?? discusses the simulation results for the ADC.
- Chapter ?? concludes the work and discusses future scope of the work.
- References are given in the bibliography.





## **Chapter 2**

# **CHAPTER NAME**

### **2.1 Introduction**





# **Chapter 3**

## **chapter name**

### **3.1 The Digital-to-Analog converter**

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# Chapter 4

## Chapter name

### 4.1 ....

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# Chapter 5

## Chapter name

### 5.1 ....

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# Chapter 6

## Chapter name

### 6.1 ....

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# **Chapter 7**

## **Chapter name**

### **7.1 ....**

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