Vaibhav Ambastha

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Technical Skills

Languages: Java | C++ | C | SQL | Scala | ARM Assembly | Verilog | Python | HTML/CSS | JavaScript
Developer Tools: VS Code | IntelliJ IDEA | ModelSim | Quartus | Jenkins | DBeaver | Apache Zeppelin
Technologies/Frameworks: Linux | GitHub | JUnit | FPGA | MongoDB | ROS | Apache Hive | Apache Hadoop

Education

University of British Columbia **Expected Graduation: May 2026**
Bachelor of Applied Science in Computer Engineering – Third Year Student *Vancouver, BC*
CGPA: 3.70/4.33, Dean's Honour List 2023
Relevant Coursework: Data Structures & Algorithms | Object-Oriented Programming | Software Construction | Computer Architecture | Operating Systems | Digital Systems Design

Experience

UBC SailBot **January 2024 – Present**
Software Developer - Network Systems *Vancouver, BC*
- Implemented system in C++ to transmit global coordinates to autonomous boat using Iridium satellite network and the Rockblock remote server
- Integrated serialized Google Protobuf strings into ROS messages, enabling real-time updates for boat's navigation
- Developed backend API using REST principles and HTTP methods to process JSON coordinate data from the land server, serialize it, and send it to Rockblock servers using libcurl
- Conducted rigorous testing by creating a virtual Rockblock server, validating successful transmission and database storage in MongoDB of boat data to showcase on website, providing users access to oceanic collected data

Insurance Corporation of British Columbia **May 2024 – August 2024**
Data Engineer Co-op *Vancouver, BC*
- Designed and deployed ETL pipelines using Scala and Apache Spark to process large datasets for business intelligence, collaborating with cross-functional teams under the Agile Scrum framework to maintain high data quality standards
- Leveraged SQL to execute complex data queries and transformations within Apache Hive supporting the decommissioning of Enterprise Data Warehouse (EDW) to Big Data Management (BDM)
- Optimized data storage solutions with Apache Hadoop to enhance database performance and ETL pipeline efficiency
- Integrated Jenkins for continuous integration and automation of ETL pipeline testing and rapid deployment

Technical Projects

Fullstack Web-Based Chat Application | *JavaScript, HTML/CSS, Node.js, WebSockets, MongoDB* **October 2024**
- Built a responsive GUI with HTML/CSS and JavaScript, structuring app with client-side routing and MVC architecture
- Developed real-time chat functionality using WebSockets and AJAX for client-server data exchange, powered by Node.js
- Integrated MongoDB for data persistence and created RESTful API endpoints in Node.js for CRUD operations
- Added basic authentication, session management, and XSS defenses for secure, user-friendly access

Premier League Prediction Model | *Python, Pandas, Scikit-Learn, BeautifulSoup* **January 2024**
- Web scraped football data using Python with requests, BeautifulSoup, and Pandas libraries for DataFrame analysis
- Applied Random Forest algorithm from machine learning library scikit-learn to forecast match outcomes based on ranging conditions resulting in a 55.4% accuracy score based on training data
- Tested machine learning method against rolling average statistical method to validate robustness of model

IoT Data Analytics Client Handling Server | *Java, JUnit, Socket Programming, AWS Lambda* **December 2023**
- Developed Java program to simulate an IoT analytics sever which received sensor data and provided 16 various services to clients such as notifications, aggregation, and predictive modeling, achieving 90%+ test coverage using JUnit
- Handled concurrent clients through efficient implementation of server socket programming while ensuring QoS
- Launched AWS Lambda to strengthen server networks, optimize event handling, and develop predictive services

RISC Machine | *Verilog, ARM Assembly, ModelSim, Quartus, FPGA* **November 2023**
- Assembled a RISC Machine utilizing Verilog HDL to maximize performance on the five-stage pipelined processor
- Implemented a range of instructions to optimize instruction executions through the processor and generated exhaustive Verilog RTL and post-synthesis testbenches to test architecture on ModelSim
- Improved CPU to process ARMv7 instructions such as LDR, ADD, CMP within 15 cycles and presented on FPGA

Interests & Languages

Interests: Football (Barcelona Fan) | Journal Writing | Swimming | Sunset Watching | Formula One
Languages: Native English Speaker | Proficient Hindi Speaker | Proficient French Speaker