EEN - 611 FPGA Implementation of Signal Processing Systems

Tutorial-1: Verilog structural modelling

1) Write a verilog code for the logic gates AND, OR, NOT, NAND, NOR, XOR, XNOR and verify with test bench.
2) Design a half adder and verify the performance through verilog code.
3) Design a 1-bit full adder and verify the performance through verilog code.
4) Develop a 1-bit full adder verilog module using the half adder verilog modules.
5) Design and develop a 4-bit ripple carry adder verilog module using the 1-bit full adder modules.
6) Design a 4-bit prime number detector and write a verilog structural module.
7) Design and verify the 4×1 multiplexer function through verilog structural module.
8) Design a 3×8 line decoder and verify the performance through verilog.
9) Design a 4×1 multiplexer with tristate buffers and verify the performance through verilog.
10) Design a full- subtractor with half subtractor verilog modules.