

P37) Implement a variable-width barrel shifter in Verilog. Design a module that accepts a 6-bit input (A), a 3-bit shift amount (Shift), and a control signal (Direction). If Direction is 0, the shifter should perform a left shift; if it's 1, it should perform a right shift. Generate a 6-bit output (Result) accordingly.

Logic Used

A simple for loop was used. In every iteration of the loop, the MSB/LSB was checked depending upon whether it was a left/right shift. If it was a 1, the shifted result was ORed with 000001/100000 accordingly. If it was 0, the shifted result was left as it is. At the end of the for loop, appropriately barrel shifted result is available to us.

Source Code

```
`timescale 1ns / 1ps

module barrelshifter(input wire [5:0] A,          // 6-bit input
    input wire [2:0] Shift,          // 3-bit shift amount
    input wire Direction,          // Control signal for direction (0 for left, 1 for right)
    output wire [5:0] Result        // 6-bit output
);
    reg [5:0] shifted_result;
    integer i;
    always @(*) begin
        shifted_result=A;
        if (Direction == 0) begin
            for (i=0;i<Shift;i=i+1) begin
                if (shifted_result[5]==0) begin
                    shifted_result = (shifted_result << 1);
                end
                else begin
                    shifted_result = (shifted_result << 1) | (6'b000001);
                end
            end
        end
        else begin
            for (i=0;i<Shift;i=i+1) begin
                if (shifted_result[0]==0) begin
                    shifted_result = (shifted_result >> 1);
                end
                else begin
                    shifted_result = (shifted_result >> 1) | (6'b100000);
                end
            end
        end
    end
end
```

```
    assign Result = shifted_result;
endmodule
```

Testbench

```
'timescale 1ns / 1ps
module barrelshifter_tb(

    );
reg [5:0] a;
reg [2:0] b;
reg c;
wire [5:0] d;

barrelshifter dut (a,b,c,d);

initial begin
a=6'b011110; b=3'b011; c=1;
#10;
a=6'b100111; b=3'b010; c=0;
#10;
a=6'b111000; b=3'b111; c=1;
#10;
a=6'b010100; b=3'b110; c=0;
#10;
a=6'b110110; b=3'b100; c=1;
end
endmodule
```

Results

