EE5311 - Assignment 4

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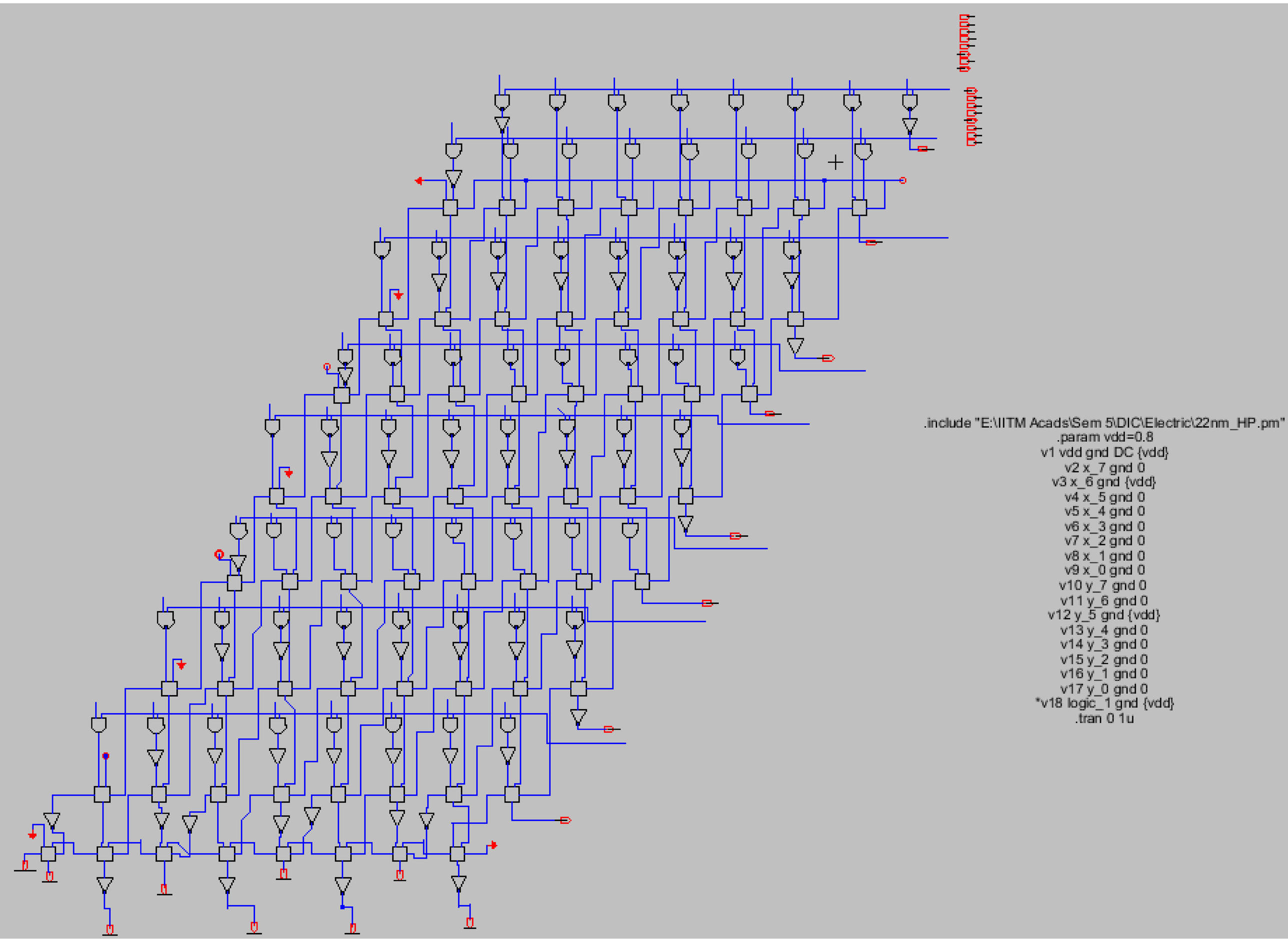
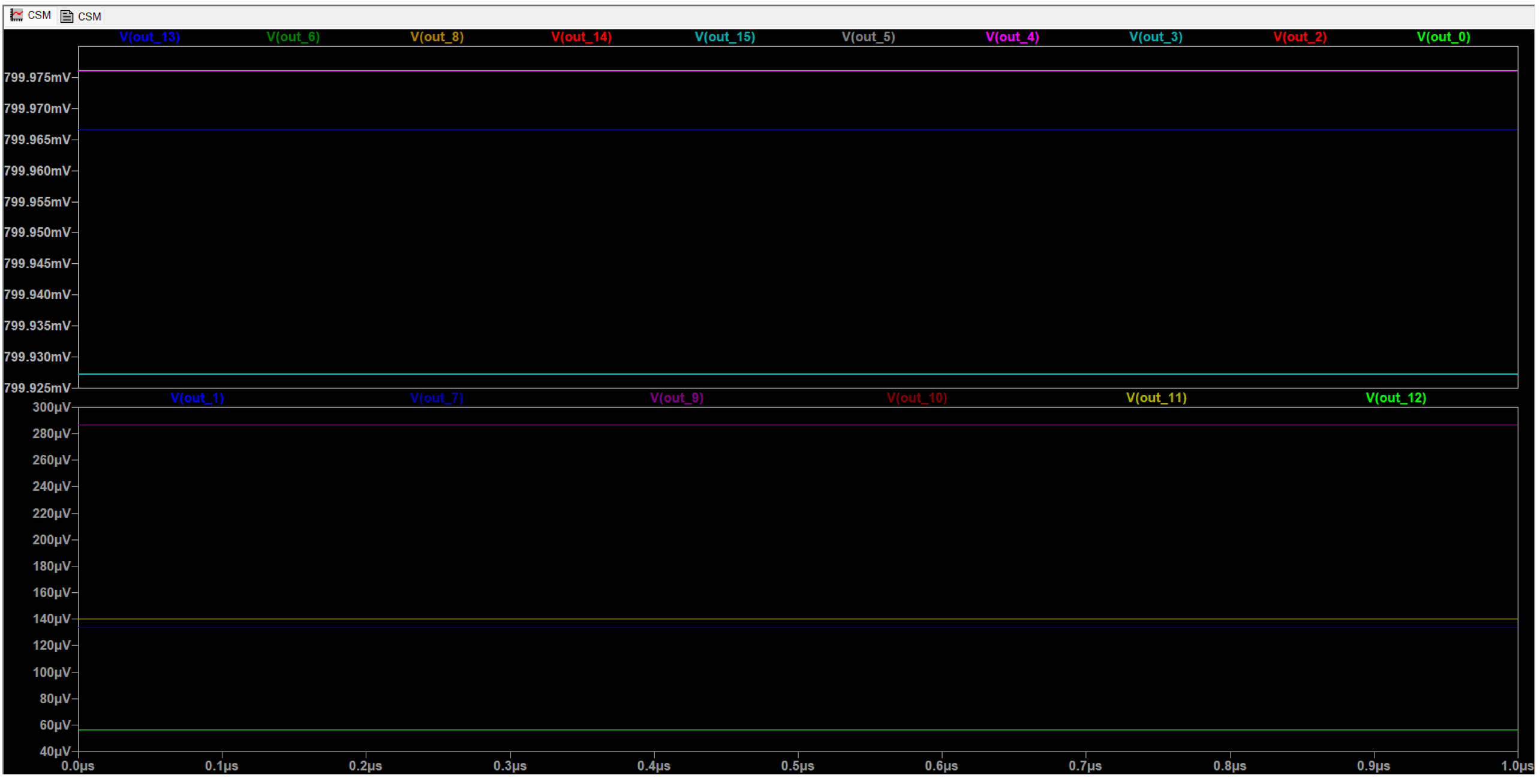
8-bit Carry Save Multiplier

Schematic

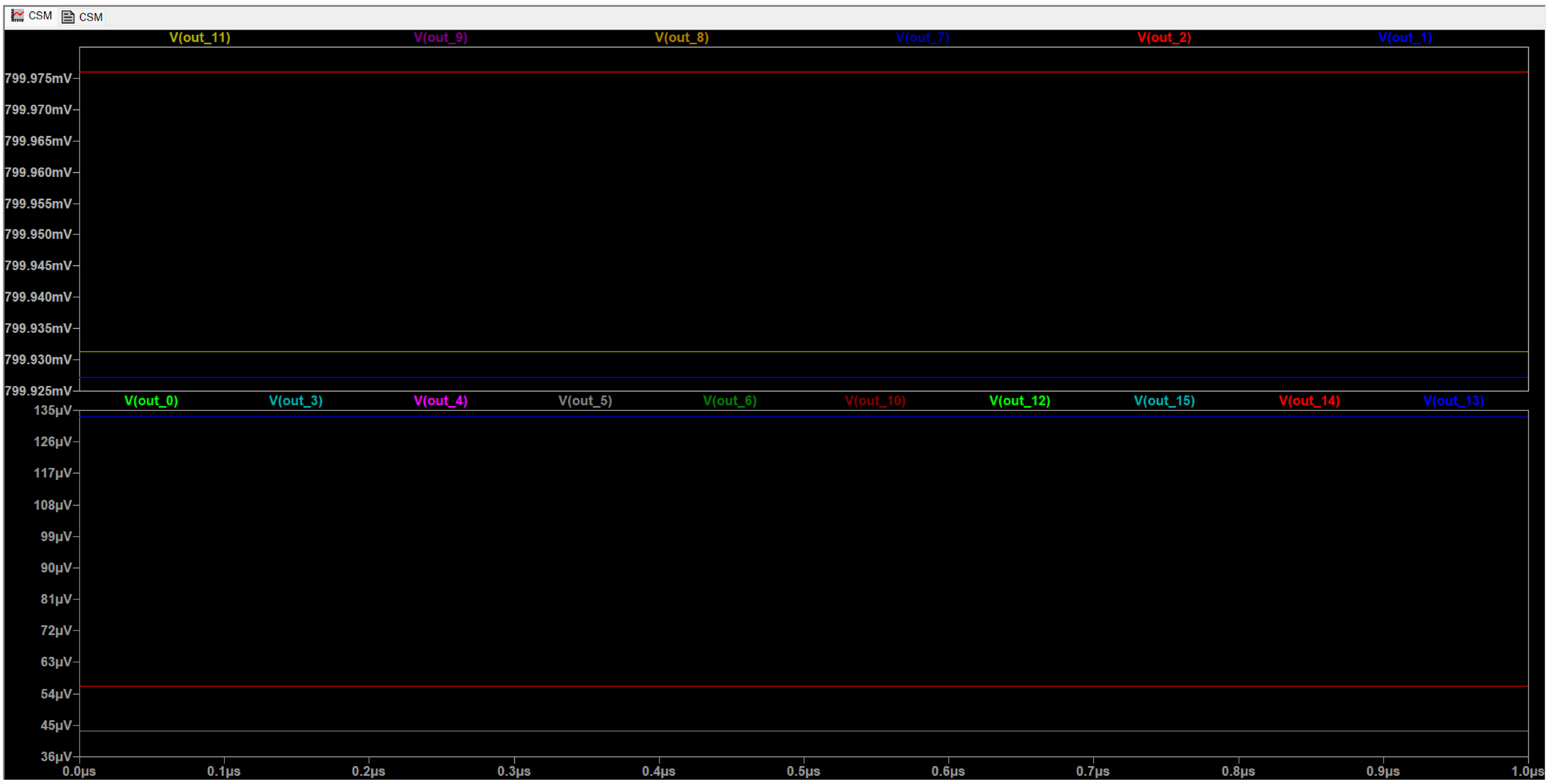


Simulation to show functionality of schematic

X=8'b10110111 Y=8'b01101011 OUT=16'b1110000101111101

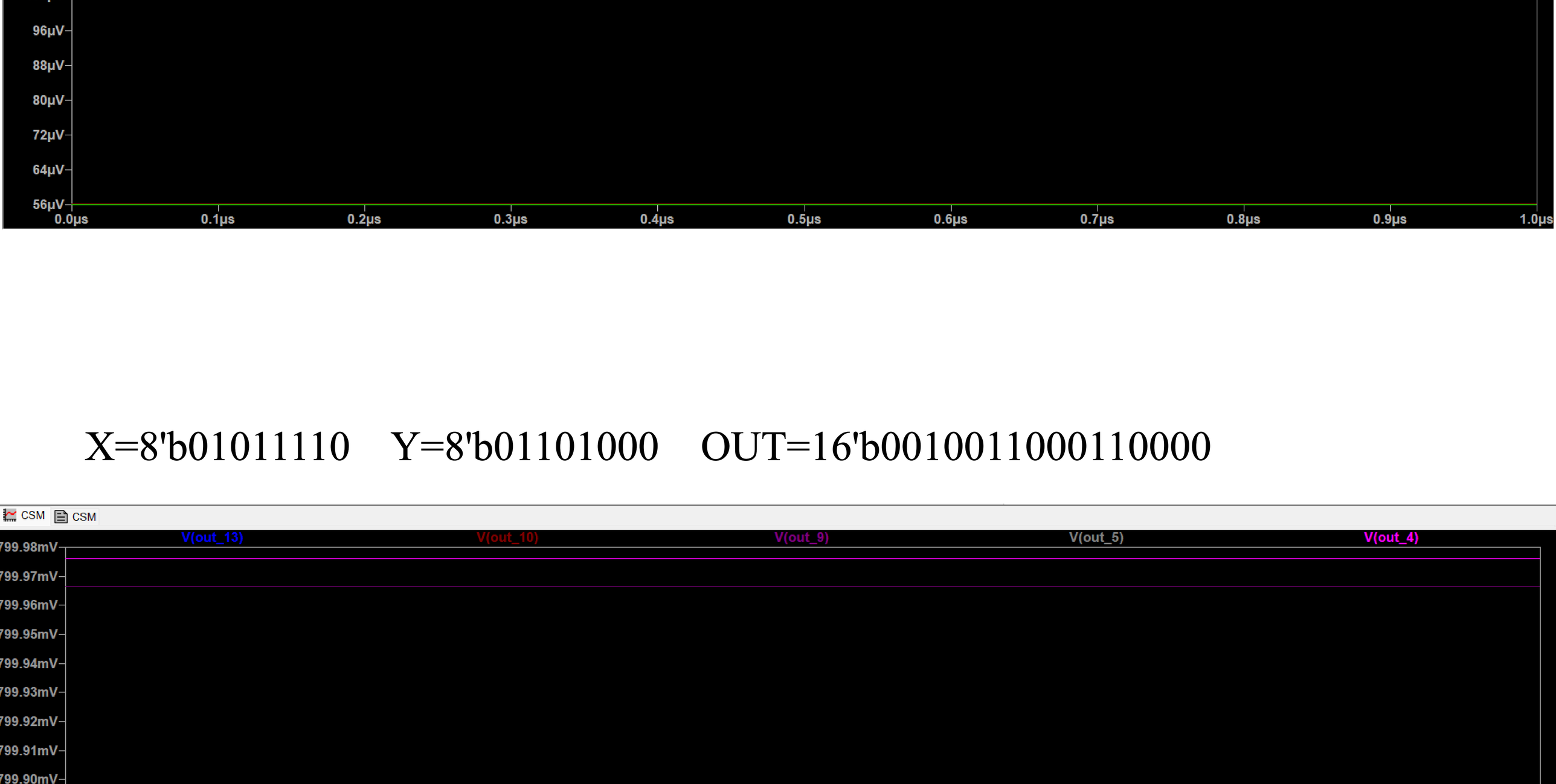


X=8'b10001010 Y=8'b11100111 OUT=16'b0000101110000110



X=8'b00111111 Y=8'b11101010 OUT=16'b1111101010010110

X=8'b01011110 Y=8'b01101000 OUT=16'b0010011000110000



Justification for choice of CARRY and SUM sizes

Sum and Carry-out Delays : A toggled; B, Ci fixed

Inputs			Sum' Rise and Fall delays for CxSx sizes										
A-Toggle	B	Ci	11	12	13	21	22	23	31	32	33		
R	0	0	1.94E-11	1.39E-11	1.26E-11	1.60E-11	1.41E-11	1.26E-01	1.99E-11	1.44E-11	1.29E-11		
F	0	0	1.77E-11	2.27E-11	2.77E-11	1.80E-11	2.31E-11	2.82E-11	1.82E-11	2.35E-11	2.86E-11		
R	0	1	2.29E-11	2.31E-11	2.51E-11	2.02E-11	1.95E-11	2.02E-11	1.94E-11	1.83E-11	1.87E-11		
F	0	1	2.26E-11	2.35E-11	2.60E-11	2.77E-11	2.84E-11	3.08E-11	3.25E-11	3.32E-11	3.55E-11		
R	1	0	2.48E-11	2.59E-11	2.82E-11	3.32E-11	3.42E-11	3.63E-11	4.15E-11	4.21E-11	4.42E-11		
F	1	0	2.83E-11	2.71E-11	2.87E-11	2.57E-11	2.35E-11	2.41E-11	2.50E-11	2.25E-11	2.27E-11		
R	1	1	1.76E-11	2.69E-11	3.59E-11	1.78E-11	2.72E-11	3.61E-11	1.80E-11	2.74E-11	3.63E-11		
F	1	1	1.64E-11	1.38E-11	1.34E-11	1.67E-11	1.40E-11	1.35E-11	1.71E-11	1.43E-11	1.36E-11		
		Max Rise Delay	2.48E-11	2.69E-11	3.59E-11	3.32E-11	3.42E-11	1.26E-01	4.15E-11	4.21E-11	4.42E-11	Min Rise Delay	2.48E-11
		Max Fall Delay	2.83E-11	2.71E-11	2.87E-11	2.77E-11	2.84E-11	3.08E-11	3.25E-11	3.32E-11	3.55E-11	Min Fall Delay	2.71E-11
		Max Delay	2.83E-11	2.71E-11	3.59E-11	3.32E-11	3.42E-11	1.26E-01	4.15E-11	4.21E-11	4.42E-11	Min Delay	2.71E-11

	Carry out' Delays for CxSx Sizes										
	11	12	13	21	22	23	31	32	33		
	1.27E-11	1.48E-11	1.72E-11	1.08E-11	1.22E-11	1.35E-11	1.03E-11	1.13E-11	1.23E-11		
	1.19E-11	1.44E-11	1.70E-11	1.62E-11	1.87E-11	2.13E-11	2.03E-11	2.29E-11	2.55E-11		
	1.56E-11	1.82E-11	2.07E-11	2.30E-11	2.56E-11	2.82E-11	3.04E-11	3.30E-11	3.57E-11		
	1.33E-11	1.55E-11	1.79E-11	1.20E-11	1.33E-11	1.48E-11	1.18E-11	1.29E-11	1.39E-11		
Max Rise Delay	1.56E-11	1.82E-11	2.07E-11	2.30E-11	2.56E-11	2.82E-11	3.04E-11	3.30E-11	3.57E-11	Min Rise Delay	1.56E-11
Max Fall Delay	1.33E-11	1.55E-11	1.79E-11	1.62E-11	1.87E-11	2.13E-11	2.03E-11	2.29E-11	2.55E-11	Min Fall Delay	1.33E-11
Max Delay	1.45E-11	1.69E-11	1.93E-11	1.96E-11	2.22E-11	2.47E-11	2.54E-11	2.80E-11	3.06E-11	Min Delay	1.45E-11

Sum and Carry-out Delays : B toggled; A, Ci fixed

Inputs			Sum' Rise and Fall delays for CxSx sizes										
A	B-Toggle	Ci	11	12	13	21	22	23	31	32	33		
0	R	0	1.68E-11	1.30E-11	1.19E-11	1.20E-11	1.31E-11	1.20E-11	1.74E-11	1.34E-11	1.23E-11		
0	F	0	1.62E-11	2.14E-11	2.65E-11	1.65E-11	2.18E-11	2.69E-11	1.69E-11	2.22E-11	2.75E-11		
0	R	1	2.66E-11	2.66E-11	2.85E-11	2.21E-11	2.12E-11	2.20E-11	2.07E-11	1.95E-11	1.99E-11		
0	F	1	2.44E-11	2.56E-11	2.79E-11	2.95E-11	3.06E-11	3.30E-11	3.46E-11	3.54E-11	3.77E-11		
1	R	0	2.47E-11	2.59E-11	2.81E-11	3.32E-11	3.42E-11	3.64E-11	4.15E-11	4.22E-11	4.43E-11		
1	F	0	2.79E-11	2.84E-11	3.06E-11	2.42E-11	2.37E-11	2.48E-11	2.33E-11	2.23E-11	2.30E-11		
1	R	1	1.76E-11	2.72E-11	3.64E-11	1.79E-11	2.75E-11	3.67E-11	1.82E-11	2.78E-11	3.70E-11		
1	F	1	1.52E-11	1.33E-11	1.30E-11	1.56E-11	1.34E-11	1.31E-11	1.59E-11	1.37E-11	1.33E-11		
		Max Rise Delay	2.66E-11	2.72E-11	3.64E-11	3.32E-11	3.42E-11	3.67E-11	4.15E-11	4.22E-11	4.43E-11	Min Rise Delay	2.66E-11
		Max Fall Delay	2.79E-11	2.84E-11	3.06E-11	2.95E-11	3.06E-11	3.30E-11	3.46E-11	3.54E-11	3.77E-11	Min Fall Delay	2.79E-11
		Max Delay	2.79E-11	2.84E-11	3.64E-11	3.32E-11	3.42E-11	3.67E-11	4.15E-11	4.22E-11	4.43E-11	Min Delay	2.79E-11

	Carry out' Delays for CxSx Sizes										
	11	12	13	21	22	23	31	32	33		
	1.52E-11	1.76E-11	2.00E-11	1.21E-11	1.34E-11	1.49E-11	1.12E-11	1.22E-11	1.33E-11		
	1.42E-11	1.66E-11	1.92E-11	1.84E-11	2.09E-11	2.35E-11	2.26E-11	2.52E-11	2.78E-11		
	1.58E-11	1.83E-11	2.08E-11	2.32E-11	2.58E-11	2.83E-11	3.07E-11	3.33E-11	3.59E-11		
	1.47E-11	1.72E-11	1.97E-11	1.27E-11	1.43E-11	1.57E-11	**1.23E-11**	1.35E-11	1.46E-11		
Max Rise Delay	1.58E-11	1.83E-11	2.08E-11	2.32E-11	2.58E-11	2.83E-11	3.07E-11	3.33E-11	3.59E-11	Min Rise Delay	1.58E-11
Max Fall Delay	1.47E-11	1.72E-11	1.97E-11	1.84E-11	2.09E-11	2.35E-11	2.26E-11	2.52E-11	2.78E-11	Min Fall Delay	1.47E-11
Max Delay	1.53E-11	1.77E-11	2.02E-11	2.08E-11	2.33E-11	2.59E-11	2.66E-11	2.92E-11	3.18E-11	Min Delay	1.53E-11

Sum and Carry-out Delays : Ci toggled; A, B fixed

Inputs			Sum' Rise and Fall delays for CxSx sizes										
A	B	Ci-Toggle	11	12	13	21	22	23	31	32	33		
0	0	R	1.33E-11	1.13E-11	1.08E-11	1.35E-11	1.13E-11	1.08E-11	1.36E-11	1.15E-11	1.10E-11		
0	0	F	1.15E-11	1.62E-11	2.11E-11	1.17E-11	1.65E-11	2.14E-11	1.19E-11	1.68E-11	2.17E-11		
0	1	R	2.31E-11	2.43E-11	2.63E-11	1.85E-11	1.88E-11	1.99E-11	1.69E-11	1.69E-11	1.78E-11		
0	1	F	1.97E-11	2.25E-11	2.50E-11	1.60E-11	1.77E-11	1.92E-11	1.49E-11	1.60E-11	1.71E-11		
1	0	R	2.06E-11	2.13E-11	2.32E-11	1.77E-11	1.75E-11	1.85E-11	1.67E-11	1.61E-11	1.68E-11		
1	0	F	1.82E-11	2.18E-11	2.52E-11	1.51E-11	1.67E-11	1.86E-11	1.43E-11	1.52E-11	1.65E-11		
1	1	R	1.58E-11	2.48E-11	3.39E-11	1.60E-11	2.50E-11	3.40E-11	1.62E-11	2.53E-11	3.42E-11		
1	1	F	1.26E-11	1.18E-11	1.20E-11	1.27E-11	1.19E-11	1.19E-11	1.29E-11	1.19E-11	1.20E-11		
		Max Rise Delay	2.31E-11	2.48E-11	3.39E-11	1.85E-11	2.50E-11	3.40E-11	1.69E-11	2.53E-11	3.42E-11	Min Rise Delay	1.69E-11
		Max Fall Delay	1.97E-11	2.25E-11	2.52E-11	1.60E-11	1.77E-11	2.14E-11	1.49E-11	1.68E-11	2.17E-11	Min Fall Delay	1.49E-11
		Max Delay	2.31E-11	2.48E-11	3.39E-11	1.85E-11	2.50E-11	3.40E-11	1.69E-11	2.53E-11	3.42E-11	Min Delay	1.69E-11
		Sizes:	128	160.5	198.5	168	200	237	175.5	208.5	246.5		

	Carry out' Delays for CxSx Sizes										
	11	12	13	21	22	23	31	32	33		
	1.31E-11	1.55E-11	1.79E-11	1.02E-11	1.15E-11	1.29E-11	9.18E-12	1.02E-11	1.13E-11		
	1.01E-11	1.25E-11	1.49E-11	8.17E-12	9.68E-12	1.10E-11	7.44E-12	8.59E-12	9.61E-12		
	1.08E-11	1.31E-11	1.54E-11	8.98E-12	1.03E-11	1.17E-11	8.30E-12	9.31E-12	1.03E-11		
	1.09E-11	1.35E-11	1.60E-11	8.56E-12	1.00E-11	1.16E-11	7.73E-12	8.82E-12	1.00E-11		
Max Rise Delay	1.31E-11	1.55E-11	1.79E-11	1.02E-11	1.15E-11	1.29E-11	9.18E-12	1.02E-11	1.13E-11	Min Rise Delay	9.18E-12
Max Fall Delay	1.09E-11	1.35E-11	1.60E-11	8.56E-12	1.00E-11	1.16E-11	7.73E-12	8.82E-12	1.00E-11	Min Fall Delay	7.73E-12
Max Delay	1.20E-11	1.45E-11	1.69E-11	9.40E-12	1.08E-11	1.23E-11	8.46E-12	9.50E-12	1.06E-11	Min Delay	8.46E-12

From the above tables, we can see that among the maximum Sum and Carry-Out delays, the least is achieved for a Carry 3x + Sum 1x configuration. This configuration also has the fourth least size among all the possible configurations. The (1x, 1x) configuration has a significantly smaller size than the (3x, 1x) configuration, but it has a higher delay.

The critical path delays for (3x, 1x) and (1x, 1x) were compared (while keeping the NAND-INV sizes fixed at (2x, 2x), which was justified later in the report), and this was the deciding factor.

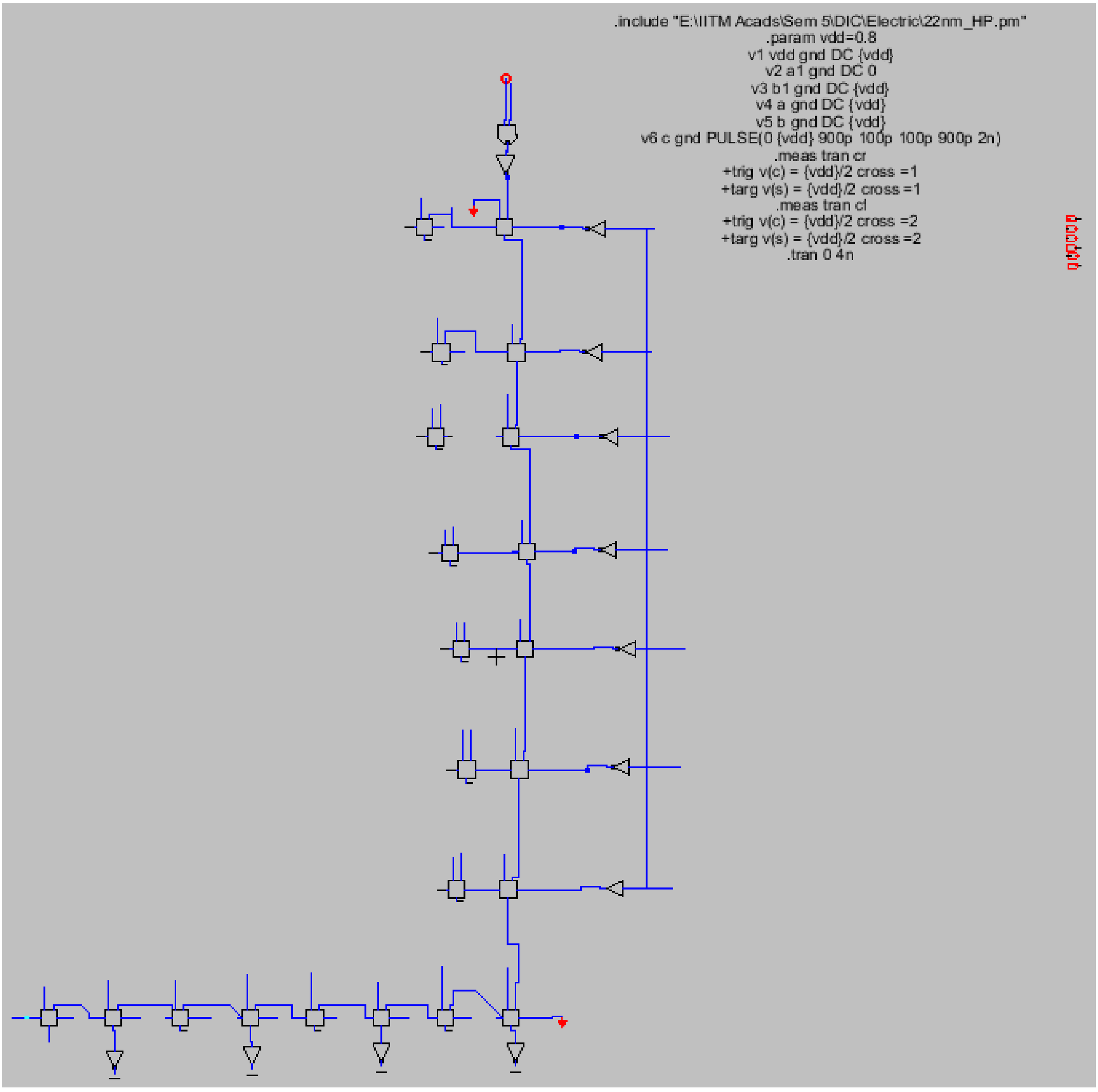
For NAND-INV configuration (2x, 2x)		
	(1x, 1x)	(3x, 1x)
Critical Path Rise	5.09E-10	4.01E-10
Critical Path Fall	4.98E-10	3.79E-10

There is a 26.9% increase in critical path delay with (1x, 1x) configuration. This conflicted with our 10% threshold (set by us). With the above calculations, we came to the conclusion that the delay must be prioritized over the area. Keeping this in mind, the final sizes chosen are:

CARRY 3x
SUM 1x

Justification for choice of NAND and INVERTER sizes

Analysis of the below critical path was done with 9 different configurations of NAND-INV sizes, and Rise and Fall delays were calculated. The results for the same are tabulated below.



	Rise and Fall Delay of Critical Path with C3S1 and INVxNANDx sizes									
	11	12	14	21	22	24	41	42	44	**Min Rise Delay**
Rise Delay	4.04E-10	4.02E-10	4.01E-10	3.99E-10	3.96E-10	3.94E-10	4.01E-10	3.95E-10	3.92E-10	3.92E-10
Fall Delay	3.86E-10	3.84E-10	3.83E-10	3.81E-10	3.77E-10	3.76E-10	3.82E-10	3.76E-10	3.73E-10	3.73E-10
Size	58	58	73.5	58	58	73.5	66	66	81.5	

The least delay was achieved for a NAND-INV configuration (4x, 4x). But, this configuration has a much larger size but only a slightly smaller delay when compared to the configuration (2x, 2x). There is only a 1% increase in delay when NAND-INV (2x, 2x) configuration is used. Keeping both delay and size constraints in mind, the final sizes chosen are:

NAND	**2x**
INV	**2x**

Note:
To make the schematic even more clear, we have interchanged the A and Ci inputs in our full adder, as the A input was being toggled. So to minimise the delay we made this change.