Vaibhav Krishna Garimella

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RESEARCH EXPERIENCE

Compute In-Memory Group **(Integrated Circuits and Systems Group, IIT Madras)**
Guide: Prof. Janakiraman Viraraghavan *June 2024 - Present*

Time-Domain Chip Tape-Out
- Designed the layout for the full SRAM array and peripherals like Sense Amp and Word Line Drivers and performed RC-extracted Monte Carlo simulations to verify functionality and compute read/write times.
- Designing a calibrated Voltage-to-Time Converter (VTC).
- Analyzed layer-wise statistics of various Neural Networks and tested inferences based on ADC-bit and MAC length limitations.

Current-Domain Chip Testing
- Ran neural network inferences on taped-out TSMC 28nm Current-Domain chip employing the Optimal Clipping Criterion.
- Corrected SAR-ADC comparator offset using the compute and reference columns to bring down output error below 1 LSB.

SHAKTI Processor **(Govt. of India Sponsored Project for Indigenous Microprocessors)**
Guide: Prof. Kamakoti Veezhinathan *Dec 2023 - June 2024*

Instruction Set Architecture Implementation and Testing
- Implemented Packed Single Instruction, Multiple Data (PSIMD) instructions on Shakti's C-class SOC in BlueSpec Verilog.
- Performed Area vs Speed calculations benchmarked against M-extension instructions using Synopsys Design Compiler to obtain optimized performance.
- Integrated the newly designed p-box module with the processor pipeline.

Team Avishkar Hyperloop **(Student Hyperloop Team, IIT Madras)**
Faculty Advisor: Prof. Satya Chakravarthy *Sept 2022 - Aug 2023*

Hyperloop Pod Electrical Systems Design and Testing
- Designed and tested a 4-layer PCB to run the inverter and collect pod-critical data from the Intelligent Power Module monitoring the inverter.
- Configured a Battery Management System (BMS) with self-designed high voltage battery packs, tested CAN communication and implemented fault states through the BMS based on safety limits.
- Assembled and tested battery packs with LFP cells (net configuration of 88s 4p, 300V nominal) by charging and discharging them while monitoring parameters like SoC, SoH, etc and logged data to observe passive cell balancing.

COURSE PROJECTS

Embedded Memory Design
Guide: Prof. Janakiraman Viraraghavan *Jan 2024 - June 2024*

Charge-Domain Compute In-Memory Engine Design `Project site`
- Designed a Charge-Domain based 9T-1C CIM engine to run inferences on the MNIST dataset with only a 0.8% accuracy drop from the software baseline.
- Performed Monte-Carlo simulations on the compute column and current-steering DAC and achieved 1.85 TOPS/W.

EDUCATION

Indian Institute of Technology Madras
BTech. in Engineering Physics
CGPA : 8.68/10

INTERESTS

In-Memory Computing
Approximate Computing
Machine Learning Hardware
Integrated Circuit Design

SKILLS

PROGRAMMING
C • Python • PyTorch • Verilog • BlueSpecVerilog • MATLAB

TOOLS/PLATFORMS
Cadence Virtuoso • Genus • Innovus • Advanced Design System (ADS) • Altium Designer • Vivado • Synopsys Design Compiler • LTSpice • Vivado HLS • Electric

COURSEWORK

GRADUATE
Embedded Memory Design
Digital IC Design
Analog IC Design
Neuromorphic Computing
Deep Learning for Imaging
Mapping DSP Algos. to Arch.

UNDERGRADUATE
Computer Organization
Machine Learning Techniques
Analog Circuits
Digital Signal Processing
Solid State Devices
Analog Systems
Digital Systems

ACHIEVEMENTS

JEE Advanced 2021
All India Rank 1013

KVPA SA Scholar
All India Rank 365

Devices for AI and Neuromorphic Computing

Guide: Prof. Bhaswar Chakrabarti *July 2024 - Present*

NVM-based Compute In-Memory Engine GitHub

- Designed two-layer RRAM crossbar arrays to enable efficient in-memory computation for alphabet classification tasks.
- Performed hardware-aware training to approximately binarize weights and achieve minimal loss in hardware inference accuracy.

Deep Learning for Imaging (KLA Project Challenge)

Guide: Prof. A N Rajagopalan *July 2024 - Nov 2024*

Defect Preserving Image Denoising (Winner of KLA Contest) GitHub

- Implemented a Residual Channel Attention Network model to denoise MVTec Anomaly Detection dataset images while keeping the object defect intact.
- Achieved a high PSNR of 29.63dB and SSIM of 0.9335 on the test dataset.

Digital IC Design

Guide: Prof. Janakiraman Viraraghavan *July 2023 - Dec 2023*

8-Bit Carry Save Multiplier Design

- Designed a transistor-level schematic and layout of an 8-bit Carry Save Multiplier on Electric with multi-level Carry Lookahead Adder for vector merge
- Designed a pipelined schematic using C2MOS Dynamic Flip Flops to achieve an 85% increase in operating clock frequency from 1.86MHz to 3.75MHz.

Analog IC Design

Guide: Prof. Nagendra Krishnapura *Jan 2024 - May 2024*

Fully Differential Inverting Amplifier Design

- Designed a fully differential inverting amplifier with a closed-loop DC gain of 15.54 dB and a 3dB-bandwidth of 16.04MHz.
- Implemented the fully differential opamp with two-stage common-mode feedback to achieve an open-loop DC gain of 70.29dB.

Analog Systems Lab

Guide: Prof. Sankaran Aniruddhan *Jan 2023 - May 2023*

LED driver + ClassD Amplifier GitHub

- Built a DC-DC switching regulator in a closed-loop control system, a Peak Detector to drive an LED and an sPWM generator to drive a speaker.
- Fine-tuned a narrow band-pass filter to a Quality Factor of 10 to allow the system to work at two select frequencies.

ACTIVITIES

Team Avishkar Hyperloop
Secured a Top 5 finish at the European Hyperloop Week 2023 at the University of Edinburgh, Scotland.

EE Research Club
Part of a 40 member research enthusiast student group actively organising seminars and talks.

Avanti Fellows
Mentored and guided class 11 & 12 students for competitive exams like JEE, KVPY and olympiads.

EXTRA-CURRICULAR

Chess
Member of the freshman NSO (National Student Organization) chess team.

Represented hostels Ganga and Brahmaputra in inter-hostel chess tournaments.

Music
Classically trained in Carnatic music vocals for over 13 years.