Vaibhav Krishna Garimella | IIT Madras

Project Experience

CURRENT-DOMAIN CHIP TESTING | Guide: Prof. Janakiraman Viraraghavan

May 2024 – Present | VLSI Group, IIT Madras

- Running neural network inferences on taped out TSMC **28nm Charge-Domain based compute in-memory macro** employing the **Optimal Clipping Criterion** to fit MAC (Multiply and Accumulate) values within the ADC range.
- Performing simulations to model and analyze **non-linearity** in **MAC generation** (current) during mean subtraction.

IN-MEMORY COMPUTE ENGINE | Embedded Memory Design

Jan 2024 – June 2024

- Designed a **Charge-Domain based 9T-1C SRAM cell** compute engine to run inferences on the MNIST dataset
- Performed **Monte-Carlo** simulations on the compute column and current-steering DAC and appropriate transistor size scaling was done to preserve ADC bit precision

SHAKTI PROCESSOR | Hardware Designer

Dec 2023 – June 2024 | RISE Lab, IIT Madras

- Implementing Packed Single Instruction, Multiple Data (**PSIMD**) instructions on **Shakti's C-class SOC** in **BlueSpec Verilog** and testing using Python simulations
- Performing **Area vs Speed calculations** with tests on **Xilinx's Arty7 100T FPGA** and **Synopsys Design Compiler** to obtain optimised performance
- Integrating the newly designed p-box module with the processor pipeline and testing its performance

TEAM AVISHKAR HYPERLOOP | Electrical Systems Engineer

Sept 2022 – Aug 2023 | Centre For Innovation, IIT Madras

- Designed and tested a **4-layer PCB** employing the TI development board LAUNCHXL-F28379D Delfino MCU to run the inverter and collect data from the **Intelligent Power Module** monitoring the inverter
- Configured an externally procured **Battery Management System** (BMS) with self-designed high voltage battery packs, tested **CAN communication** and implemented **fault states** through BMS based on safety limits
- Assembled and tested **battery packs with LFP cells** (net configuration of 88s 4p) by charging and discharging them while monitoring parameters like **SoC, SoH**, etc and logged data to observe passive **cell balancing**

Course Projects

8-BIT CARRY SAVE MULTIPLIER | Digital IC Design

July 2023 – Dec 2023

- Designed a **transistor-level schematic and layout** of an 8-bit **Carry Save Multiplier** on Electric with multi-level Carry Lookahead Adder for vector merge
- Achieved a 49% increase in delay between RC-extracted layout and schematic
- Designed a **pipelined** schematic using **C2MOS Dynamic Flip Flops** to achieve an 85% increase in operating clock frequency from 1.86MHz to 3.75MHz

COMPUTER ORGANIZATION

July 2023 – Nov 2023

- Solved various arithmetic problems like barrell shifter using Verilog and verified timing diagrams on Xilinx Vivado
- Analyzed the change in **Translation Lookaside Buffer (TLB)** miss rate for different virtual memory sizes using **Champsim**, a trace based memory simulator

Skills

PROGRAMMING

C • Python • PyTorch • Verilog • BlueSpecVerilog • x86 Assembly

TOOLS/PLATFORMS

Electric • Altium Designer • Vivado • LTSpice • MATLAB • Synopsys Design Compiler • Vivado HLS

Education

INDIAN INSTITUTE OF TECHNOLOGY MADRAS

B.Tech in Engineering Physics

Nov 2021 - Present | Chennai, India

CGPA: 8.67 / 10

Coursework

GRADUATE

Embedded Memory Design
Digital IC Design
Analog IC Design
Deep Learning for Imaging
Mapping DSP Algos. to Arch.

UNDERGRADUATE

Computer Organization
Machine Learning Techniques
Analog Circuits
Digital Signal Processing
Solid State Devices

Volunteering

AVANTI FELLOWS

Mentored and guided class 11, 12 students for competitive exams like JEE, KVPY and olympiads

SAATHI

Guided college freshmen with academic and non-academic issues through their first year

Achievements

JEE Advanced 2021
All India Rank 1013

KVPY SA Scholar
All India Rank 365