# Vaibhav Krishna Garimella

vg2651@columbia.edu | (669) 544-9986

## EDUCATION

### COLUMBIA UNIVERSITY
MS in Electrical Engineering
Expected Dec 2026
New York, NY

### IIT MADRAS
BTech in Engineering Physics
Grade: 8.8/10
2021 - 2025
Chennai, India

## COURSEWORK

### ONGOING @ COLUMBIA
Advanced Logic Design
Adv. VLSI Design and Automation
Digital VLSI Circuits
Analog Electronic Circuits

### COMPLETED @ IITM
Embedded Memory Design
Digital IC Design
Analog IC Design
Neuromorphic Computing
Deep Learning for Imaging
Mapping DSP Algos. to Arch.
Computer Organization
Machine Learning Techniques
Analog Circuits
Digital Signal Processing
Solid States Devices

## SKILLS

### PROGRAMMING
Python • C • Verilog • PyTorch • BlueSpec Verilog • MATLAB • Mathematica

### TOOLS/PLATFORMS
Cadence Virtuoso • Genus • Innovus • Vivado • Synopsys Design Compiler • Advanced Design System (ADS)

## TA EXPERIENCE

Graduate Level Courses
• Digital IC Design, Summer 2025
• Digital IC Design, Spring 2025
• Modelling and Opt. in VLSI, Spring 2025

Undergraduate Level Courses
• Computer Organization, Fall 2024

## RESEARCH EXPERIENCE

### COMPUTE IN-MEMORY GROUP @ IIT MADRAS
Time-Domain Compute In-Memory Chip Tape-Out
- Designed the layout for the full SRAM array (~40KB) and peripherals like Sense Amp and Word Line Drivers and performed RC-extracted Monte Carlo simulations to verify functionality and compute read/write times.
- Designed a calibrated Voltage-to-Time Converter (VTC)
- Analyzed layer-wise statistics of various Neural Networks and tested inferences based on ADC-bit and MAC length limitations

### SHAKTI PROCESSOR
Instruction Set Architecture Design and Testing [Github]
- Implemented Packed Single Instruction, Multiple Data (PSIMD) instructions on Shakti's C-class SOC in BlueSpec Verilog
- Performed Area vs Speed calculations benchmarked against M-extension instructions using Synopsys Design Compiler to obtain optimized performance

### TEAM AVISHKAR HYPERLOOP
Electrical Systems Design
- Designed and tested a 4-layer PCB to run the inverter and collect pod-critical data from the Intelligent Power Module monitoring the inverter
- Configured a Battery Management System (BMS) with self-designed high voltage battery packs, tested CAN communication and implemented fault states through the BMS based on safety limits

## COURSE PROJECTS

### EMBEDDED MEMORY DESIGN
Charge-Domain Compute In-Memory Engine Design
- Designed a Charge-Domain based 9T-1C Compute In-Memory engine
- Performed Monte-Carlo simulations to verify robustness of memory by computing read, write and hold margins

### DEVICES FOR AI AND NEUROMORPHIC COMPUTING
NVM-based Compute In-Memory Engine [Github]
- Designed a 2-layer feedforward neural network using CMOS neurons and NVM (RRAMs and FeFETs) synaptic arrays
- Implementing Sigmoid and tanh activation functions using MOS transistors as part of the In-Memory Computing array for alphabet classification

### DEEP LEARNING FOR IMAGING
Defect Preserving Image Denoising [Github]
- Implemented a Residual Channel Attention Network model to denoise MVTec Anomaly Detection dataset images while keeping the object defect intact
- Implementing Sigmoid and tanh activation functions using MOS transistors as part of the In-Memory Computing array for alphabet classification

### DIGITAL IC DESIGN
8-Bit Carry Save Multiplier Design
- Designed a transistor-level schematic and layout of an 8-bit Carry Save Multiplier on Electric with multi-level Carry Lookahead Adder for vector merge
- Designed a pipelined schematic using C2MOS Dynamic Flip Flops to achieve an 85% increase in operating clock frequency from 1.86MHz to 3.75MHz