Vagicharla Mani kanta

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RESUME SUMMARY

"I am a passionate electronics engineering student with a strong foundation in digital electronics, Verilog HDL, and VLSI design. I have completed a successful internship in Sri Shasha Prayathi technologies, where I gained hands-on experience in FIR filter design using Verilog. I am eager to apply my skills and knowledge in a challenging role to contribute to the advancement of the field."

PERSONAL DETAILS

Current Location	Bapatla
Date of birth	November 30, 2002
Gender	Male

EDUCATION

Graduation	B.Tech/B.E. (Electronics/Telecommunication) Bapatla Engineering College, Bapatla, Bapatla with Score 7.9%
Class XII	Andhra Pradesh with 95% in 2020
Class X	Andhra Pradesh with 85% in 2018
Certification Course	HTML5 (October 2023 - Present)

INTERNSHIPS AND PROJECTS

Internships	**Sri Shasha prayathi technologies Pvt.Ltd** (Duration May 2023 - June 2023) I learned so many new things and technologies through this internship also designed a fir filter using verilog . Based on knowledge of verilog I practicing more circuits in digital electronics like adders , encoders ,multiplexers,decoders,demultiplexers, seven segment decoder etc.. Skills used - C
Projects	**fir digital filter design** (Duration May 2023 - June 2023) I had completed VLSI SIGNAL PROCESSING six weeks internship in Sri Shasha Prayathi technologies in online mode. In the perid of internship doing a small minor project . the project title is FIR filter design using verilog hdl in xilinx vivado tool.

SKILLS AND ACHIEVEMENTS

Skills	Digital Electronics,Verilog HDL,VLSI Design,RTL Design,C,Microprocessors,Html/Css
Language	english (Both)