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HSF Property:ROHS or Halogen-Free

DAKAR10F/FG
(45W CPU)

MP(A02) BUILD

2012.03.23

DATE	CHANGE NO.	REV
21-OCT-2002		

	EE	DATE	POWER	DATE
DRAWER	LOREN	2012.03.23	EDISON	2012.03.23
DESIGN	LOREN	2012.03.23	EDISON	2012.03.23
CHECK	BRYAN	2012.03.23	BY	2012.03.23
RESPONSIBLE	BRYAN	2012.03.23	BY	2012.03.23

SIZE: VER:

FILE NAME:

P/N: XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DAKAR10F/FG MAIN BOARD

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310A0491301-0-MTR	X01

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3. BLOCK DIAGRAM
4. POWER MAP
5. POWER CHARGER
6. POWER +V3LA/+V3A/+5A
7. POWER +V1.5/+V0.75
8. POWER +V1.8S
9. POWER VCCIO
10. POWER VCCSA
11. POWER VCORE
12. POWER VGFX
13. POWER VCORE_DGPU
14. ENABLE PIN
15. LOAD SWITCH-1
16. LOAD SWITCH-2
17. PCB SCREW
18. HALL SENSOR
19. LED
20. K/B & TP/B CONN
21. EC
22. LAN
23. RJ45 & TRANSFORMER
24. AUDIO CODEC
25. SPEAKER/HP JACK/MIC JACK

PAGE

26. CARDREADER
27. MINI1 WLAN/DEBUG CARD
28. MINI2 3G/LTE
29. SATA HDD/ODD CONN
30. USB 2.0 CONN
31. USB 3.0 CONTROLLER(REMOVE)
32. USB 3.0 CONN W/ S&C
33. USB 3.0 CONN
34. LCM CONN
35. CRT CONN
36. HDMI CONN
37. HDMI CEC
38. DDR3 DIMM0
39. DDR3 DIMM1
40. FAN & THERMAL SENSOR
41. CPU 1
42. CPU 2
43. CPU 3 DRAM
44. CPU 4 POWER
45. CPU 5 POWER
46. CPU 6 GND
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53. PCH 7 POWER
54. PCH 8 POWER
55. PCH 9 GND
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57. VGA 2
58. VGA 3
59. VGA 4
60. VGA 5
61. VGA 6
62. VRAM 1
63. VRAM 2
64. VRAM 3
65. VRAM 4
66. USB BOARD
67. PICK BUTTON BOARD(4 PIN)
68. POWER BUTTON BOARD
69. EMI
70. PICK BUTTON BOARD(8 PIN)

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Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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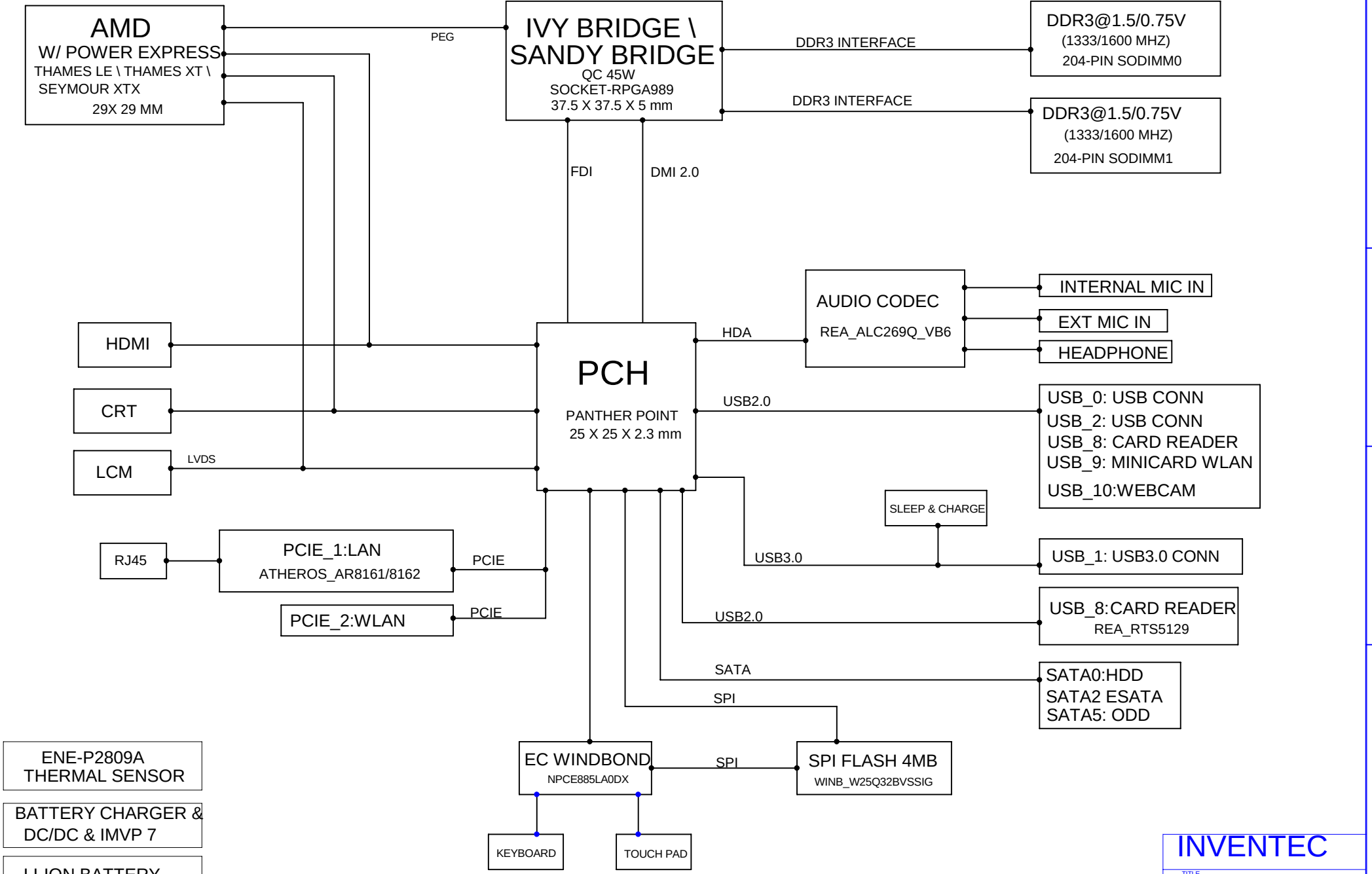

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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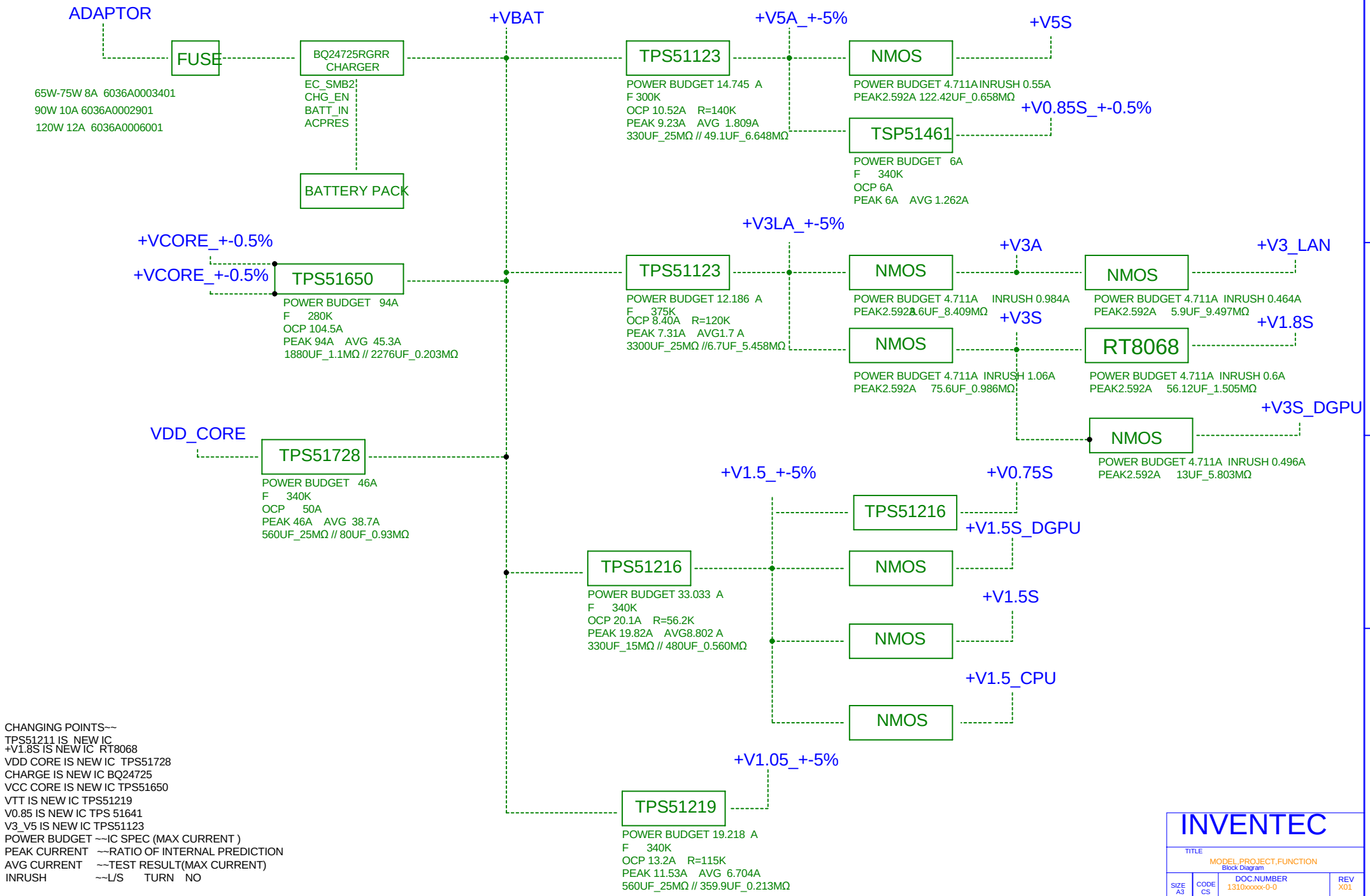

CHANGING POINTS~~
TPS51211 IS NEW IC
+V1.8S IS NEW IC RT8068
VDD CORE IS NEW IC TPS51728
CHARGE IS NEW IC BQ24725
VCC CORE IS NEW IC TPS51650
VTT IS NEW IC TPS51219
V0.85 IS NEW IC TPS 51641
V3_V5 IS NEW IC TPS51123
POWER BUDGET ~~IC SPEC (MAX CURRENT)
PEAK CURRENT ~~RATIO OF INTERNAL PREDICTION
AVG CURRENT ~~TEST RESULT(MAX CURRENT)
INRUSH ~~L/S TURN NO

INVENTEC

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MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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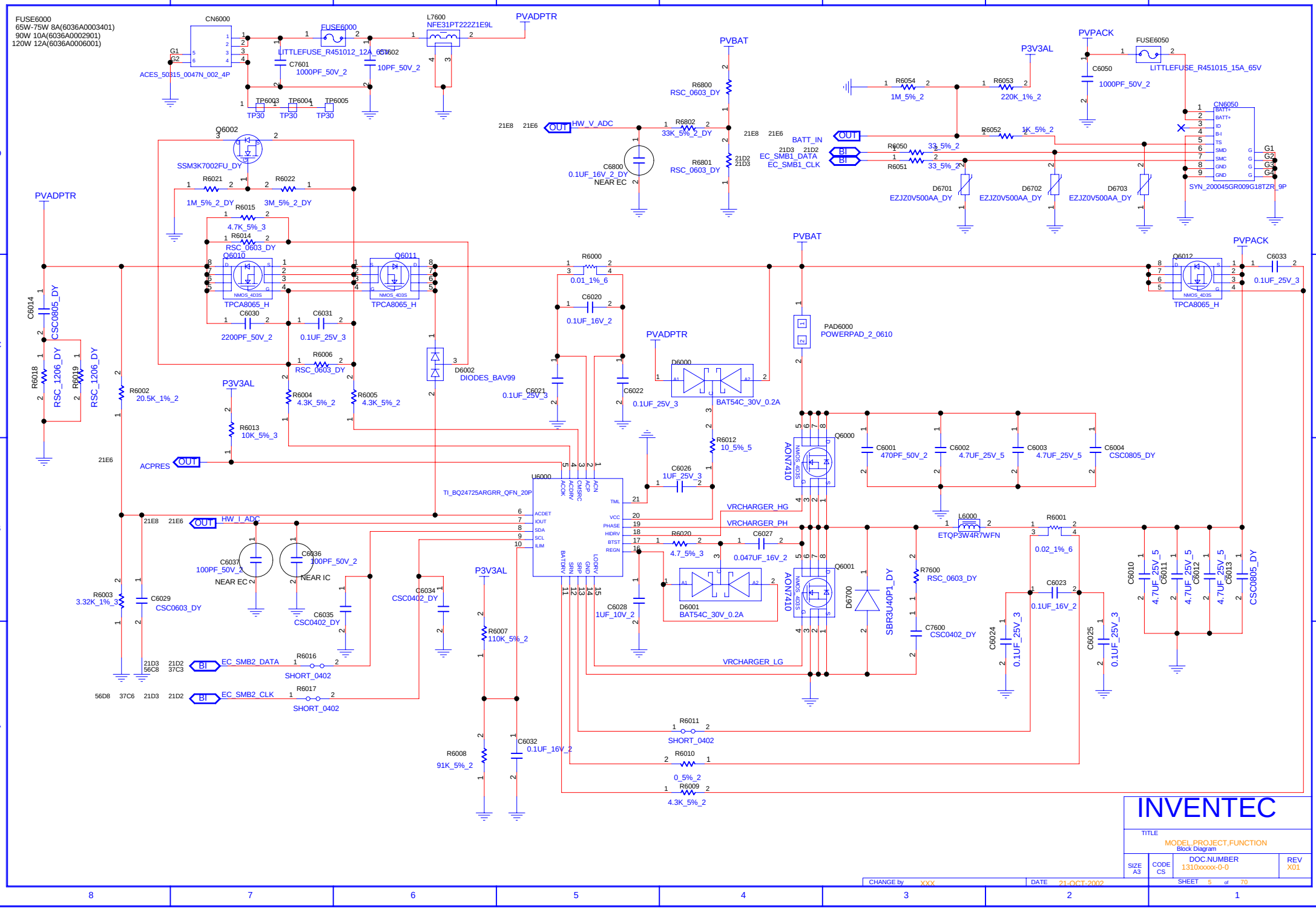
FUSE6000
65W-75W 8A(6036A0003401)
90W 10A(6036A0002901)
120W 12A(6036A0006001)
CN6000
ACES_50315_0047N_002_4P
FUSE6000
LITTLEFUSE_R451012_12A_65V
C7601
1000PF_50V_2
C7602
10PF_50V_2
L7600
NFE31PT222Z1E9L
PVADPTR
TP6003
TP6004
TP6005
TP30
PVBAT
R6800
RSC_0603_DY
R6802
33K_5%_2_DY
R6801
RSC_0603_DY
C6800
0.1UF_16V_2_DY
NEAR EC
HW_V_ADC
BATT_IN
EC_SMB1_DATA
EC_SMB1_CLK
P3V3AL
R6054
1M_5%_2
R6053
220K_1%_2
R6052
1K_5%_2
R6050
33_5%_2
R6051
33_5%_2
PVPACK
FUSE6050
LITTLEFUSE_R451015_15A_65V
C6050
1000PF_50V_2
CN6050
SYN_200045GR009G18TZR_9P
D6701
D6702
D6703
EZJZ0V500AA_DY
Q6002
SSM3K7002FU_DY
R6021
1M_5%_2_DY
R6022
3M_5%_2_DY
R6015
4.7K_5%_3
R6014
RSC_0603_DY
Q6010
Q6011
TPCA8065_H
C6030
2200PF_50V_2
C6031
0.1UF_25V_3
R6006
RSC_0603_DY
D6002
DIODES_BAV99
R6000
0.01_1%_6
C6020
0.1UF_16V_2
C6021
0.1UF_25V_3
C6022
0.1UF_25V_3
Q6012
C6033
0.1UF_25V_3
C6014
CSC0805_DY
R6018
RSC_1206_DY
R6019
RSC_1206_DY
R6002
20.5K_1%_2
R6004
4.3K_5%_2
R6005
4.3K_5%_2
R6013
10K_5%_3
ACPRES
D6000
BAT54C_30V_0.2A
PAD6000
POWERPAD_2_0610
C6026
1UF_25V_3
R6012
10_5%_5
U6000
TI_BQ24725ARGRR_QFN_20P
Q6000
AON7410
Q6001
C6001
470PF_50V_2
C6002
4.7UF_25V_5
C6003
4.7UF_25V_5
C6004
CSC0805_DY
L6000
ETQP3W4R7WFN
R6001
0.02_1%_6
C6023
0.1UF_16V_2
C6010
C6011
C6012
C6013
4.7UF_25V_5
CSC0805_DY
VRCHARGER_HG
VRCHARGER_PH
VRCHARGER_LG
R6020
4.7_5%_3
C6027
0.047UF_16V_2
D6001
BAT54C_30V_0.2A
D6700
SBR3U40P1_DY
R7600
RSC_0603_DY
C7600
CSC0402_DY
C6024
C6025
0.1UF_25V_3
HW_I_ADC
C6037
100PF_50V_2
NEAR EC
C6036
100PF_50V_2
NEAR IC
R6003
3.32K_1%_3
C6029
CSC0603_DY
C6035
CSC0402_DY
C6034
CSC0402_DY
EC_SMB2_DATA
EC_SMB2_CLK
R6016
R6017
SHORT_0402
R6007
110K_5%_2
R6008
91K_5%_2
C6032
0.1UF_16V_2
R6011
SHORT_0402
R6010
0_5%_2
R6009
4.3K_5%_2
INVENTEC
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Block Diagram
SIZE A3
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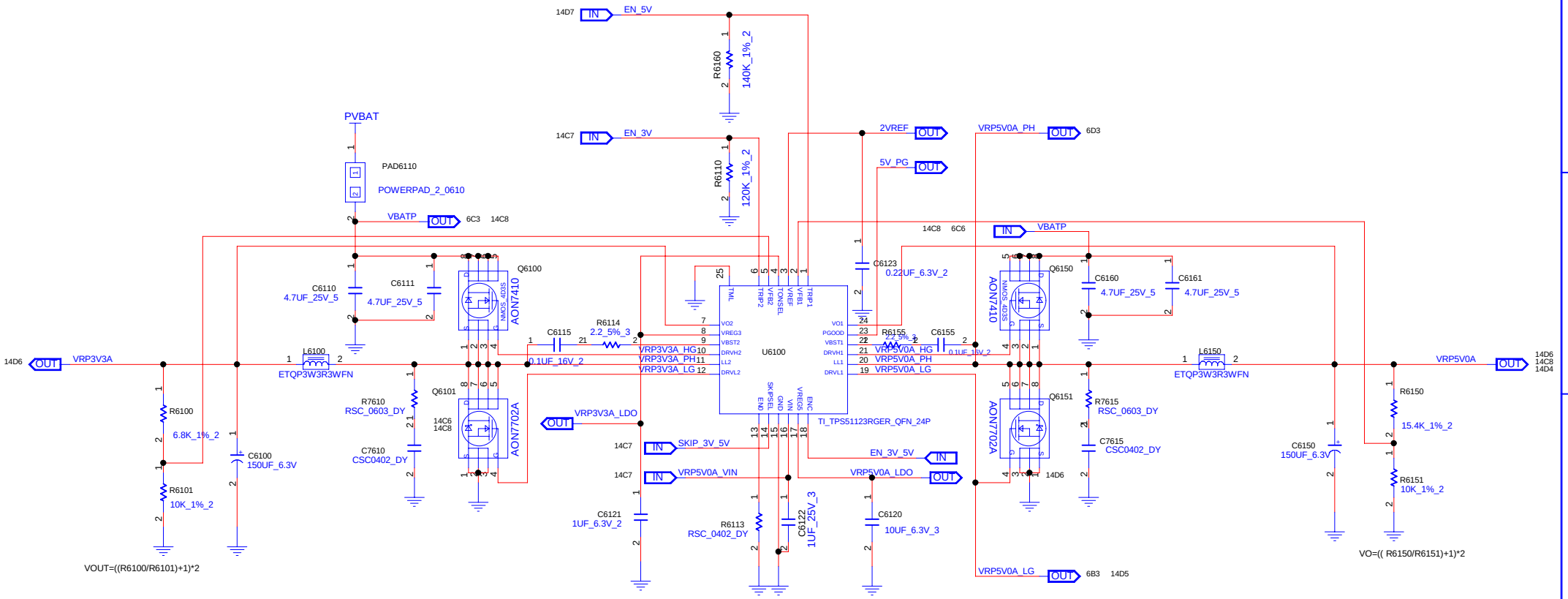

INVENTEC			
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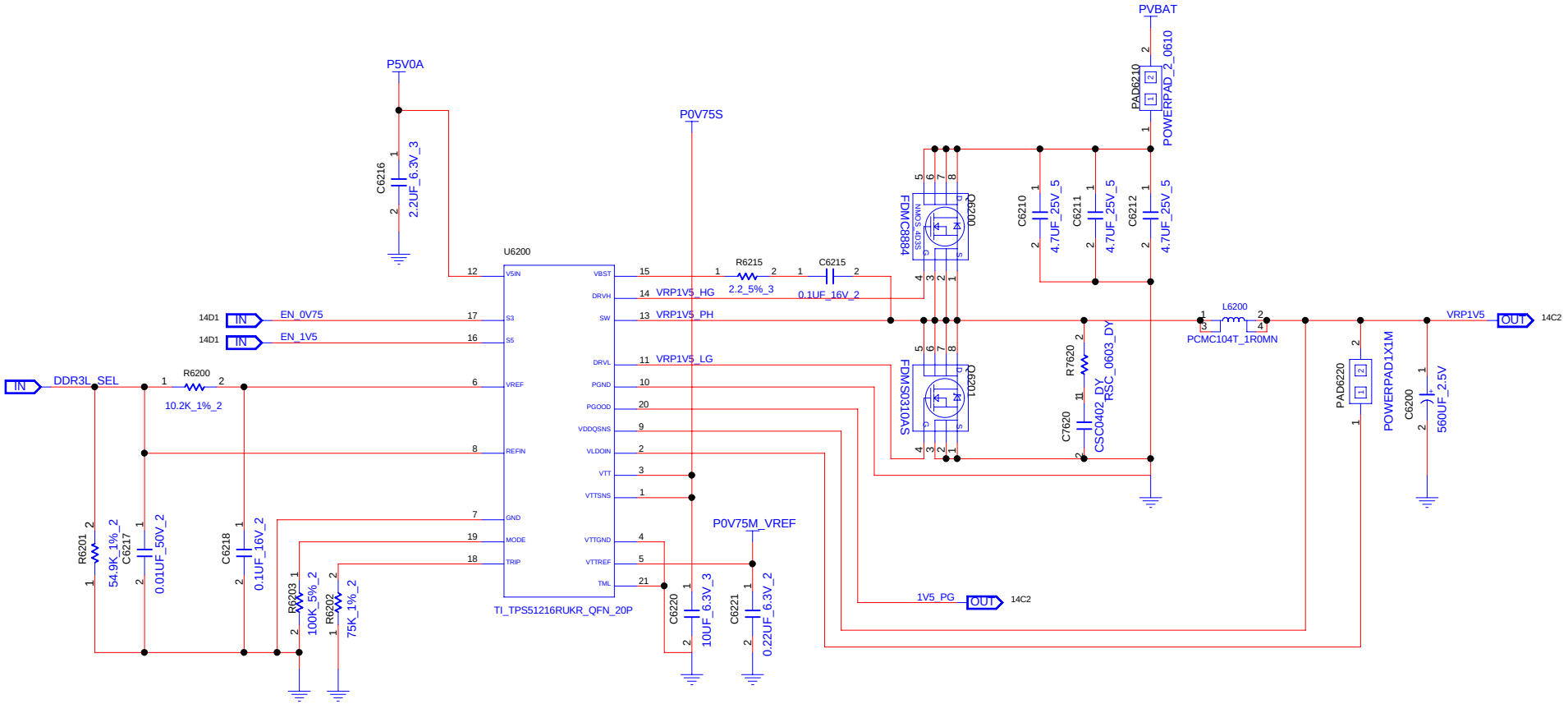

VOUT=REFIN=1.8*(R6201/(R6200+R6201))

MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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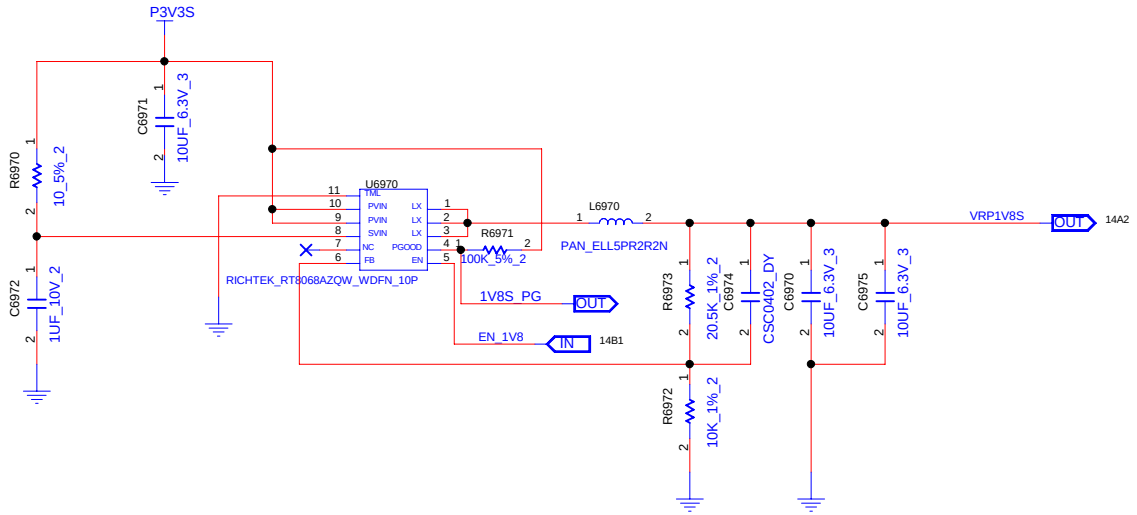

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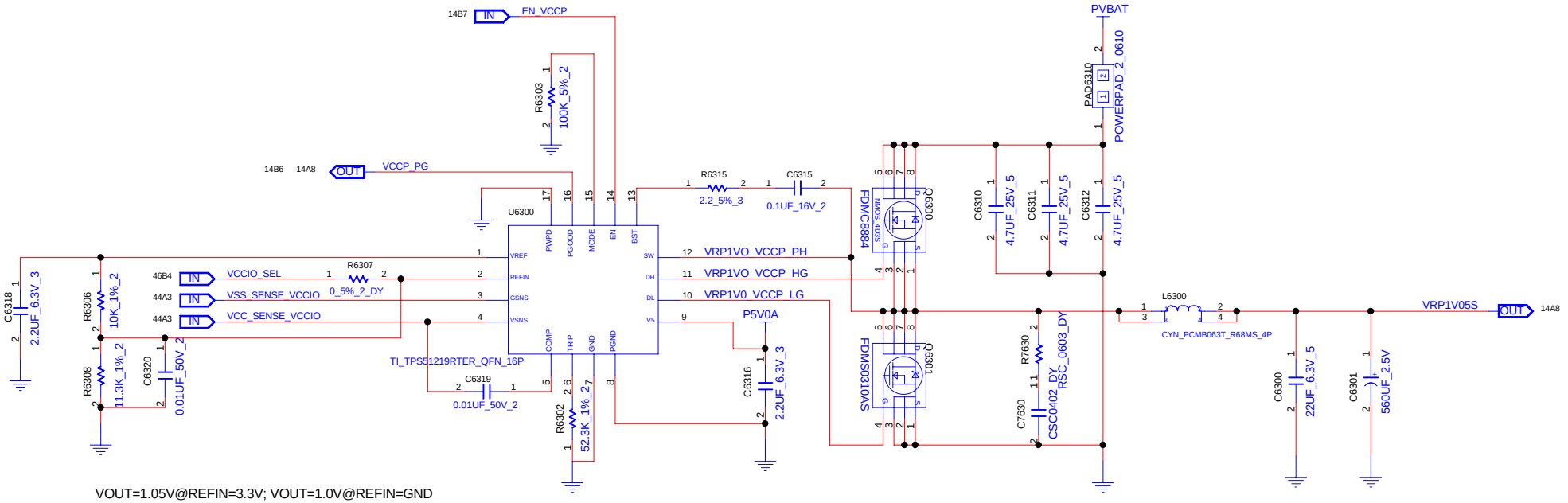

VOUT=1.05V@REFIN=3.3V; VOUT=1.0V@REFIN=GND

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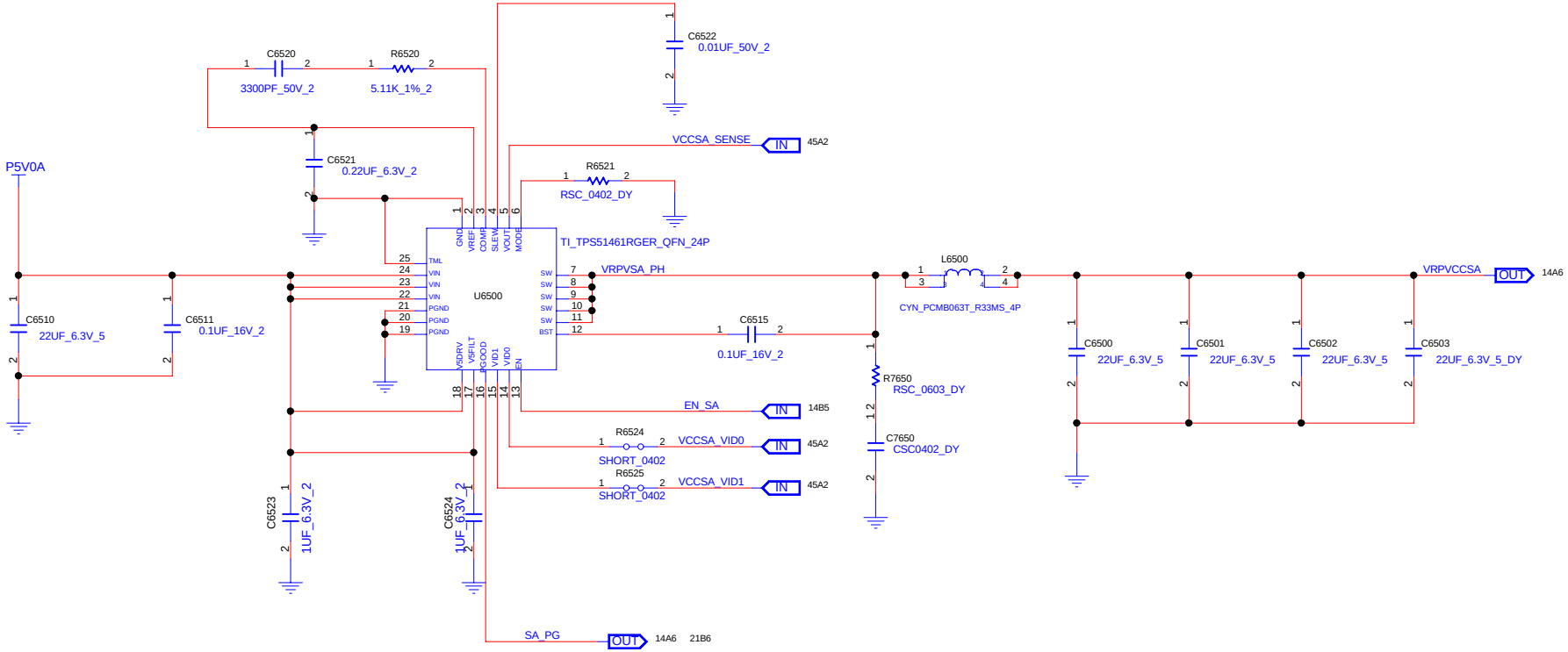

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UMA/PX DIS.

	3+2	3+0	2+1	2+0
R6620	71.5K	71.5K	44.2K	44.2K
R6621	42.2K	42.2K	90.9K	90.9K
R6622	100K	100K	39K	39K
R6626	4.7K	DNP	3.3K	DNP
R6627	75K	DNP	56K	DNP
R6711	100K	DNP	200K	DNP
R6712	24K	DNP	30K	DNP
R6719	DNP	0	DNP	0
R6723	DNP	0	DNP	0
R6635	DNP	DNP	0	0
R6636	DNP	DNP	0	0
R6714	DNP	0	DNP	0
R6716	DNP	0	DNP	0
R6721	DNP	0	0	0
R6725	DNP	0	0	0
R6726	0	DNP	DNP	DNP
R6724	0	DNP	0	DNP
R6722	0	DNP	DNP	DNP
R6720	0	DNP	0	DNP
R6713	0	DNP	0	DNP
R6715	0	DNP	0	DNP

U6600

TI_TPS51650RSLR_QFN_48P

INVENTEC

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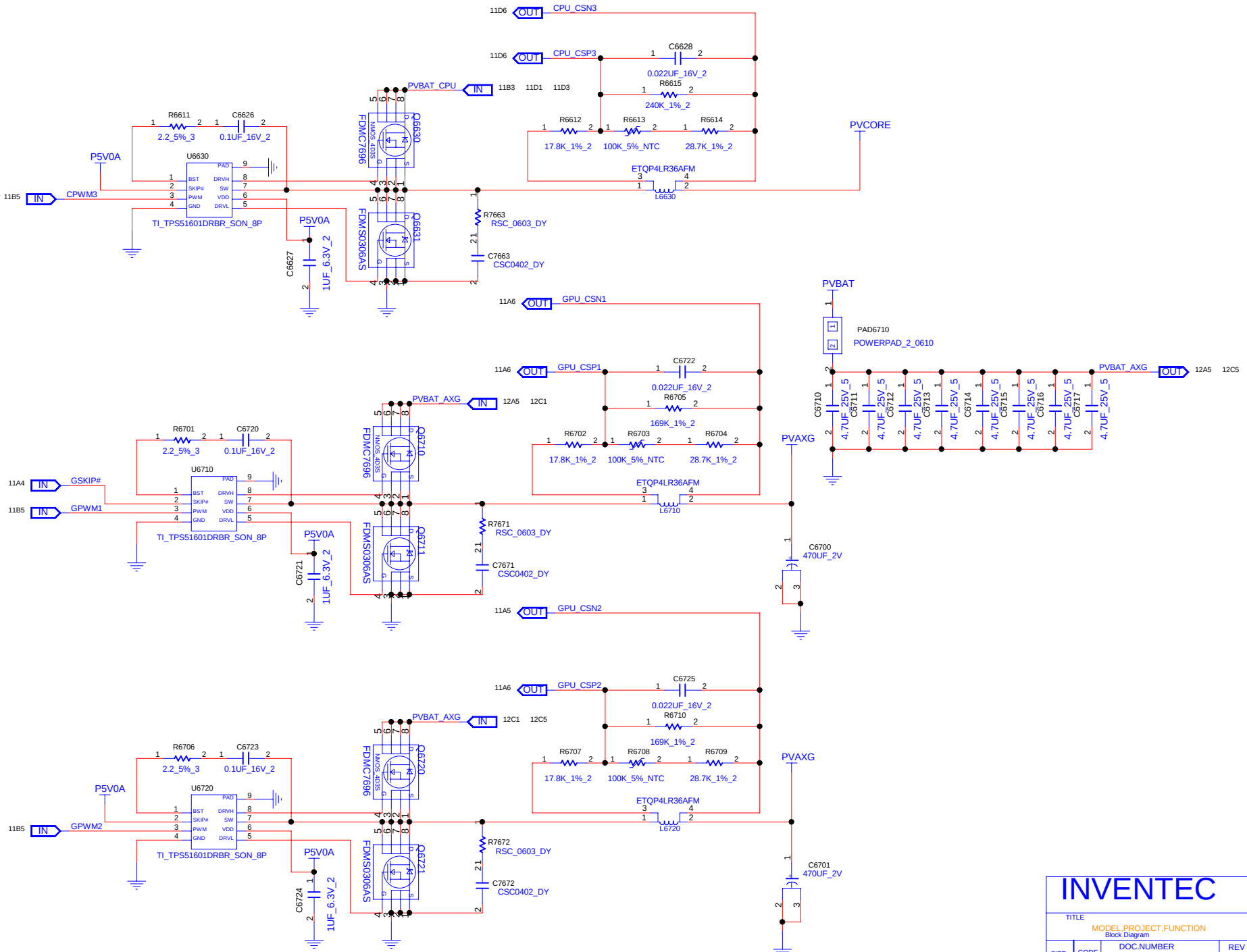
11D6 OUT CPU_CSN3
11D6 OUT CPU_CSP3
C6628
0.022UF_16V_2
R6615
240K_1%_2
R6612
17.8K_1%_2
R6613
100K_5%_NTC
R6614
28.7K_1%_2
PVBAT_CPU IN 11B3 11D1 11D3
PVCORE
R6611
2.2_5%_3
C6626
0.1UF_16V_2
P5V0A
U6630
TI_TPS51601DRBR_SON_8P
11B5 IN CPWM3
Q6630
Q6631
FDMC7696
FDMS3036AS
ETQP4LR36AFM
L6630
R7663
RSC_0603_DY
C7663
CSC0402_DY
C6627
1UF_6.3V_2
11A6 OUT GPU_CSN1
PVBAT
PAD6710
POWERPAD_2_0610
PVBAT_AXG OUT 12A5 12C5
C6710
4.7UF_25V_5
11A6 OUT GPU_CSP1
C6722
0.022UF_16V_2
R6705
169K_1%_2
R6702
17.8K_1%_2
R6703
100K_5%_NTC
R6704
28.7K_1%_2
PVBAT_AXG IN 12A5 12C1
R6701
2.2_5%_3
C6720
0.1UF_16V_2
U6710
11A4 IN GSKIP#
11B5 IN GPWM1
Q6710
Q6711
L6710
R7671
RSC_0603_DY
C7671
CSC0402_DY
C6721
1UF_6.3V_2
PVAXG
C6700
470UF_2V
11A5 OUT GPU_CSN2
11A6 OUT GPU_CSP2
C6725
0.022UF_16V_2
R6710
169K_1%_2
R6707
17.8K_1%_2
R6708
100K_5%_NTC
R6709
28.7K_1%_2
PVBAT_AXG IN 12C1 12C5
R6706
2.2_5%_3
C6723
0.1UF_16V_2
U6720
11B5 IN GPWM2
Q6720
Q6721
L6720
R7672
RSC_0603_DY
C7672
CSC0402_DY
C6724
1UF_6.3V_2
C6701
470UF_2V
INVENTEC
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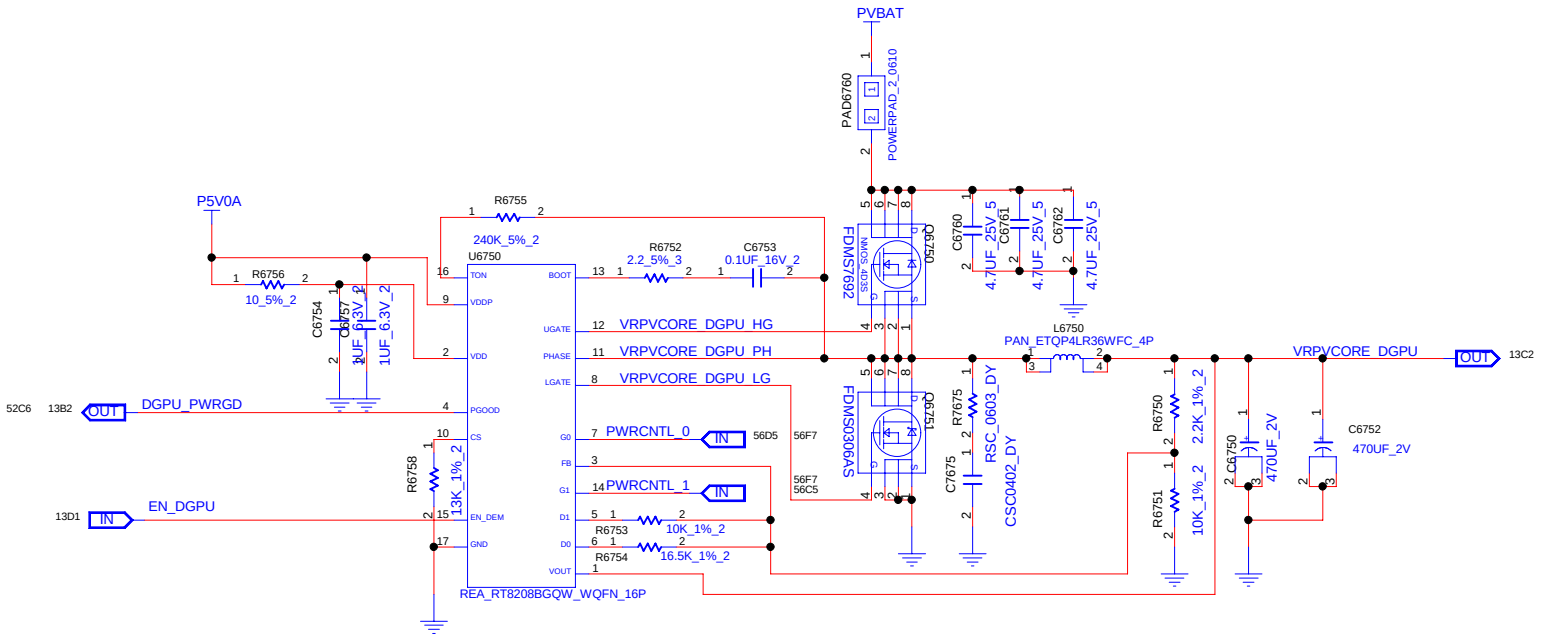
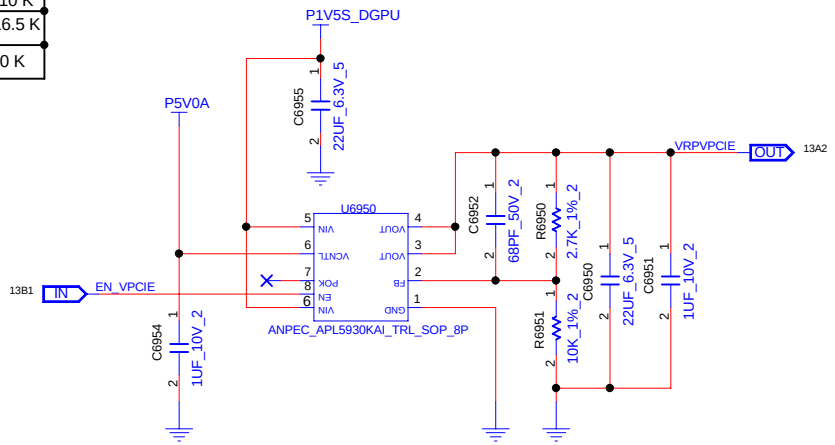
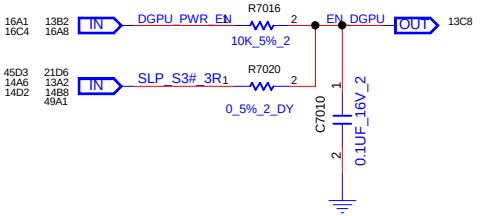


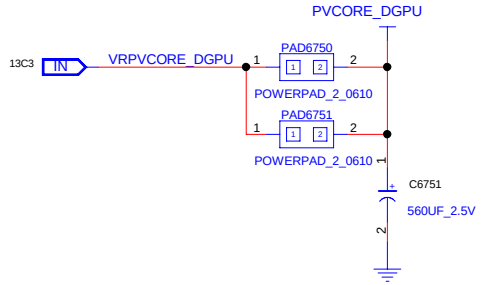
P.S. R6750(R1)R6751(R2)R6753(R3)R6754(R4)

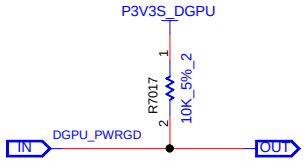
VGA TYPE :		SEYMOUR XTX	THAMES XT	THAMES LE	
G0	G1	VOUT	VOUT	VOUT	RESISTOR VALUE
0	0	1.15	N/A	N/A	R6750(R1) 2.2 K
0	1	1.05	N/A	N/A	R6751(R2) 10 K
1	0	1	1	1	R6754(R3) 16.5 K
1	1	0.9	0.9	0.9	R6753(R4) 10 K

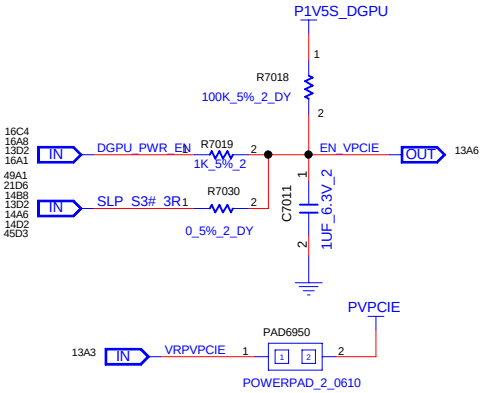
RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$











INVENTEC

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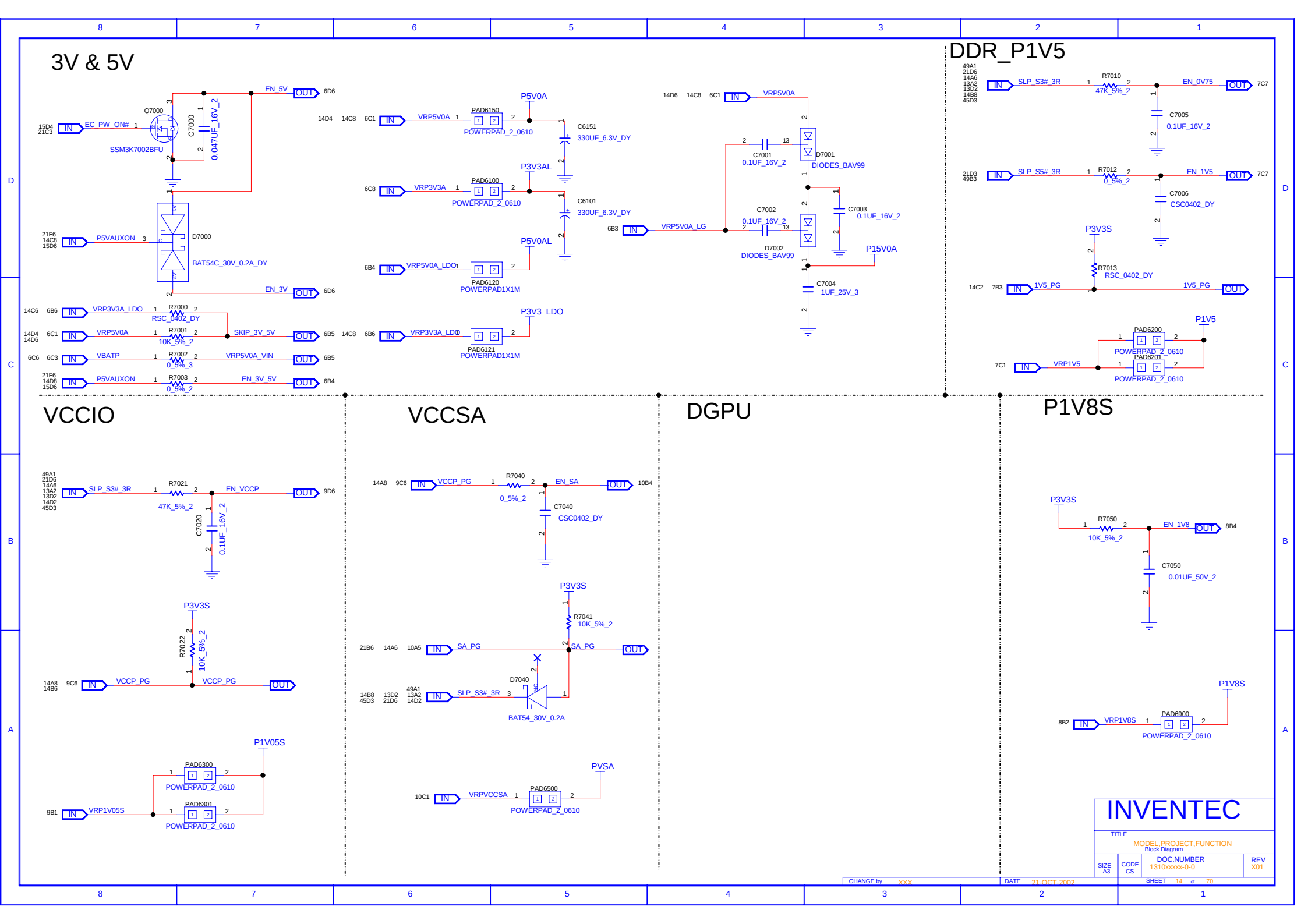
3V & 5V
EN_5V
OUT
6D6
Q7000
15D4
21C3
IN
EC_PW_ON#
1
SSM3K7002BFU
C7000
0.047UF_16V_2
D7000
21F6
14C8
15D6
P5VAUXON
3
BAT54C_30V_0.2A_DY
EN_3V
14C6
6B6
VRP3V3A_LDO
R7000
RSC_0402_DY
14D4
14D6
6C1
VRP5V0A
R7001
10K_5%_2
SKIP_3V_5V
6B5
6C6
6C3
VBATP
R7002
0_5%_3
VRP5V0A_VIN
21F6
14D8
15D6
R7003
0_5%_2
EN_3V_5V
6B4
P5V0A
PAD6150
POWERPAD_2_0610
C6151
330UF_6.3V_DY
P3V3AL
6C8
VRP3V3A
PAD6100
C6101
330UF_6.3V_DY
P5V0AL
6B4
VRP5V0A_LDO
PAD6120
POWERPAD1X1M
P3V3_LDO
14C8
6B6
VRP3V3A_LDO
PAD6121
POWERPAD1X1M
14D6
14C8
6C1
VRP5V0A
C7001
0.1UF_16V_2
D7001
DIODES_BAV99
6B3
VRP5V0A_LG
C7002
0.1UF_16V_2
D7002
DIODES_BAV99
C7003
0.1UF_16V_2
P15V0A
C7004
1UF_25V_3
DDR_P1V5
49A1
21D6
14A6
13A2
13D2
14B8
45D3
SLP_S3#_3R
R7010
47K_5%_2
EN_0V75
7C7
C7005
0.1UF_16V_2
21D3
49B3
SLP_S5#_3R
R7012
0_5%_2
EN_1V5
C7006
CSC0402_DY
P3V3S
R7013
RSC_0402_DY
14C2
7B3
1V5_PG
P1V5
PAD6200
POWERPAD_2_0610
7C1
VRP1V5
PAD6201
VCCIO
49A1
21D6
14A6
13A2
13D2
14D2
45D3
SLP_S3#_3R
R7021
47K_5%_2
EN_VCCP
9D6
C7020
0.1UF_16V_2
P3V3S
R7022
10K_5%_2
14A8
14B6
9C6
VCCP_PG
P1V05S
PAD6300
POWERPAD_2_0610
9B1
VRP1V05S
PAD6301
VCCSA
14A8
9C6
VCCP_PG
R7040
0_5%_2
EN_SA
10B4
C7040
CSC0402_DY
P3V3S
R7041
10K_5%_2
21B6
14A6
10A5
SA_PG
D7040
14B8
45D3
13D2
21D6
49A1
13A2
14D2
SLP_S3#_3R
BAT54_30V_0.2A
PVSA
10C1
VRPVCCSA
PAD6500
POWERPAD_2_0610
DGPU
P1V8S
P3V3S
R7050
10K_5%_2
EN_1V8
8B4
C7050
0.01UF_50V_2
P1V8S
8B2
VRP1V8S
PAD6900
POWERPAD_2_0610
INVENTEC
TITLE
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DOC.NUMBER
1310xxxxx-0-0
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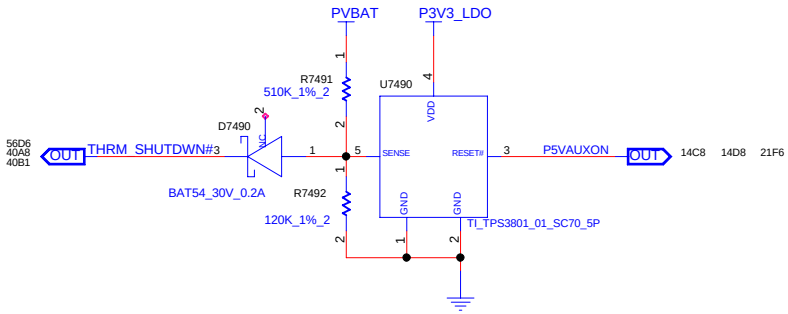

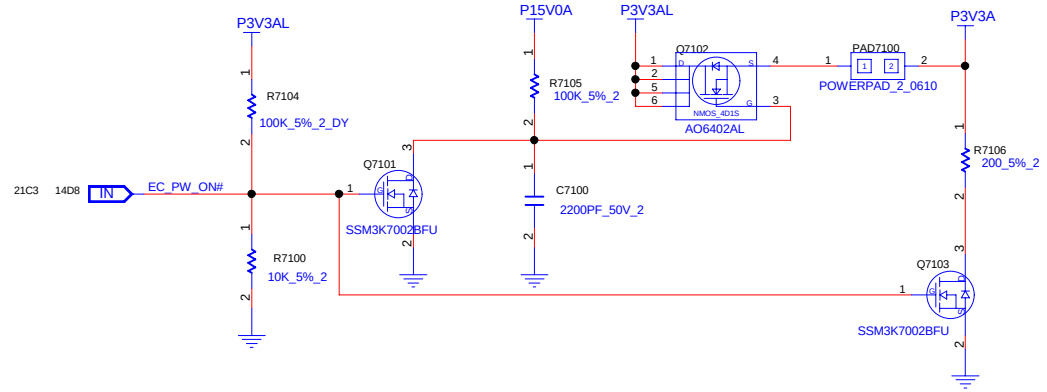

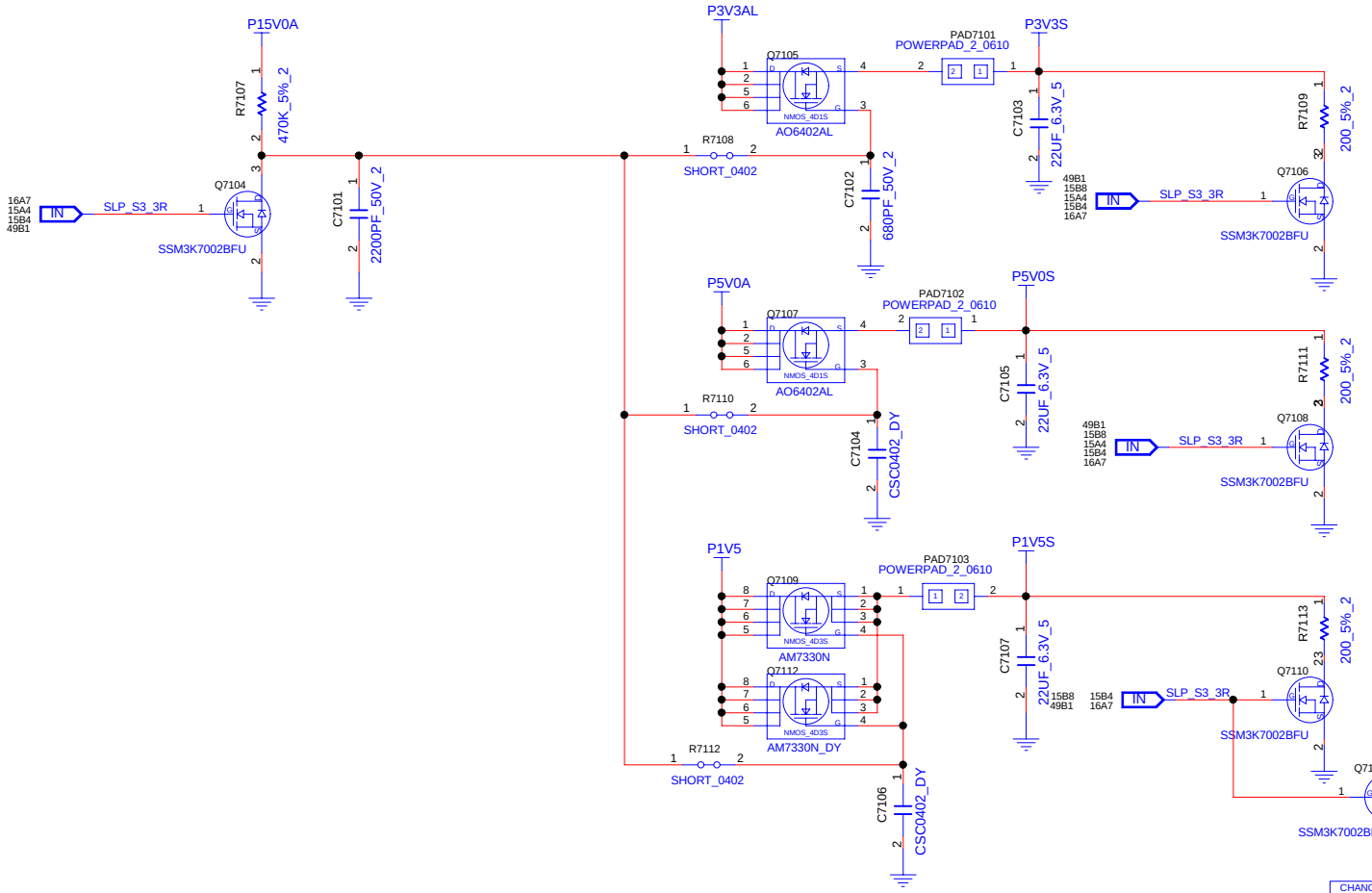

INVENTEC

TITLE
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SIZE	CODE	DOC.NUMBER	REV
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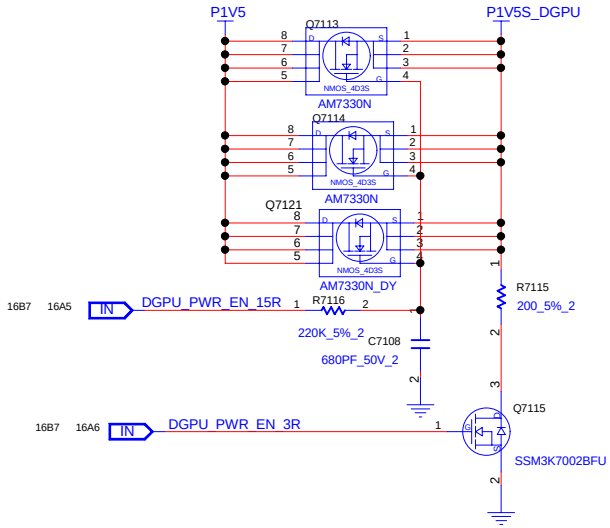
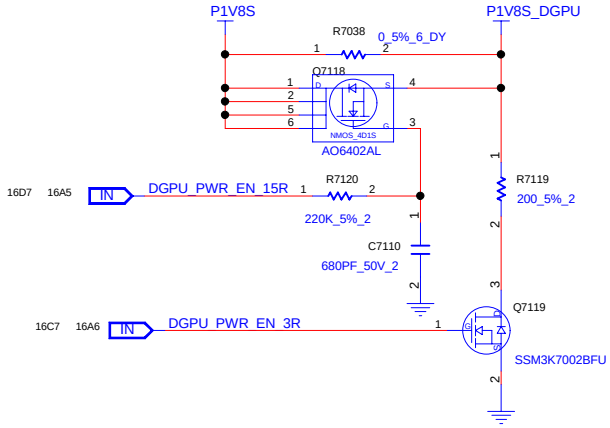
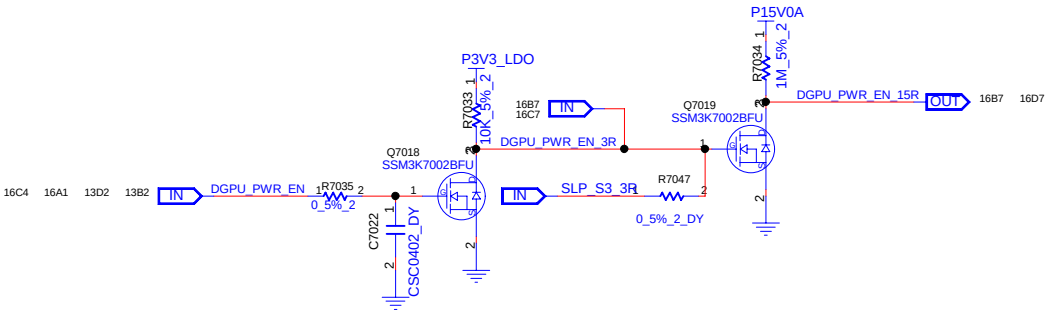
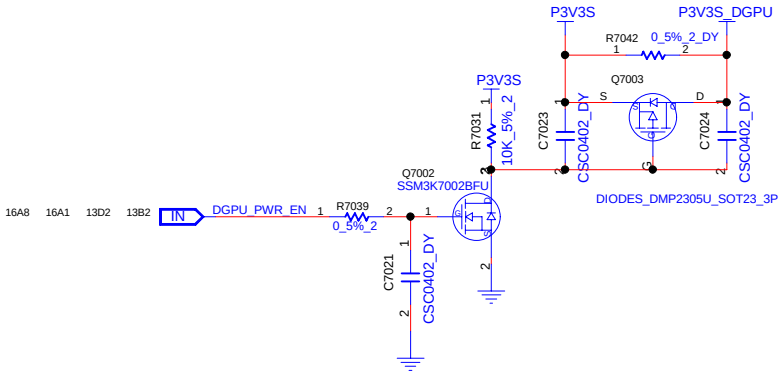


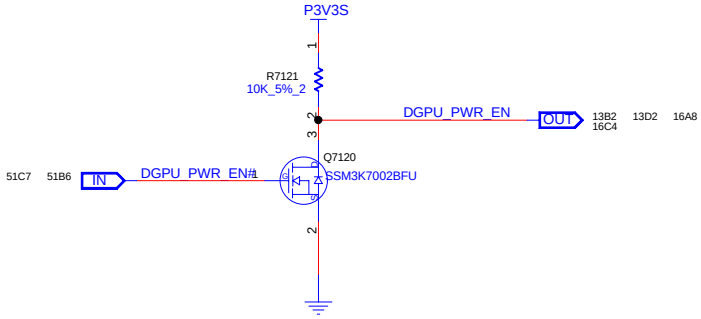




POWER EXPRESS

	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWRGD			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED





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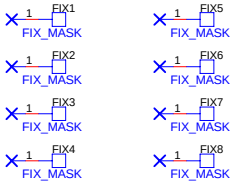
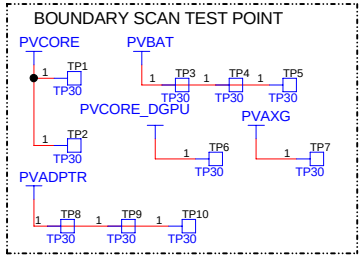
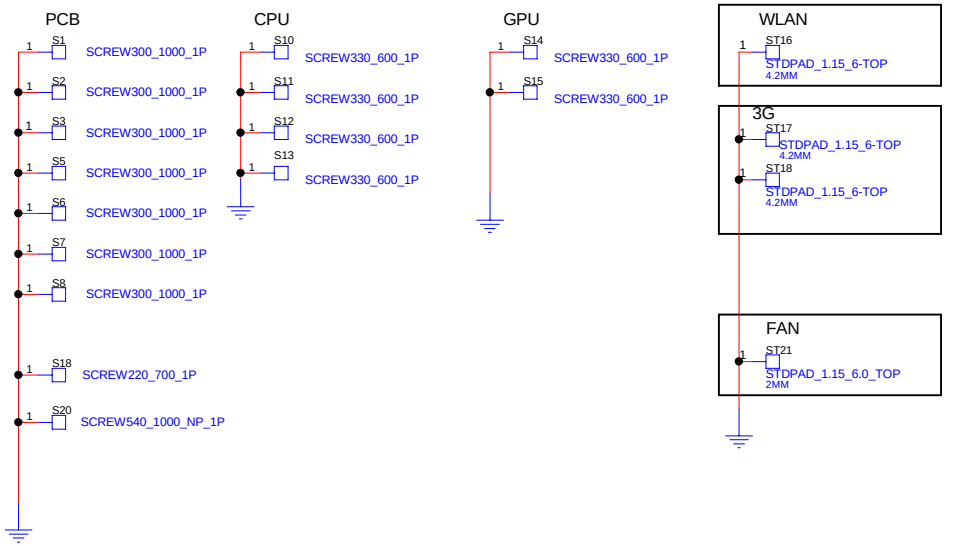
REFERENCE 0~49(PCB SCREW)







INVENTEC

TITLE
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Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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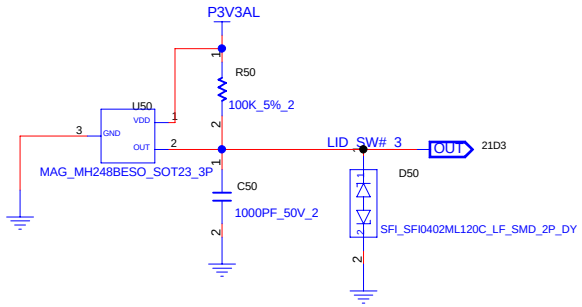
REFERENCE 50-99(HALL SENSOR)



INVENTEC

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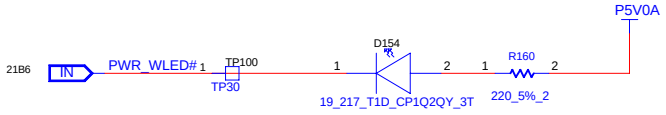
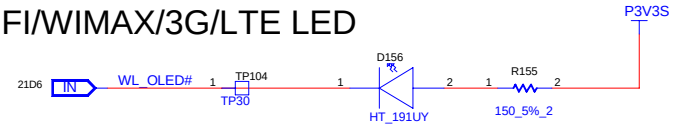
REFERENCE 100~199(LED)

POWER ON LED

D154 BRIGHT WHEN SYSTEM IS POWER ON
D154 BLINK WHEN SYSTEM GO TO SLEEP

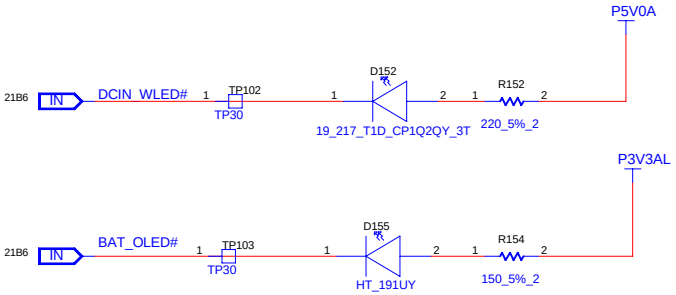


WIFI/WIMAX/3G/LTE LED



DC IN / BATTERY CHARGE LED

D152 BRIGHT:BOTH AC-ADAPTER IS PLUGGED IN AND BATTERY IS FULL CHARGED
D155 BRIGHT:WHILE CHARGING BATTERY FROM AC-ADAPTER
BLINK:LOW BATTERY



INVENTEC

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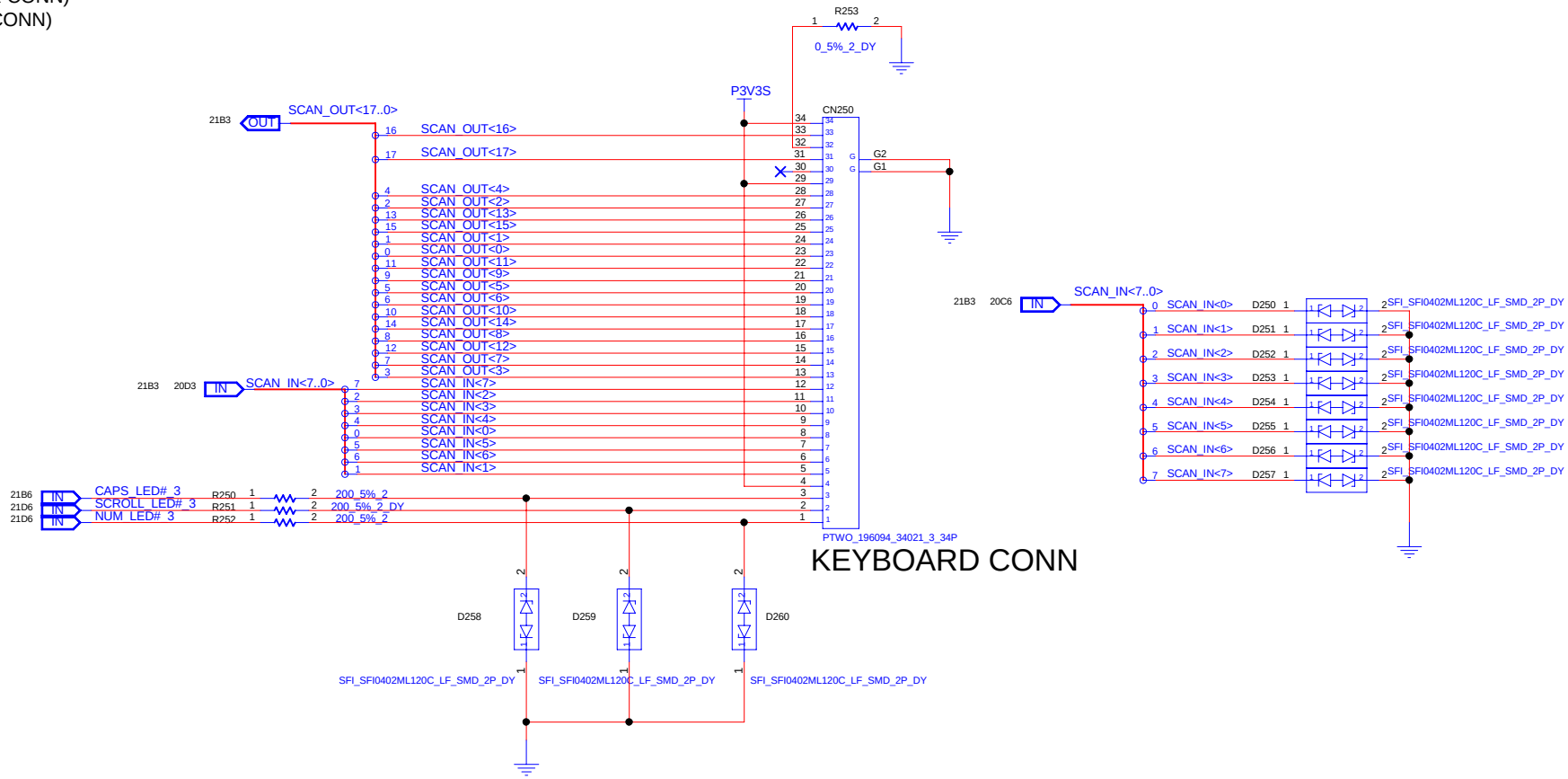
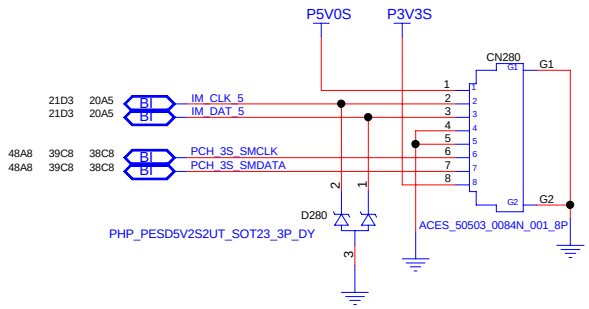
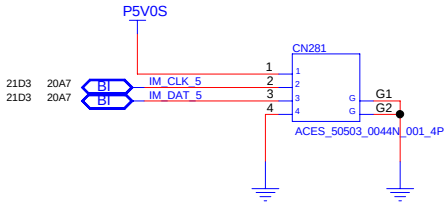
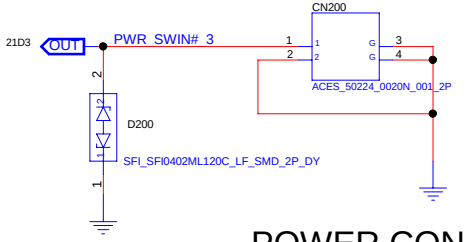
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)







TOUCHPAD CONN



POWER CONN

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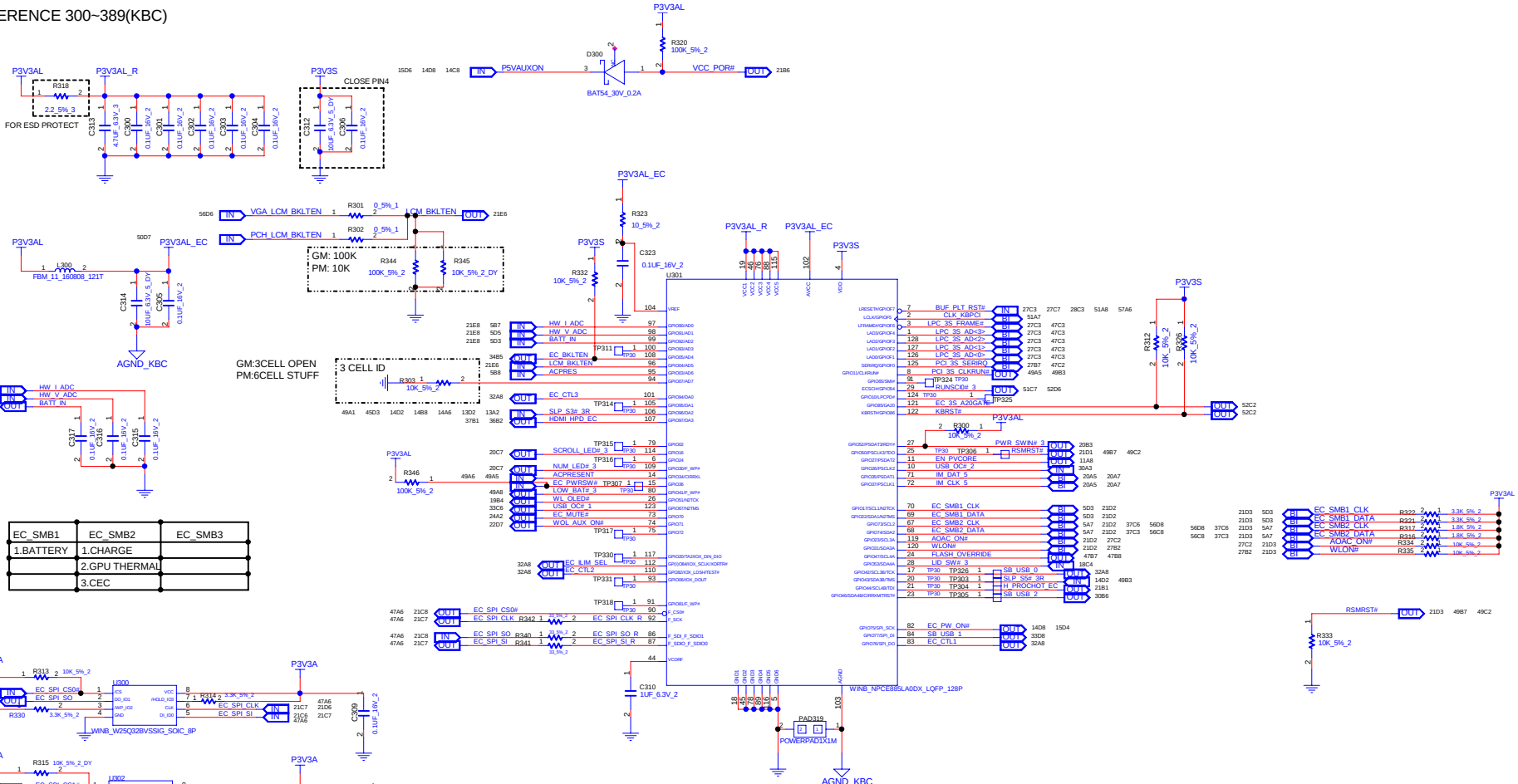
REFERENCE 300~389(KBC)



EC_SMB1	EC_SMB2	EC_SMB3
1.BATTERY	1.CHARGE	
	2.GPU THERMAL	
	3.CEC	

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-0-0	X01

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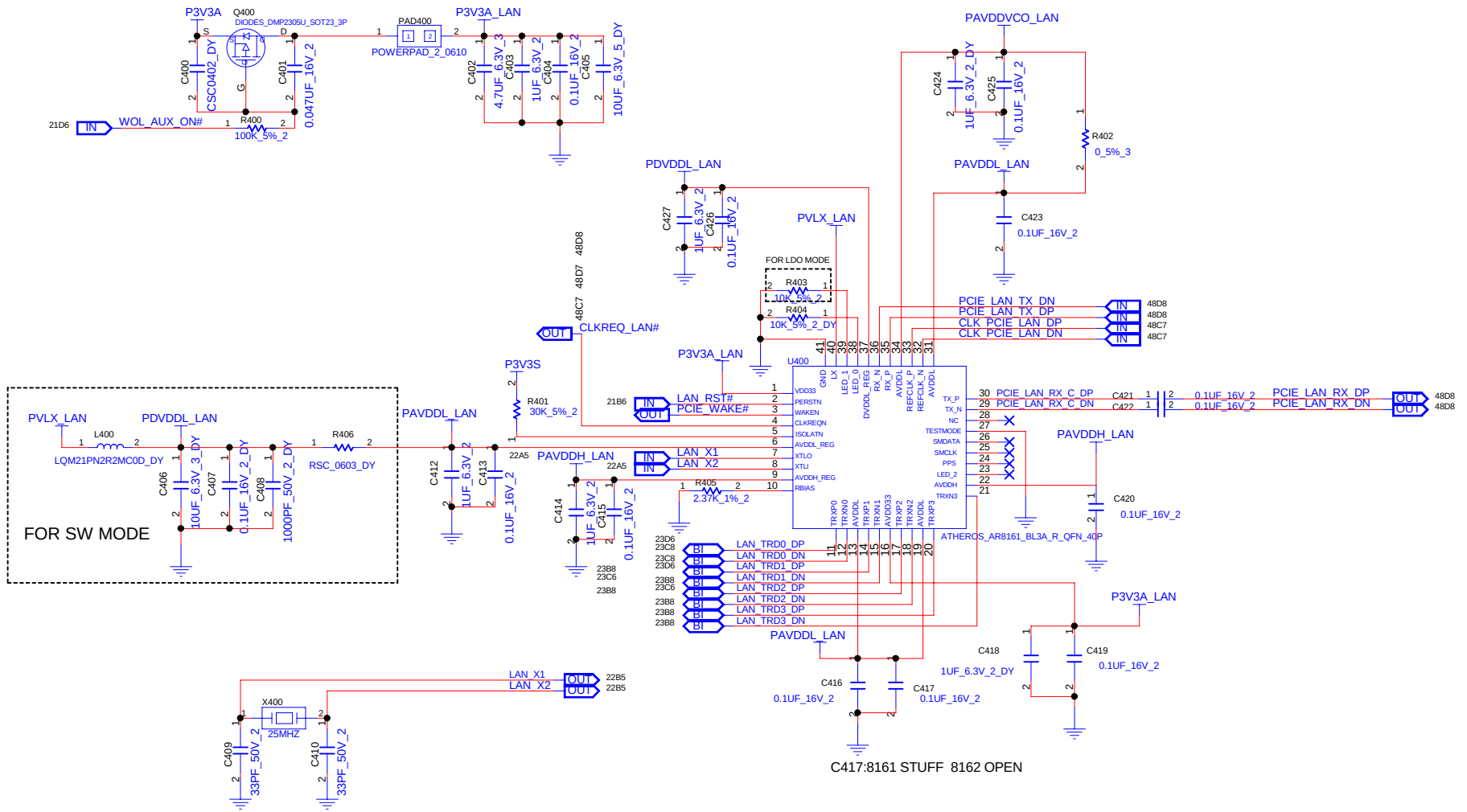
REFERENCE 400~499(LAN)



INVENTEC			
TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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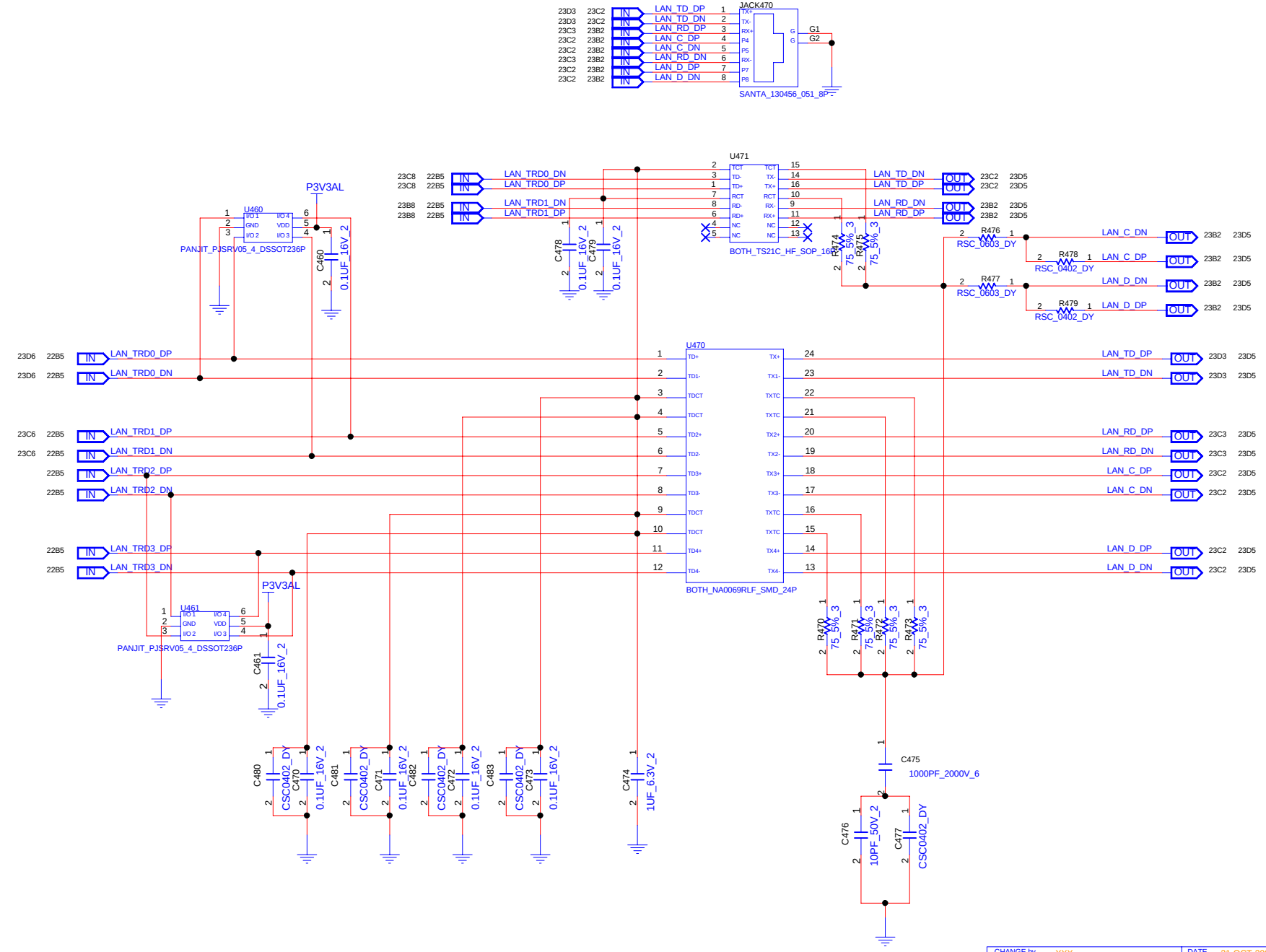
REFERENCE 400~499(LAN)



TITLE	MODEL,PROJECT,FUNCTION Block Diagram
SIZE	A3
CODE	CS
DOC.NUMBER	1310xxxxx-0-0
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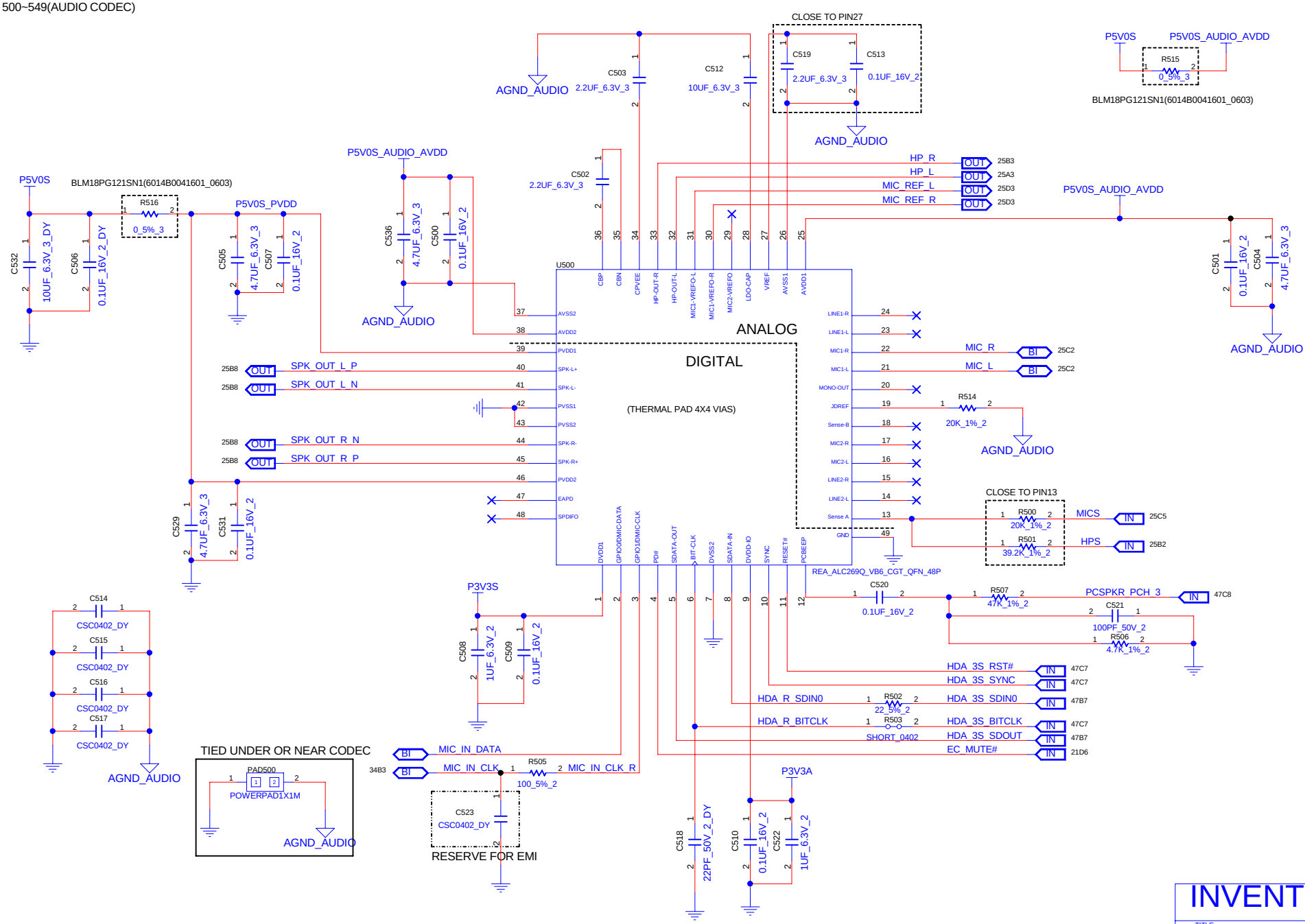
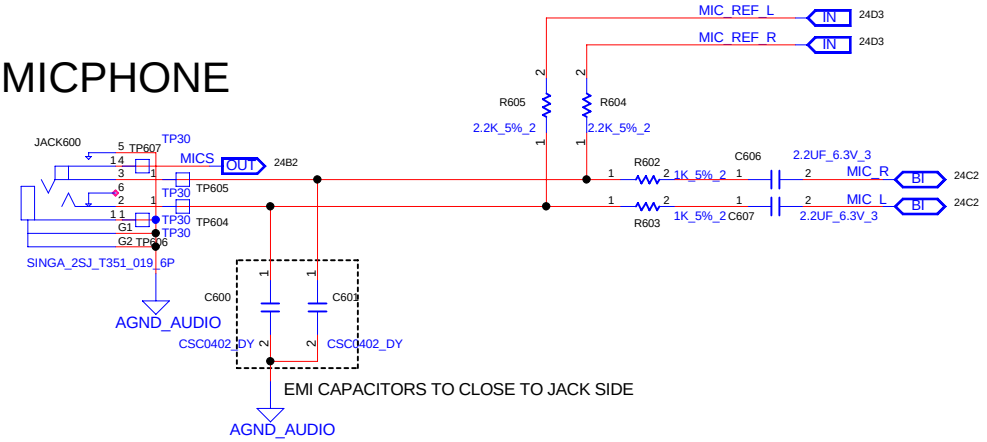
REFERENCE 500~549(AUDIO CODEC)



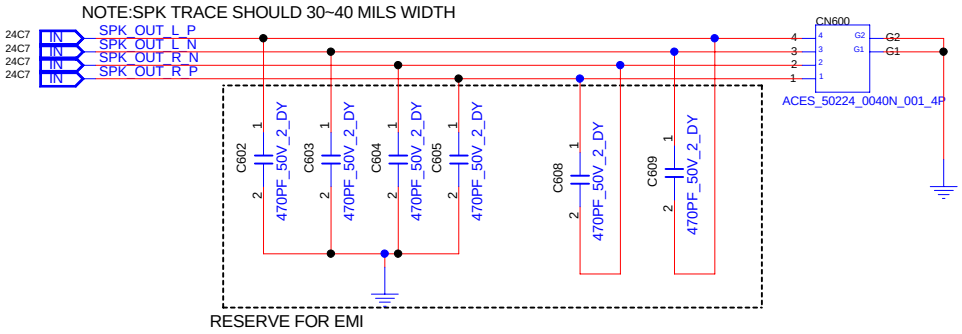
REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS

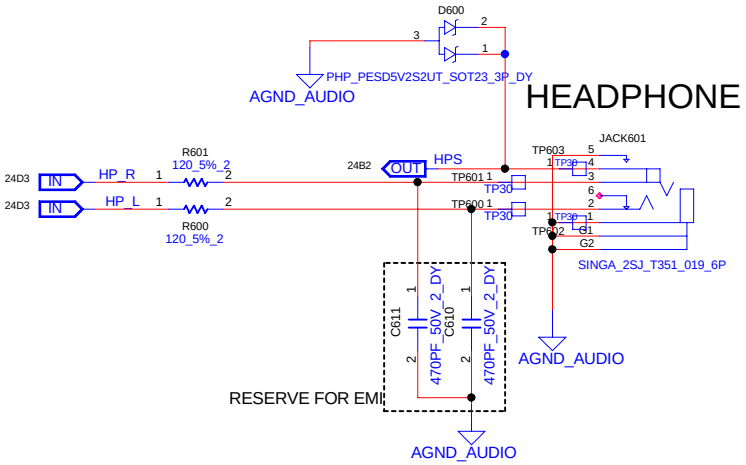
MICPHONE



INTERNAL SPEAKERS



HEADPHONE



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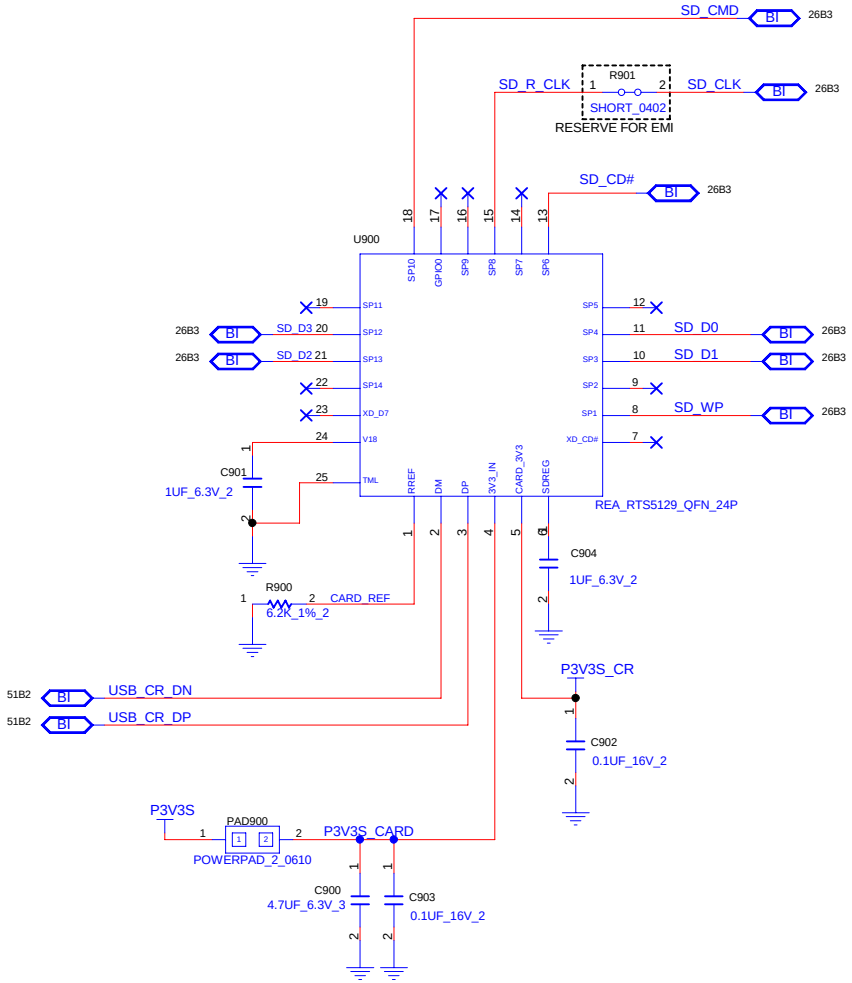
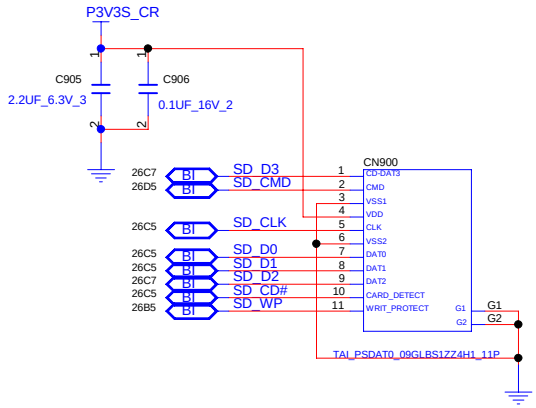
REFERNCE 900~999(CARDREADER)





INVENTEC

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A3	CS	1310xxxxx-0-0	X01

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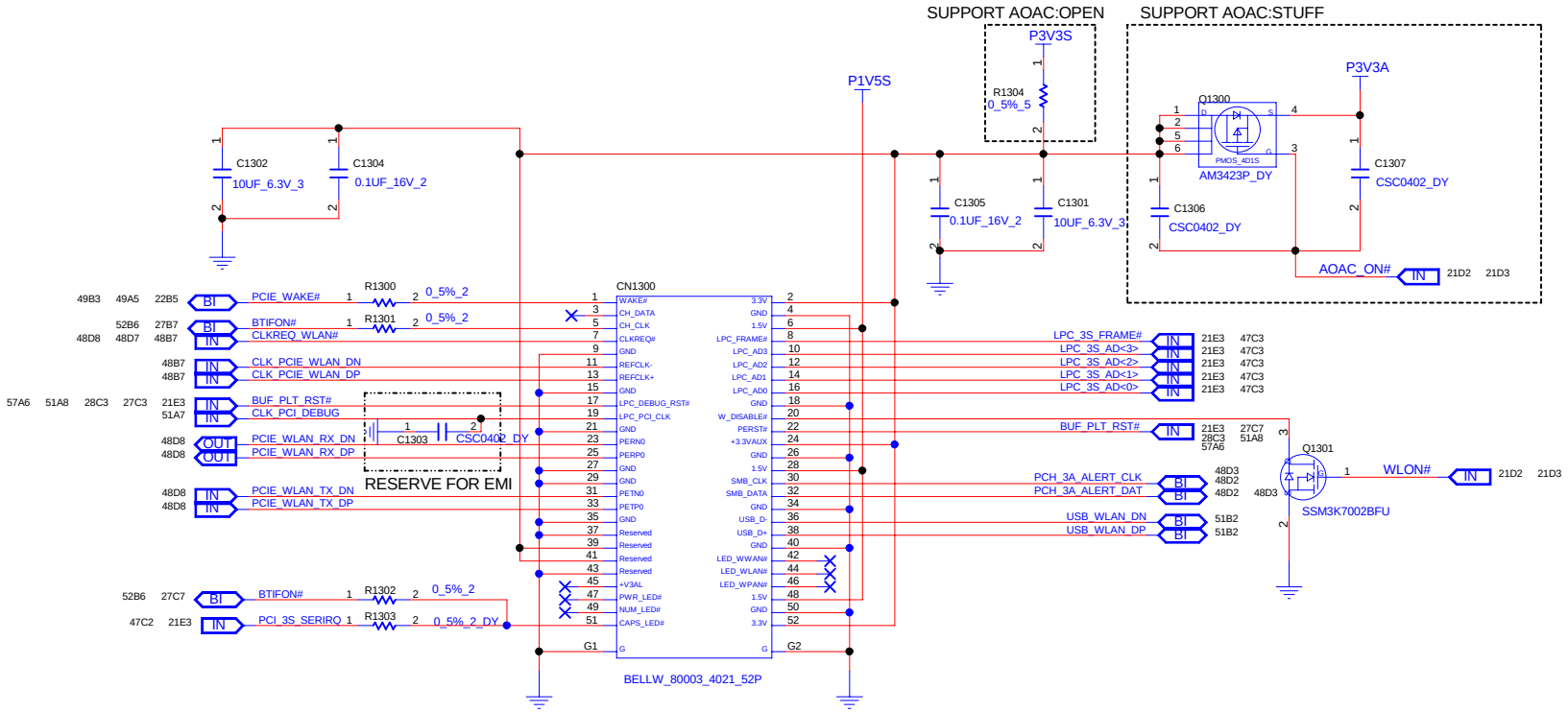
REFERENCE 1300~1349(WLAN)



MINI CARD 1(WLAN)

INVENTEC

TITLE
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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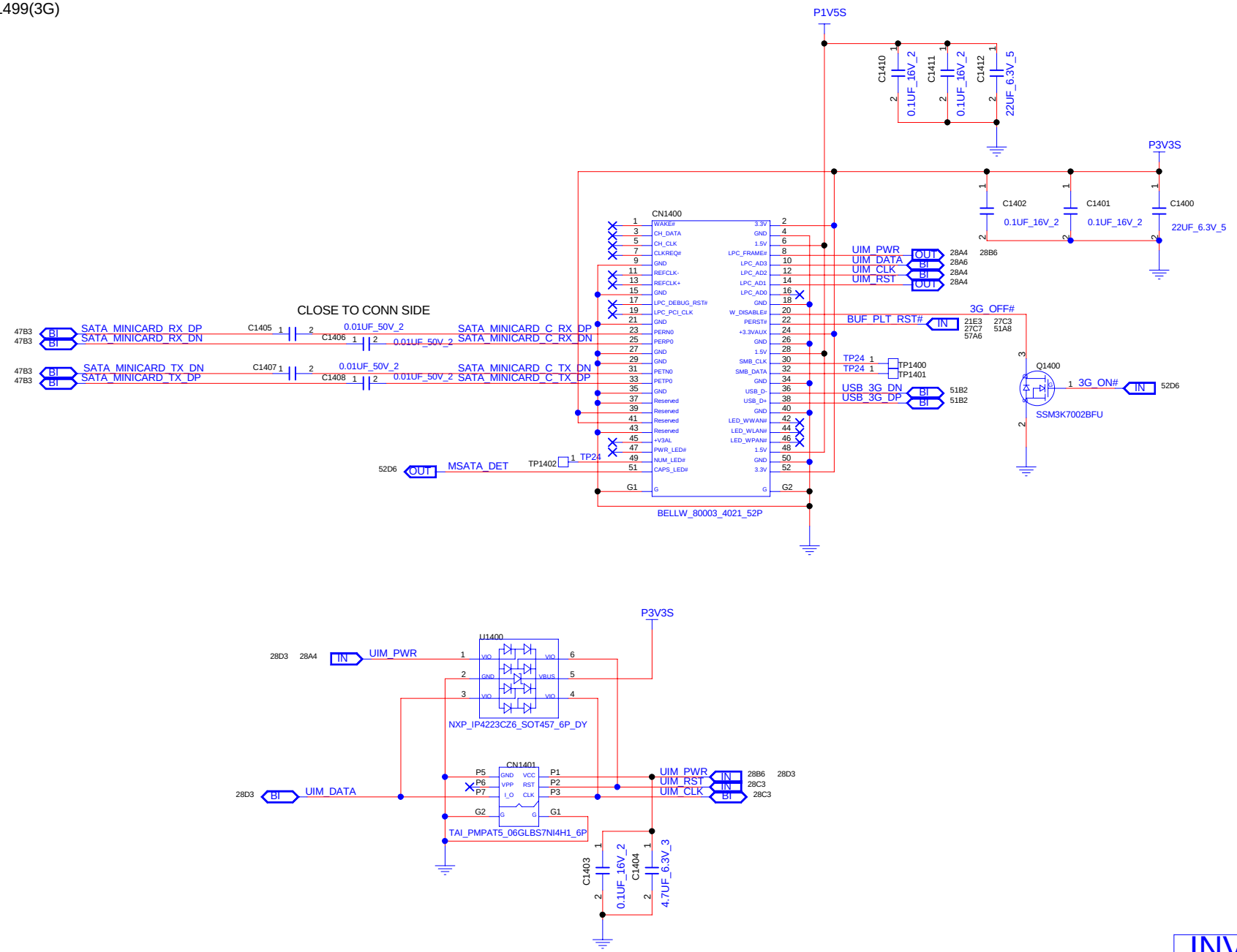
REFERENCE 1400~1499(3G)



INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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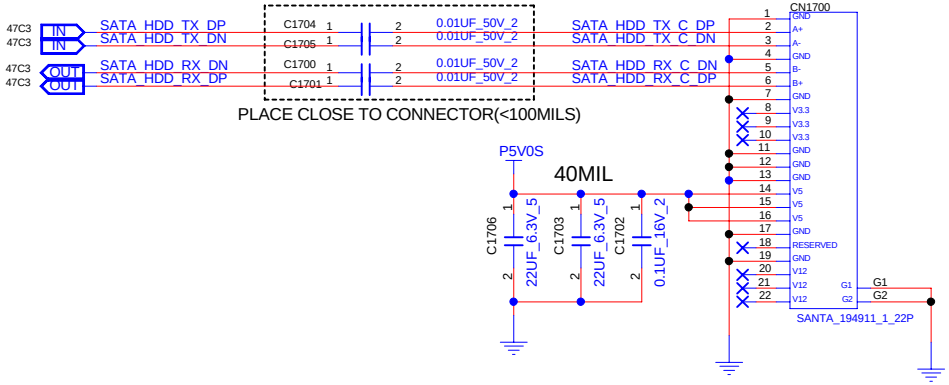
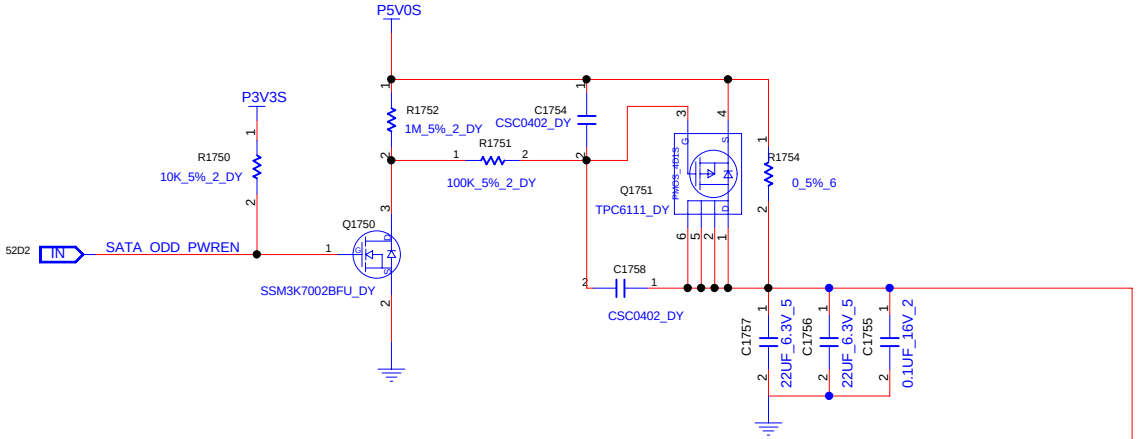
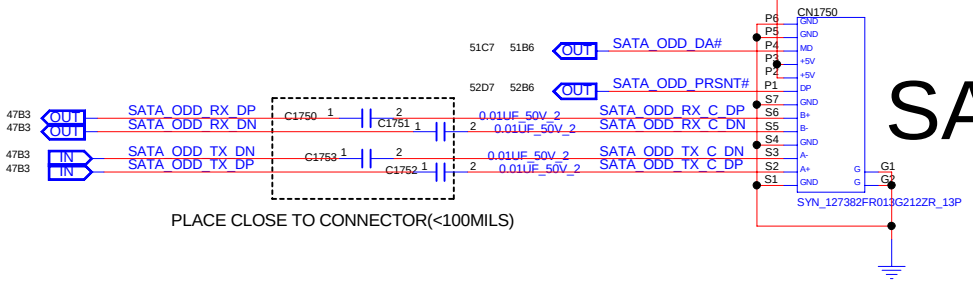
REFERENCE 1700~1749(HDD)
REFERENCE 1750~1799(ODD)

SATA HDD





SATA ODD



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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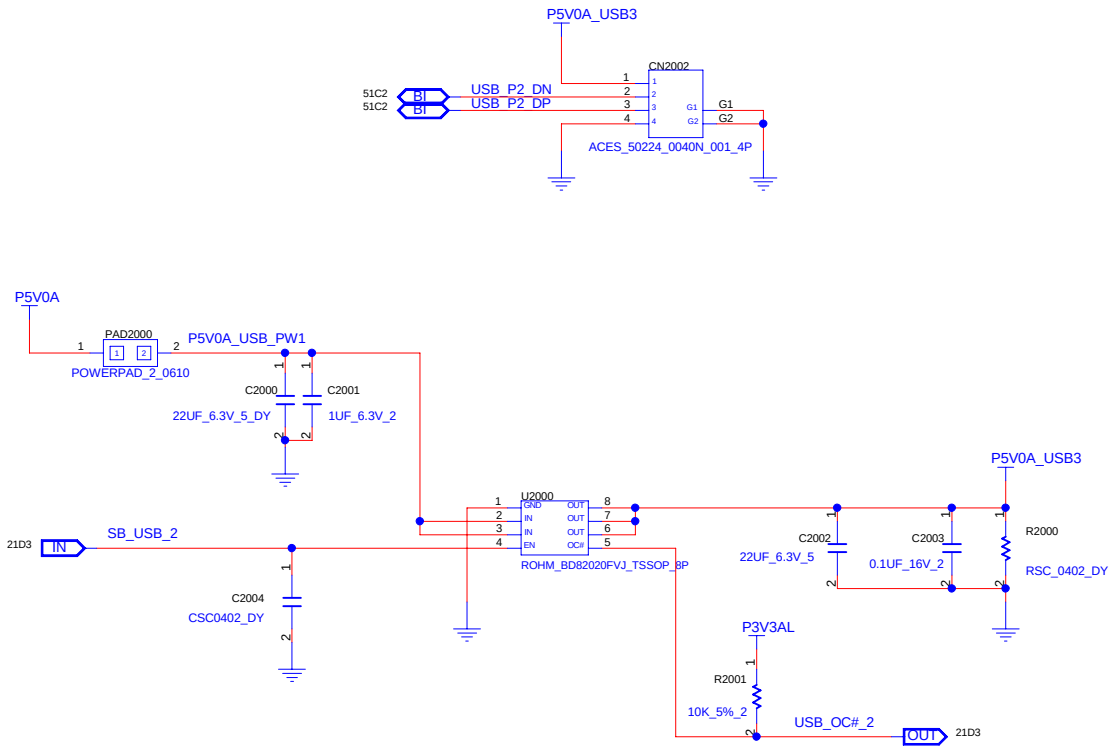
REFERENCE 2000~2099(USB)



INVENTEC

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SIZE	CODE	DOC.NUMBER	REV
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REFERENCE 2400~2499

REMOVE USB3.0 CONTROLLER IC

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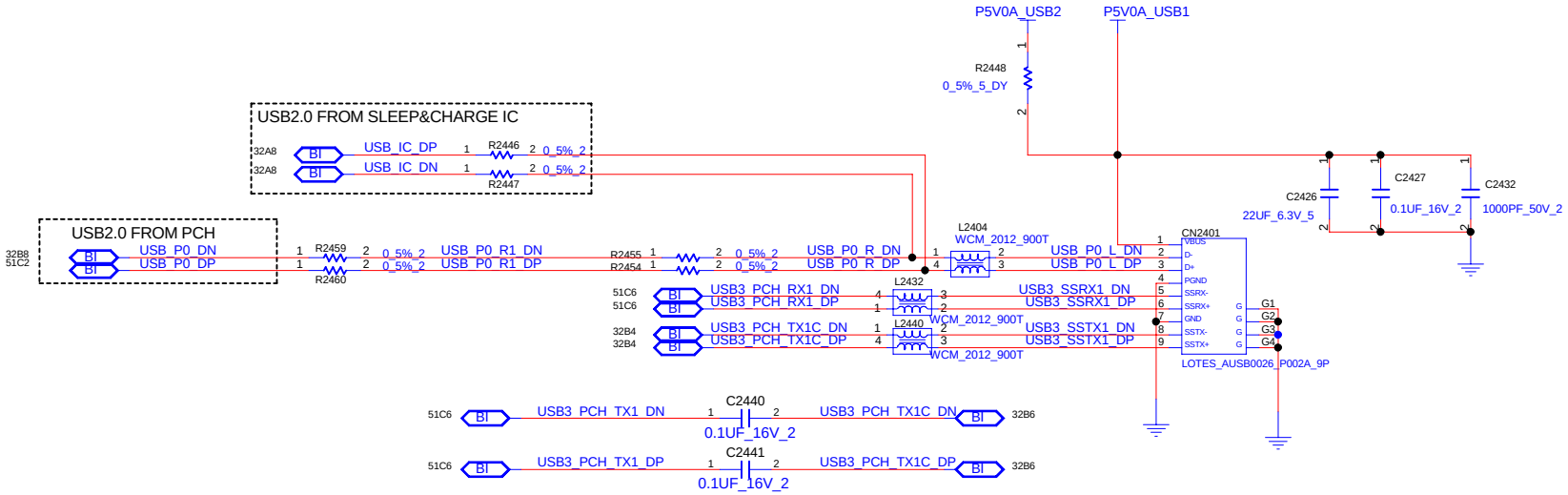

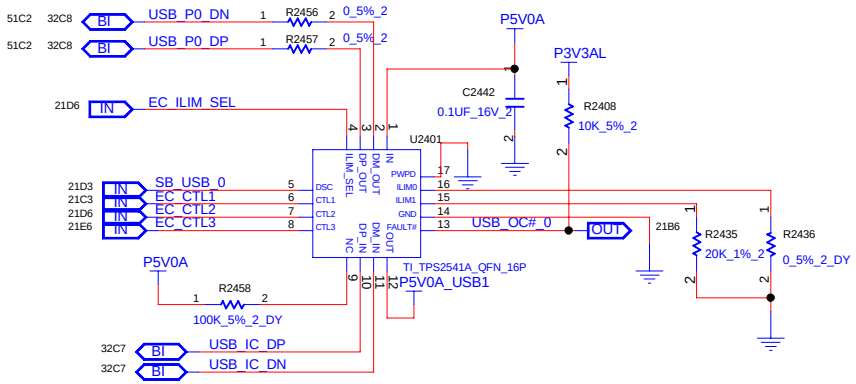

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table

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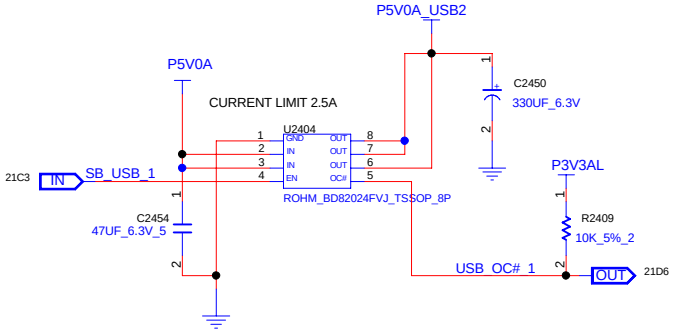
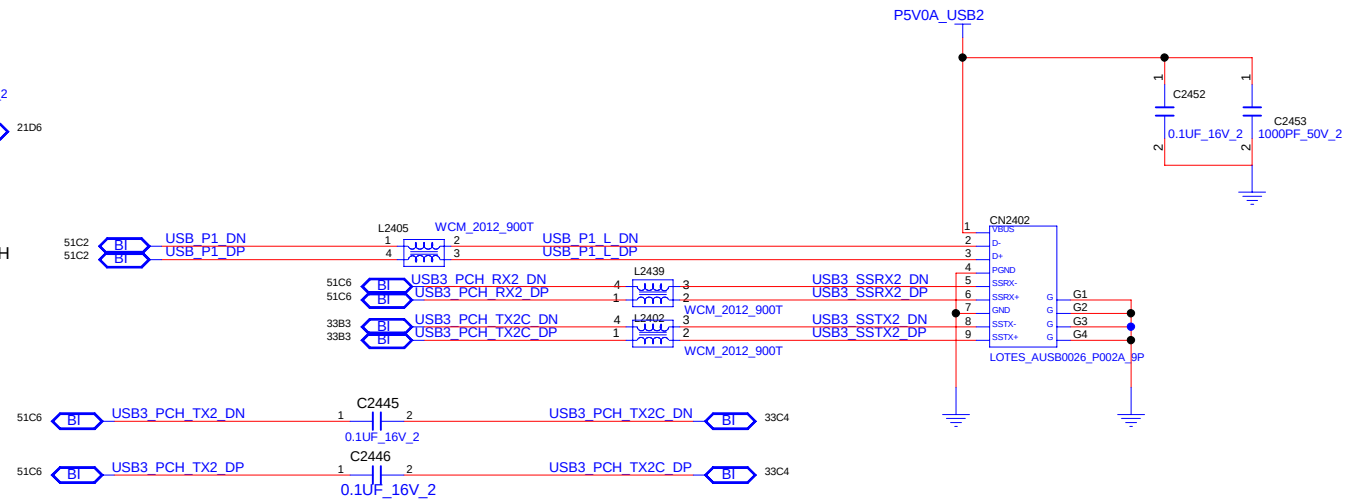
REFERENCE 2400~2499(USB3.0)

USB 3.0 CONNECTOR



USB2.0 FROM PCH



INVENTEC

TITLE
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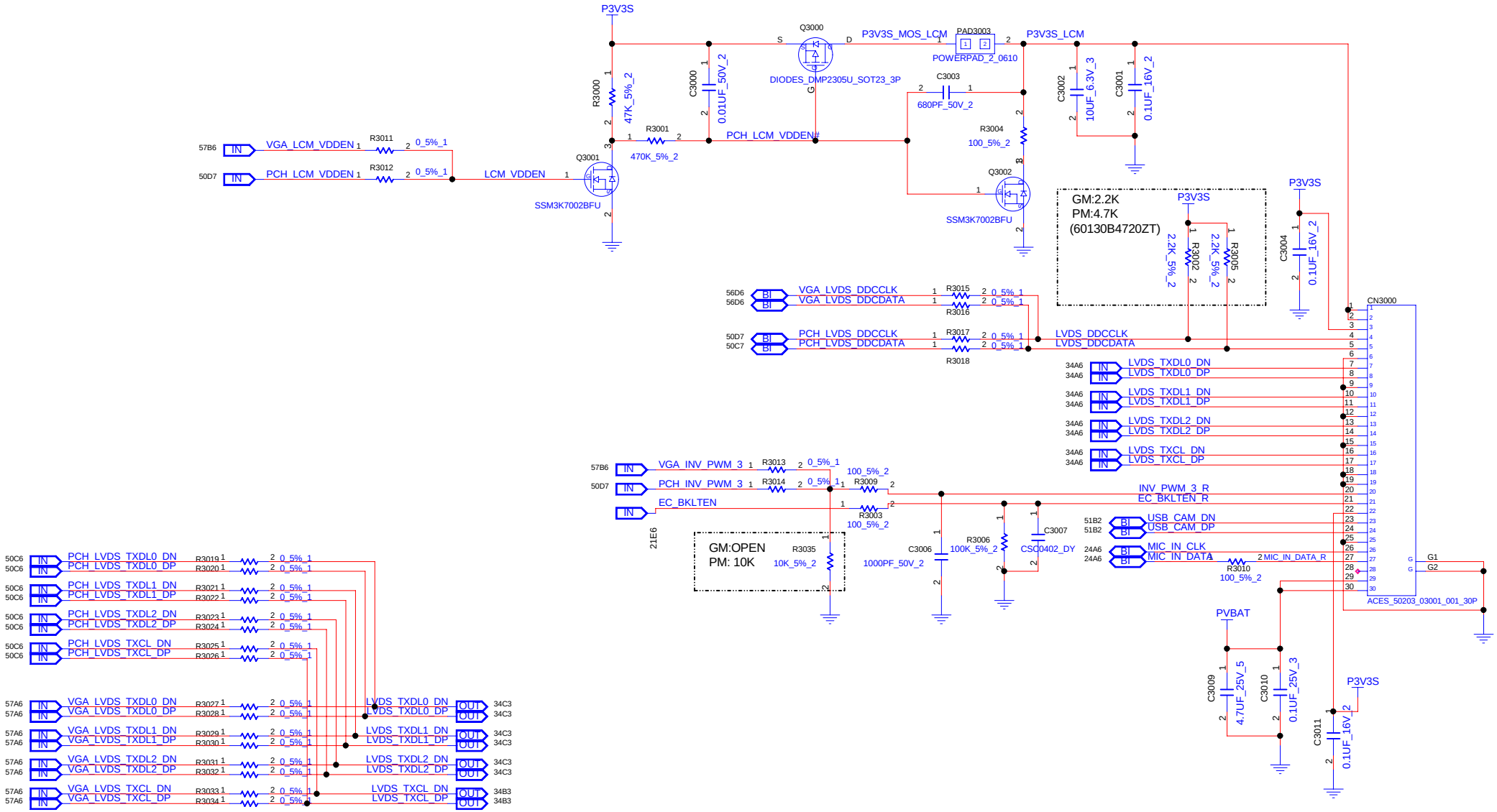
REFFERENCE 3000~3049(LCM)



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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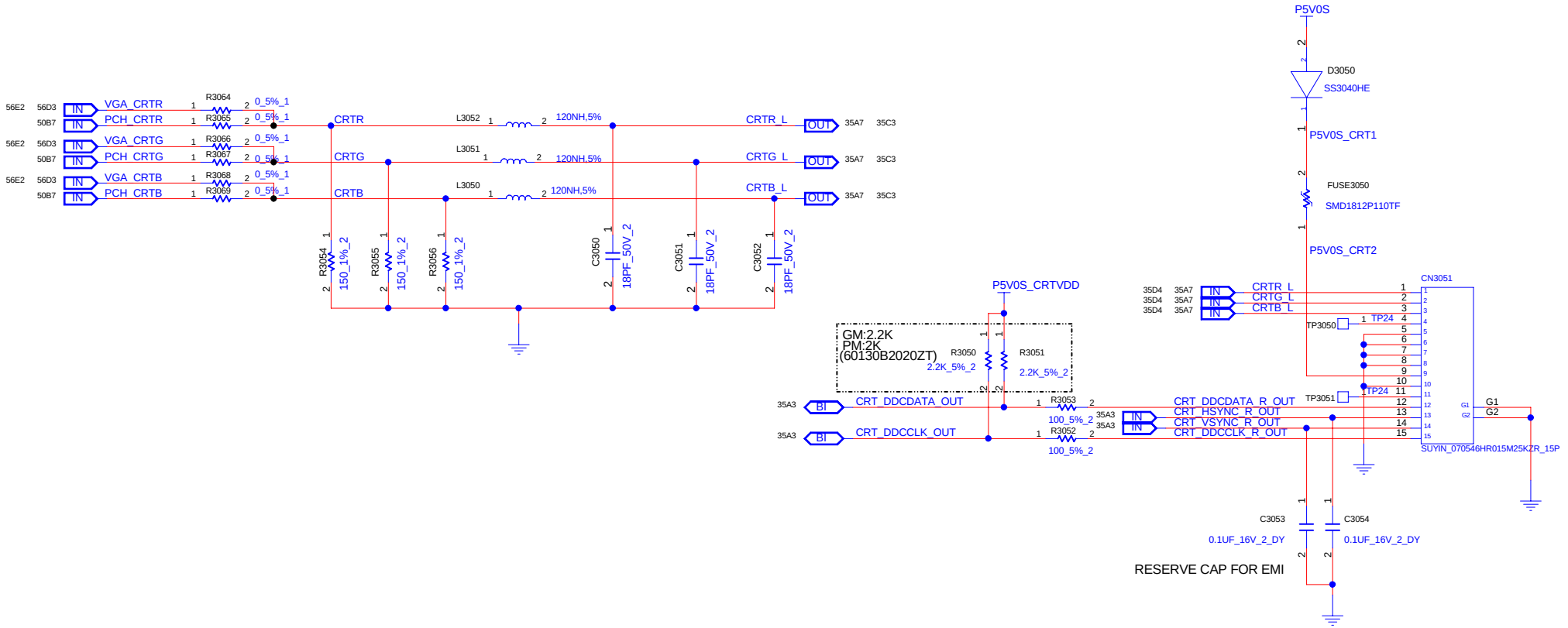
REFERENCE 3050~3099(CRT)



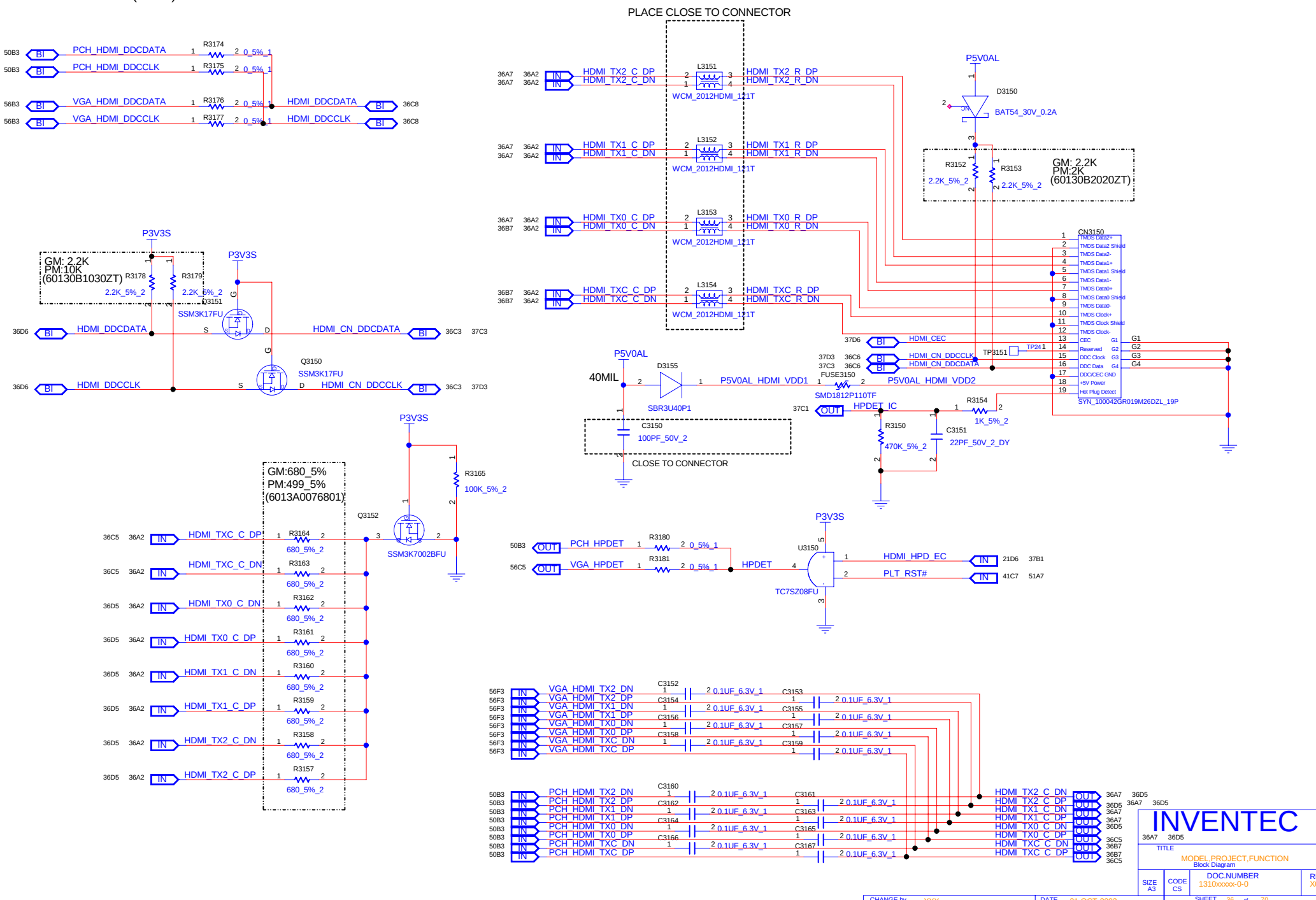
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 35 of 70

REFERENCE 3150~3199(HDMI)

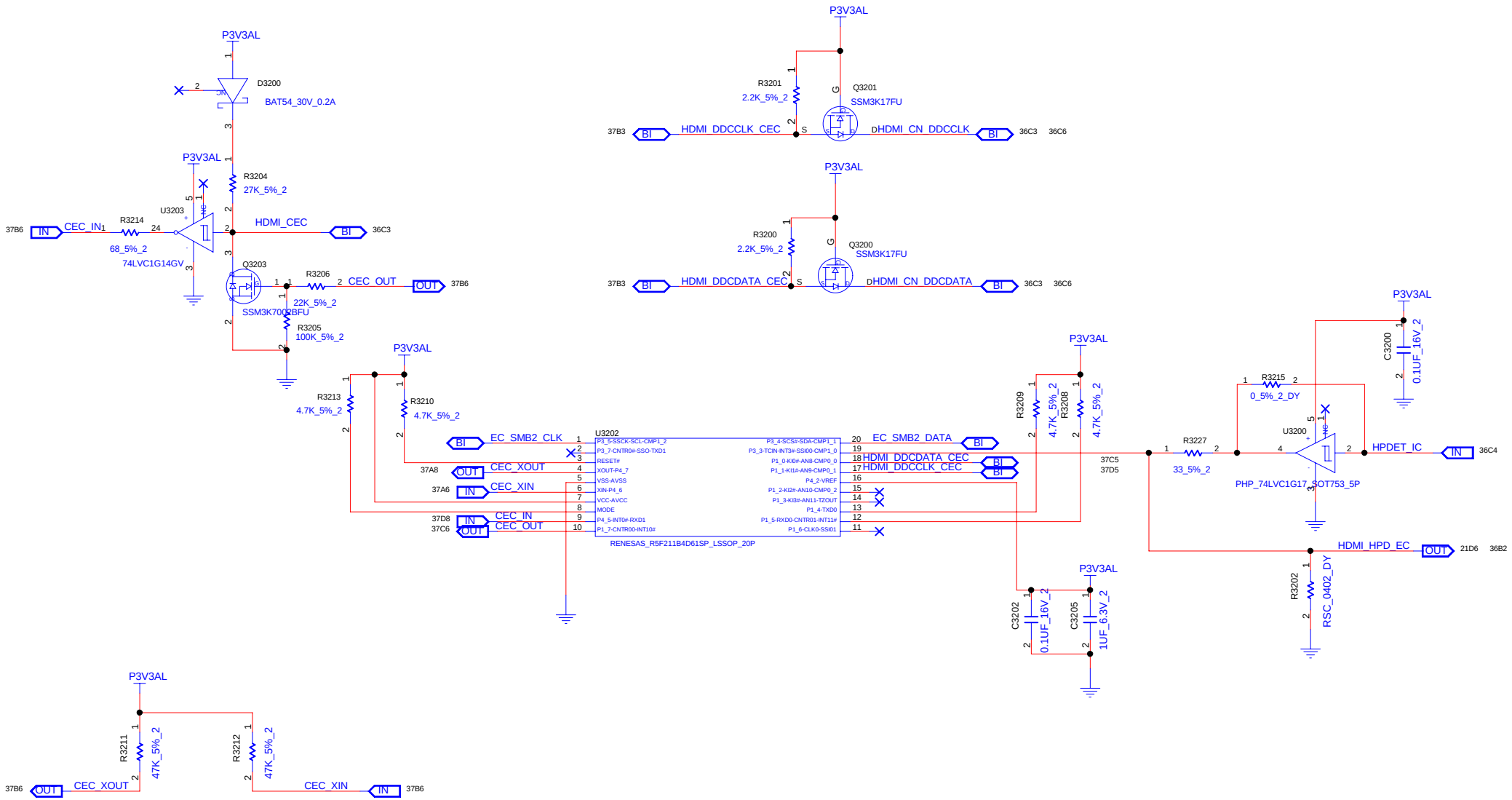


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 36 of 70



INVENTEC

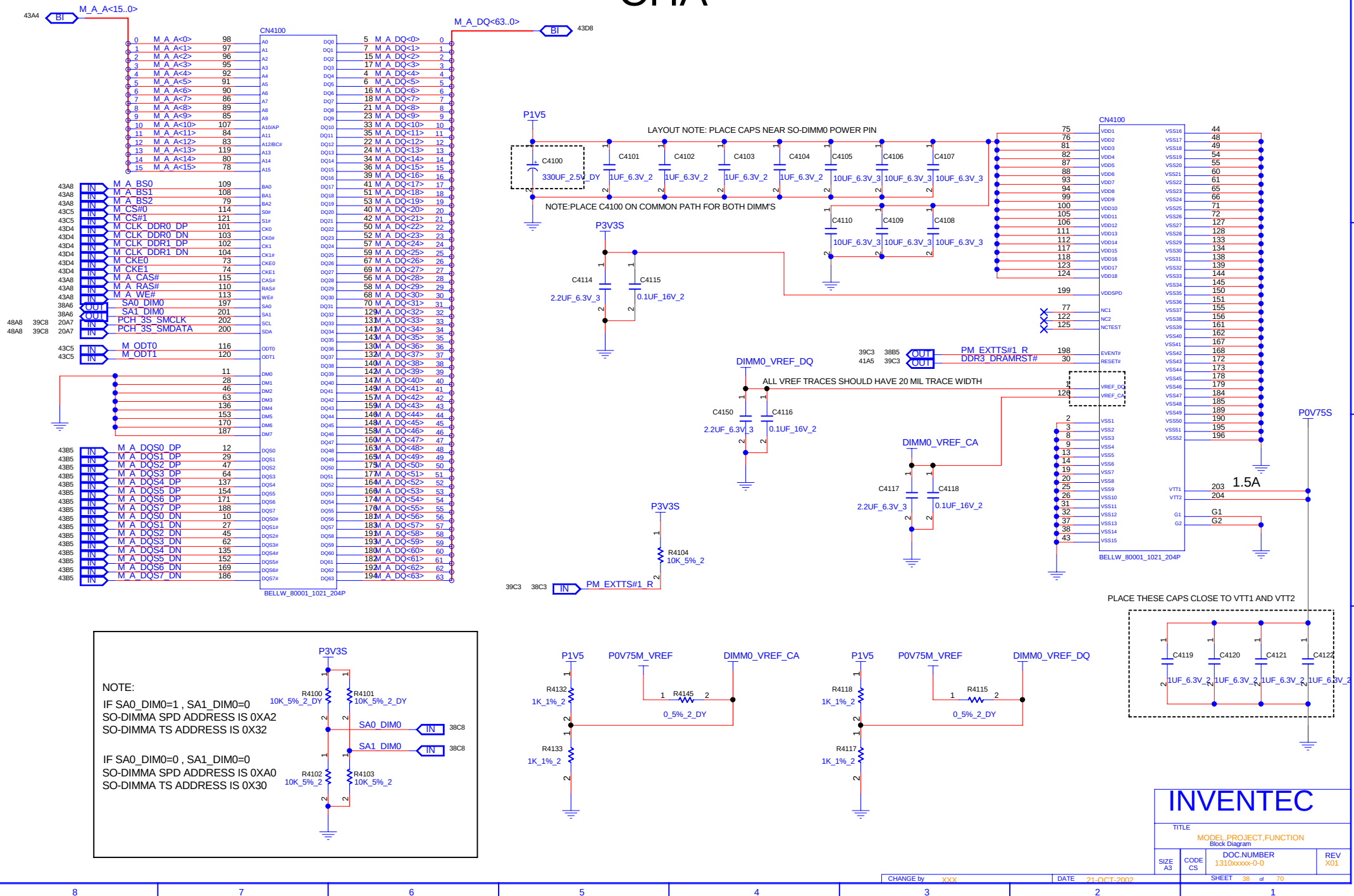
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 37 of 70

REFERENCE 4100~4299(DDR)

CHA



NOTE:

IF SA0_DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

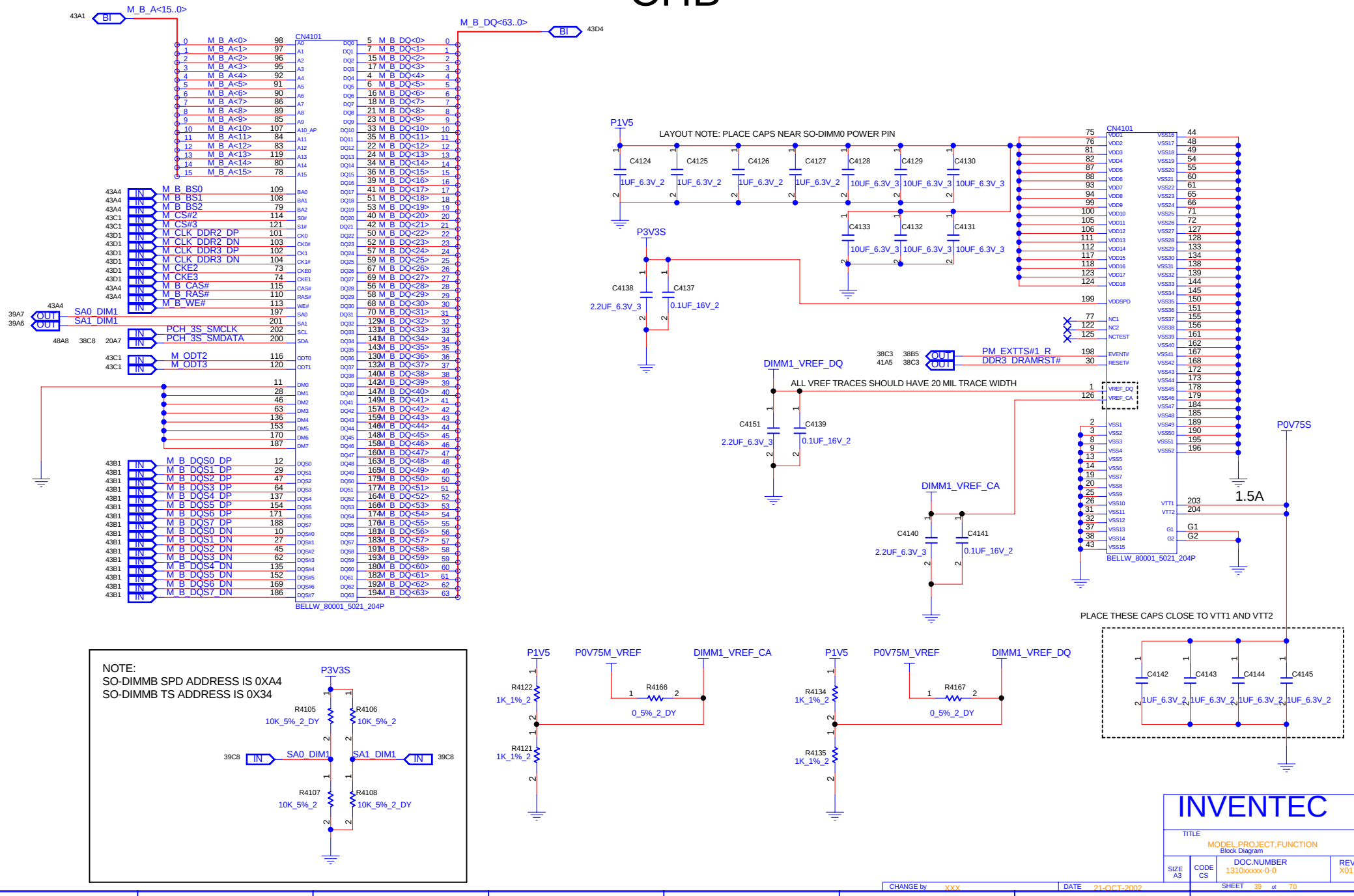
IF SA0_DIM0=0 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 38 of 70	

REFERENCE 4100~4299(DDR)

CHB



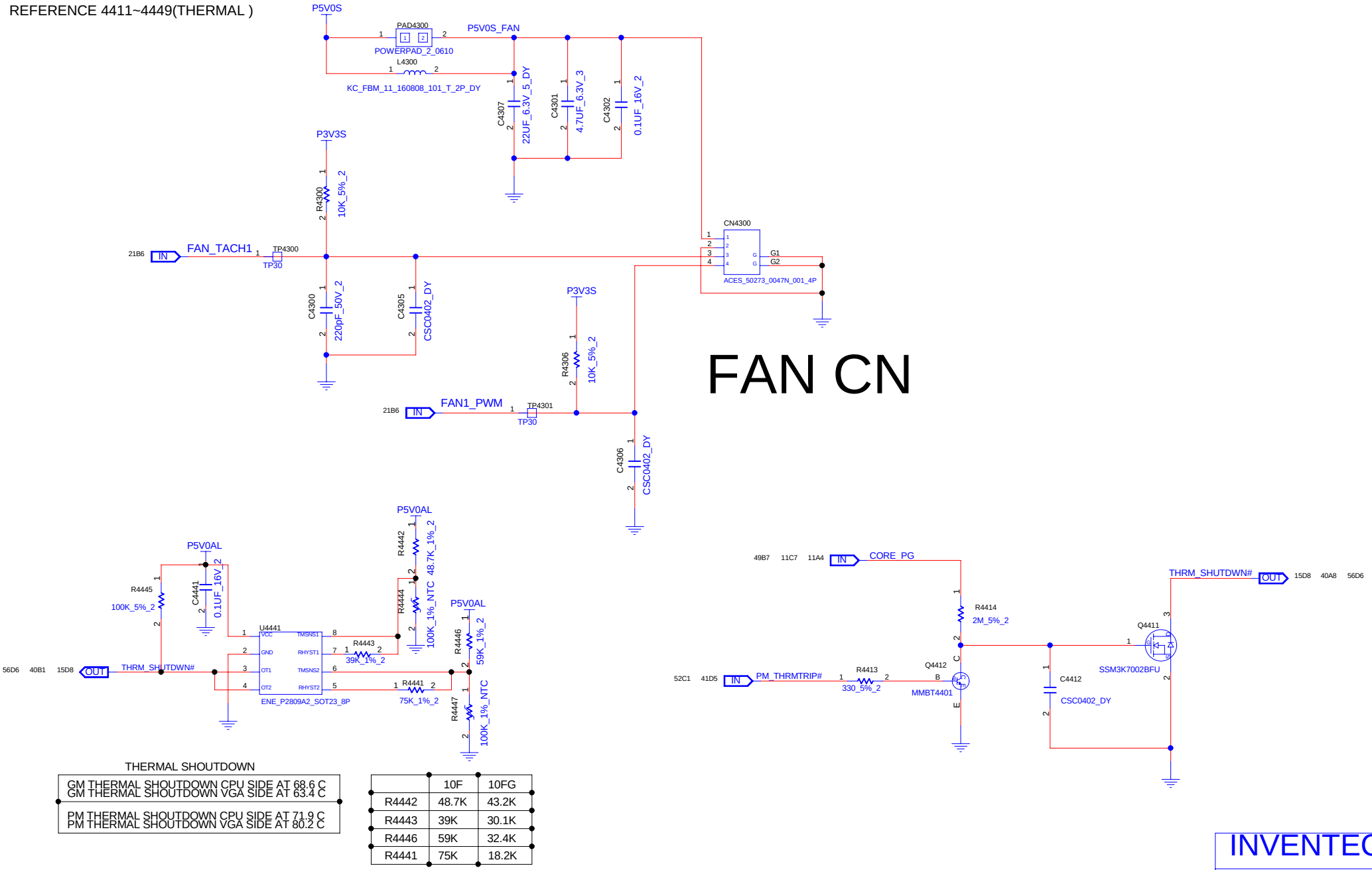
NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 39 of 70	

REFERENCE 4300~4349(FAN)

REFERENCE 4411~4449(THERMAL)



THERMAL SHOUTDOWN

GM THERMAL SHOUTDOWN CPU SIDE AT 68.6 C GM THERMAL SHOUTDOWN VGA SIDE AT 63.4 C
PM THERMAL SHOUTDOWN CPU SIDE AT 71.9 C PM THERMAL SHOUTDOWN VGA SIDE AT 80.2 C

	10F	10FG
R4442	48.7K	43.2K
R4443	39K	30.1K
R4446	59K	32.4K
R4441	75K	18.2K

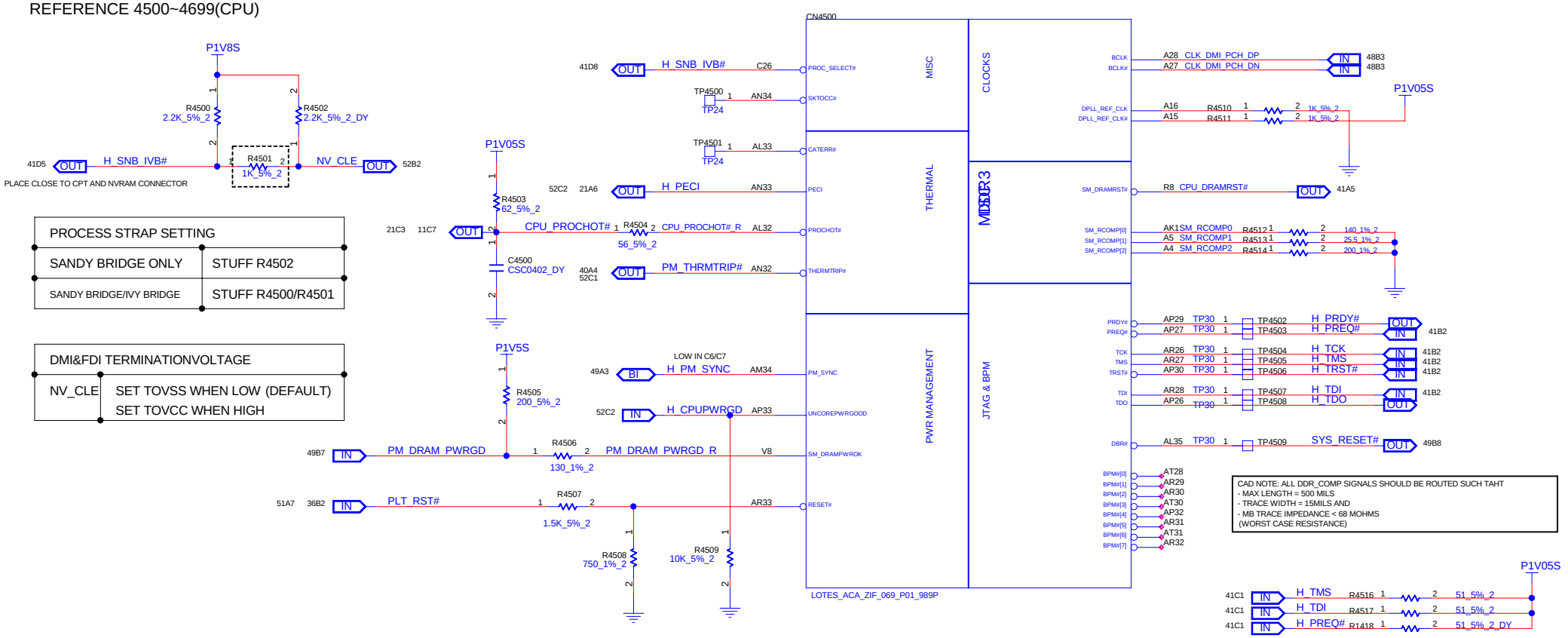
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

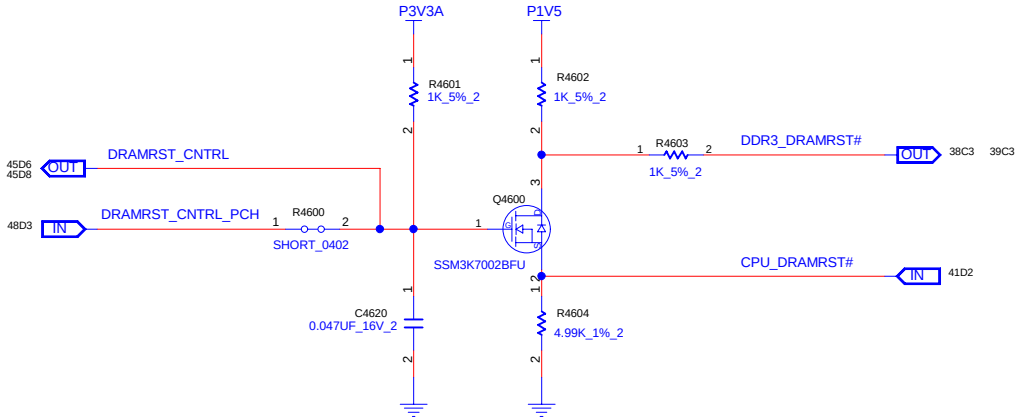
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 40 of 70

REFERENCE 4500~4699(CPU)



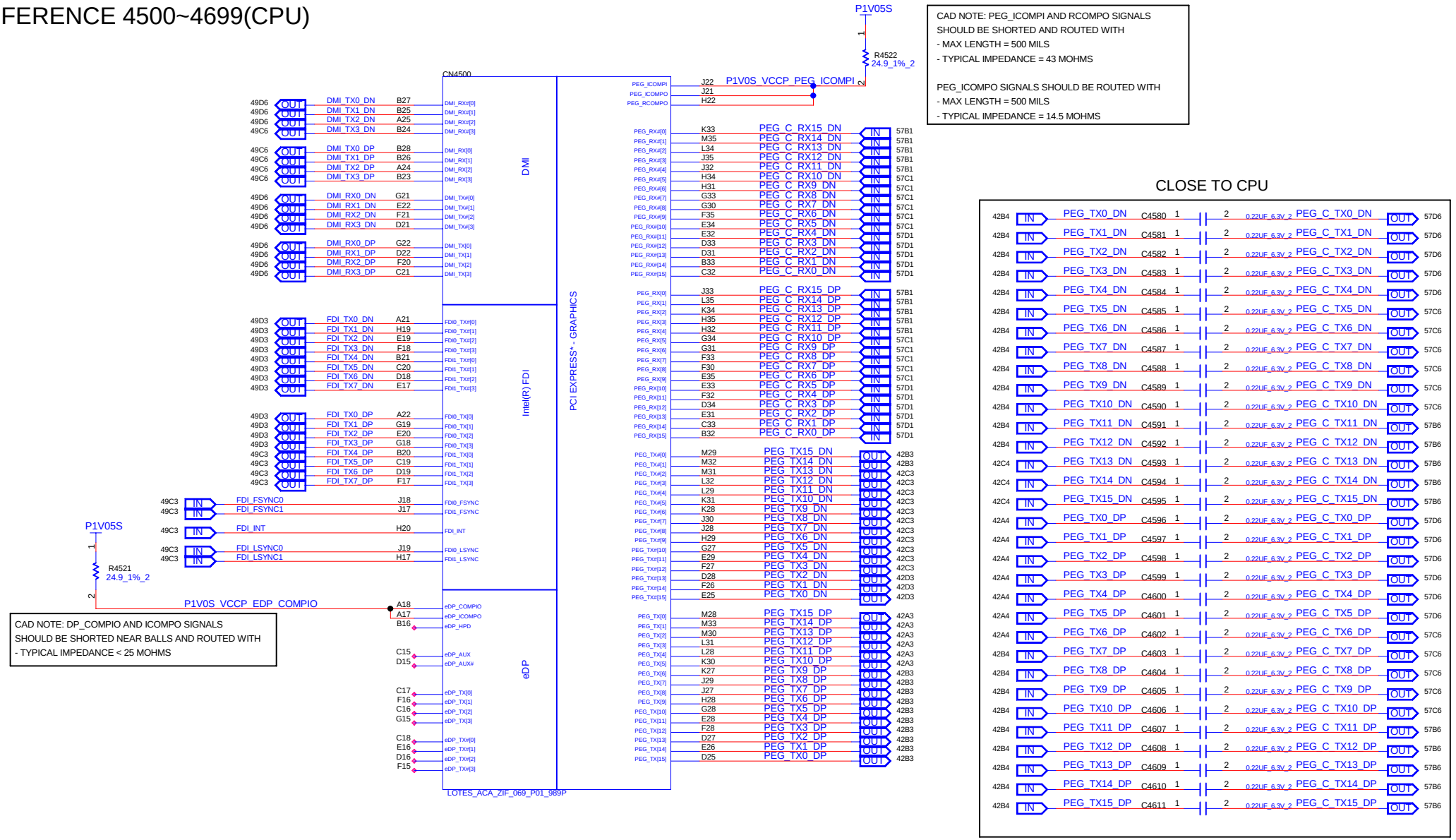
S3 CIRCUIT: DRAM_RST# TO MEMORY SHOULD BE HIGH DURING S3



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 41 of 70	

REFERENCE 4500~4699(CPU)



CAD NOTE: PEG_ICOMPI AND RCOMPO SIGNALS SHOULD BE SHORTED AND ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 43 MOHMS

PEG_ICOMPO SIGNALS SHOULD BE ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 14.5 MOHMS

CAD NOTE: DP_COMPIO AND ICOMPO SIGNALS SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH
- TYPICAL IMPEDANCE < 25 MOHMS

CLOSE TO CPU

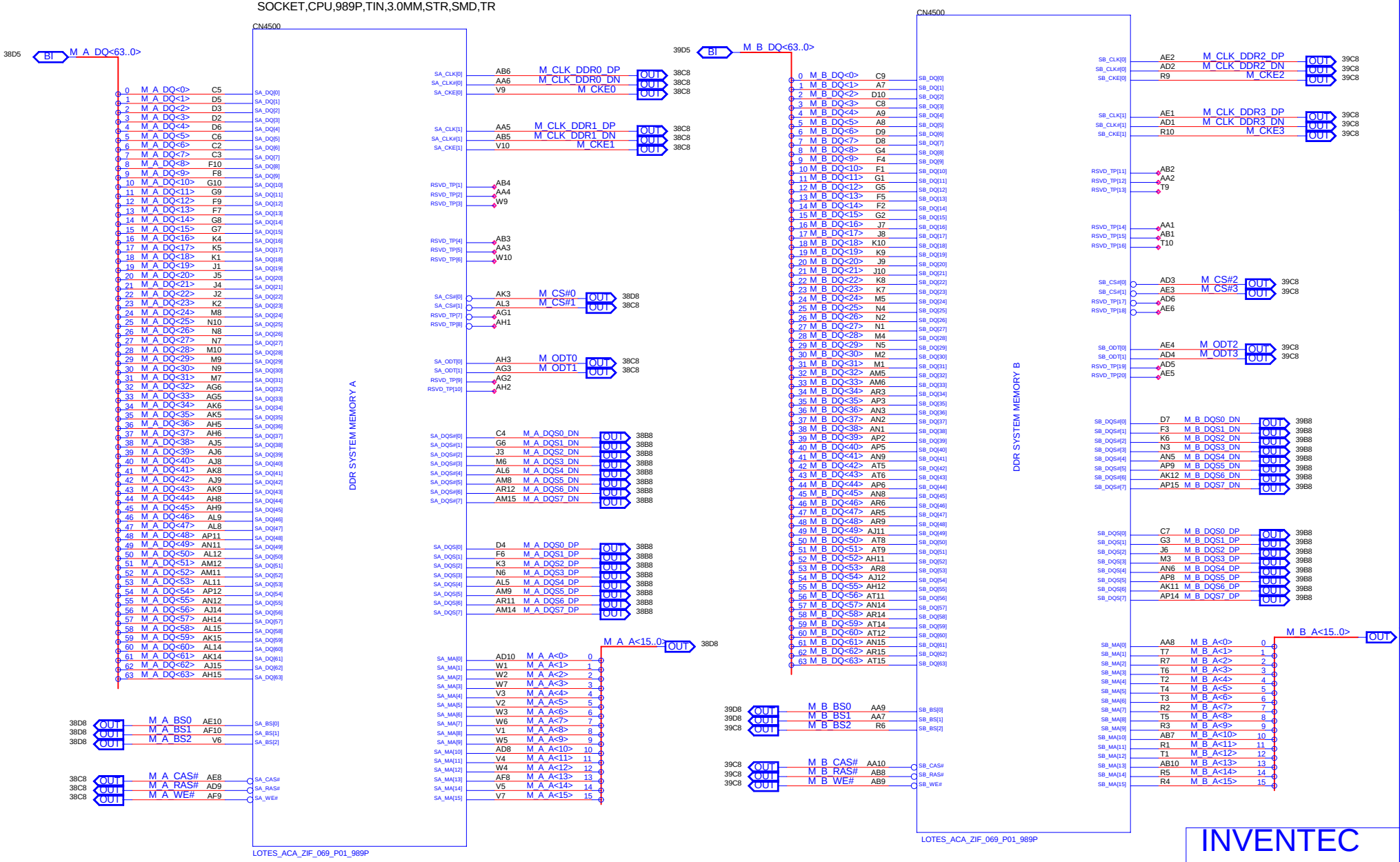
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 42 of 70

REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR



INVENTEC

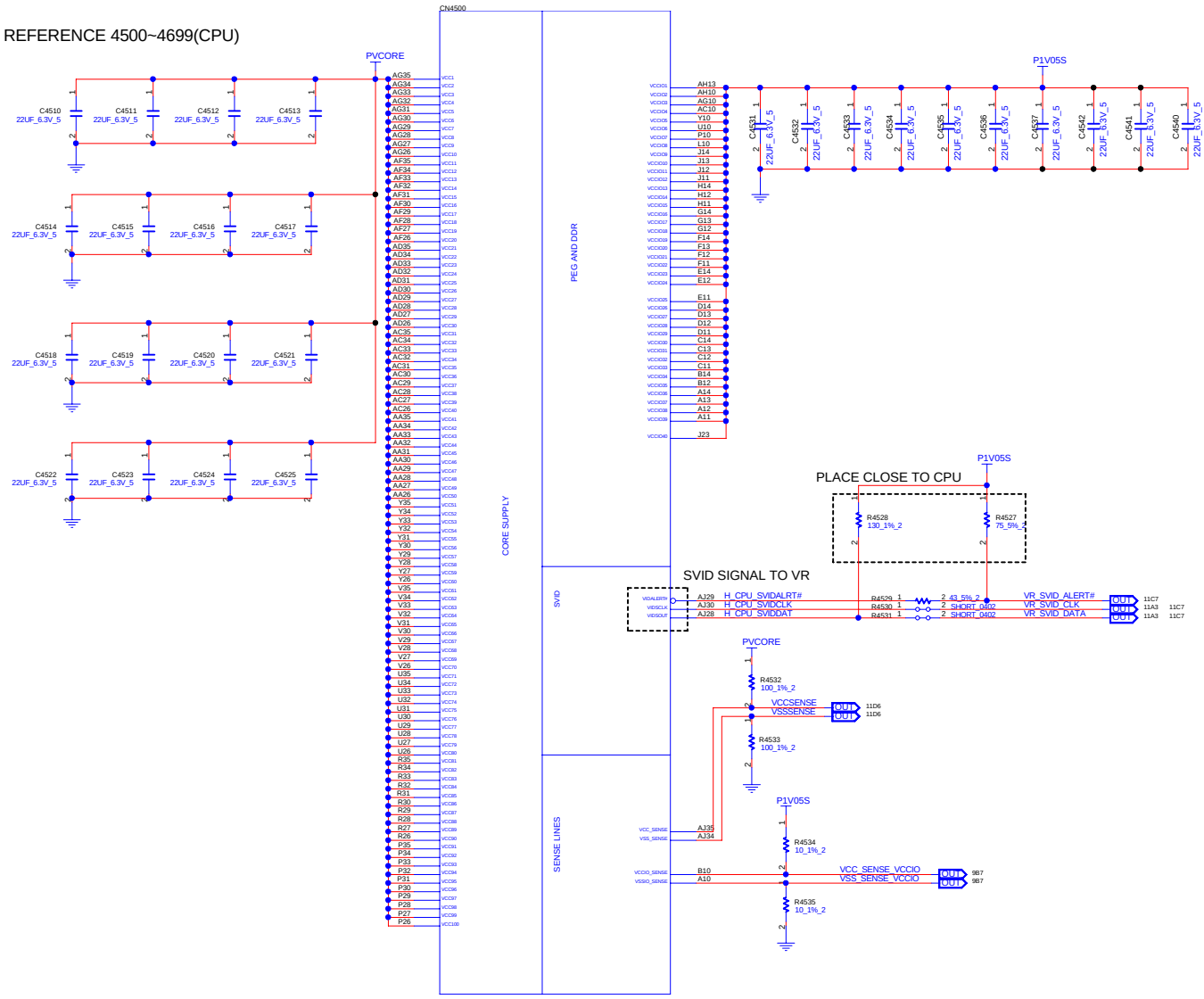
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 43 of 70

POWER

REFERENCE 4500~4699(CPU)



INVENTEC

TITLE: MODEL_PROJECT_FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 44 of 70

PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:
ROUTE WITH MIN. TRACE WIDTH OF 10 MILS

DIMM0_VREF_DQ — R4570 0_5%_2_DY — 46C4 IN CPUDDR_WR_VREF1 — Q4501 AM2302N — 45D6 41A8 IN DRAMRST_CNTRL

DIMM1_VREF_DQ — R4572 0_5%_2_DY — 46C4 IN CPUDDR_WR_VREF2 — Q4502 AM2302N — 45D8 41A8 IN DRAMRST_CNTRL

POWER

P0V75M_VREF — Q4500 AM2302N — P0V75M_VREF_H — R4541 100K_5%_2

49A1 21D6 14D2 14B8 14A6 13A2 13D2 IN SLP_S3#_3R — R4538 SHORT_0402

PVAXG — C4578 470PF_50V_2

PVAXG — C4651 22UF_6.3V_5 — C4545 22UF_6.3V_5 — C4546 22UF_6.3V_5 — C4547 22UF_6.3V_5 — C4548 22UF_6.3V_5 — C4549 22UF_6.3V_5 — C4550 22UF_6.3V_5

CN4500

SENSE LINES
VAXG_SENSE — AK35 GFX_VCC_SENSE — R4539 10_1%_2 — OUT 11B8
VSSAXG_SENSE — AK34 GFX_VSS_SENSE — R4540 10_1%_2 — OUT 11B8

VREF
P0V75M_VREF_H — SM_VREF — AL1

NOTE : DDR_WR_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE

DDR3 -1.5V RAILS
VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

5A — P1V5S — C4567 10UF_6.3V_3 — C4568 10UF_6.3V_3 — C4569 10UF_6.3V_3 — C4570 10UF_6.3V_3 — C4571 10UF_6.3V_3 — C4572 10UF_6.3V_3 — C4573 220UF_2.5V

SA RAIL
VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

PVSA — C4574 10UF_6.3V_3 — C4575 10UF_6.3V_3 — C4576 10UF_6.3V_3 — C4577 100UF_6.3V

PVSA — R4544 100_5%_2 — VCCSA_SENSE H23 — OUT 10C4

MISC
FC_C22 C22, VCCSA_VID1 C24 — VCCSA_VID0 OUT 10B4, VCCSA_VID1 OUT 10B4
R4556 1K_5%_2 — R4547 1K_5%_2

GRAPHICS
VAXG1 AT24, VAXG2 AT23, VAXG3 AT21, VAXG4 AT20, VAXG5 AT18, VAXG6 AT17, VAXG7 AR24, VAXG8 AR23, VAXG9 AR21, VAXG10 AR20, VAXG11 AR18, VAXG12 AR17, VAXG13 AP24, VAXG14 AP23, VAXG15 AP21, VAXG16 AP20, VAXG17 AP18, VAXG18 AP17, VAXG19 AN24, VAXG20 AN23, VAXG21 AN21, VAXG22 AN20, VAXG23 AN18, VAXG24 AN17, VAXG25 AM24, VAXG26 AM23, VAXG27 AM21, VAXG28 AM20, VAXG29 AM18, VAXG30 AM17, VAXG31 AL24, VAXG32 AL23, VAXG33 AL21, VAXG34 AL20, VAXG35 AL18, VAXG36 AL17, VAXG37 AK24, VAXG38 AK23, VAXG39 AK21, VAXG40 AK20, VAXG41 AK18, VAXG42 AK17, VAXG43 AJ24, VAXG44 AJ23, VAXG45 AJ21, VAXG46 AJ20, VAXG47 AJ18, VAXG48 AJ17, VAXG49 AH24, VAXG50 AH23, VAXG51 AH21, VAXG52 AH20, VAXG53 AH18, VAXG54 AH17

1.8V RAIL
VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

P1V8S — L4500 MPZ1608S221AT — 1.2A — P1V8S_VCCPLL — C4562 10UF_6.3V_3 — C4563 1UF_6.3V_2 — C4564 1UF_6.3V_2 — C4565 22UF_6.3V_5

LOTES_ACA_ZIF_069_P01_989P

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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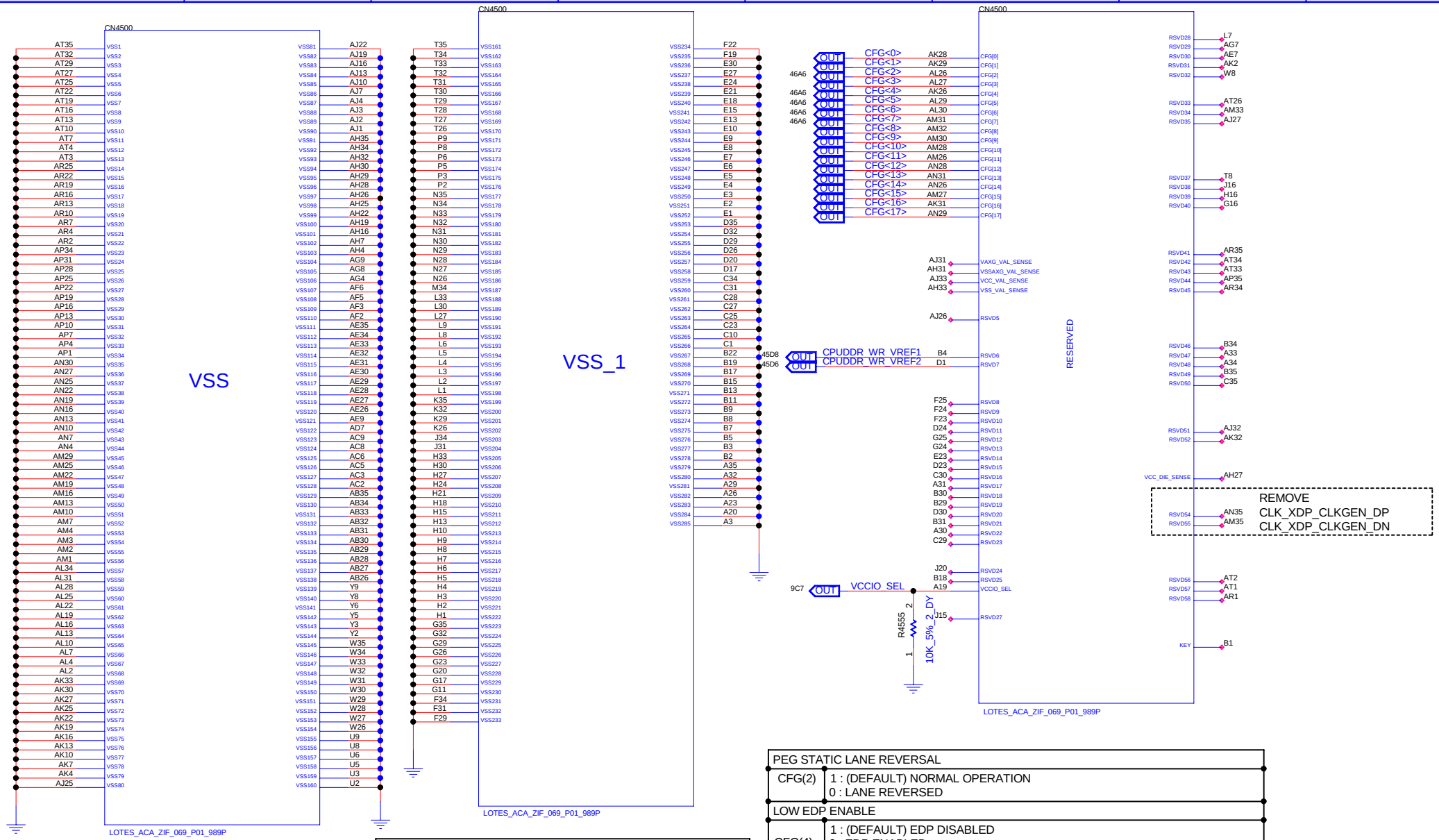

PEG STATIC LANE REVERSAL	
CFG(2)	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED
LOW EDP ENABLE	
CFG(4)	1 : (DEFAULT) EDP DISABLED 0 : EDP ENABLED
PEG DEFER TRAINING	
CFG(7)	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING
PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11 : (DEFAULT) X16 - DEVICE 1 FUNCTION AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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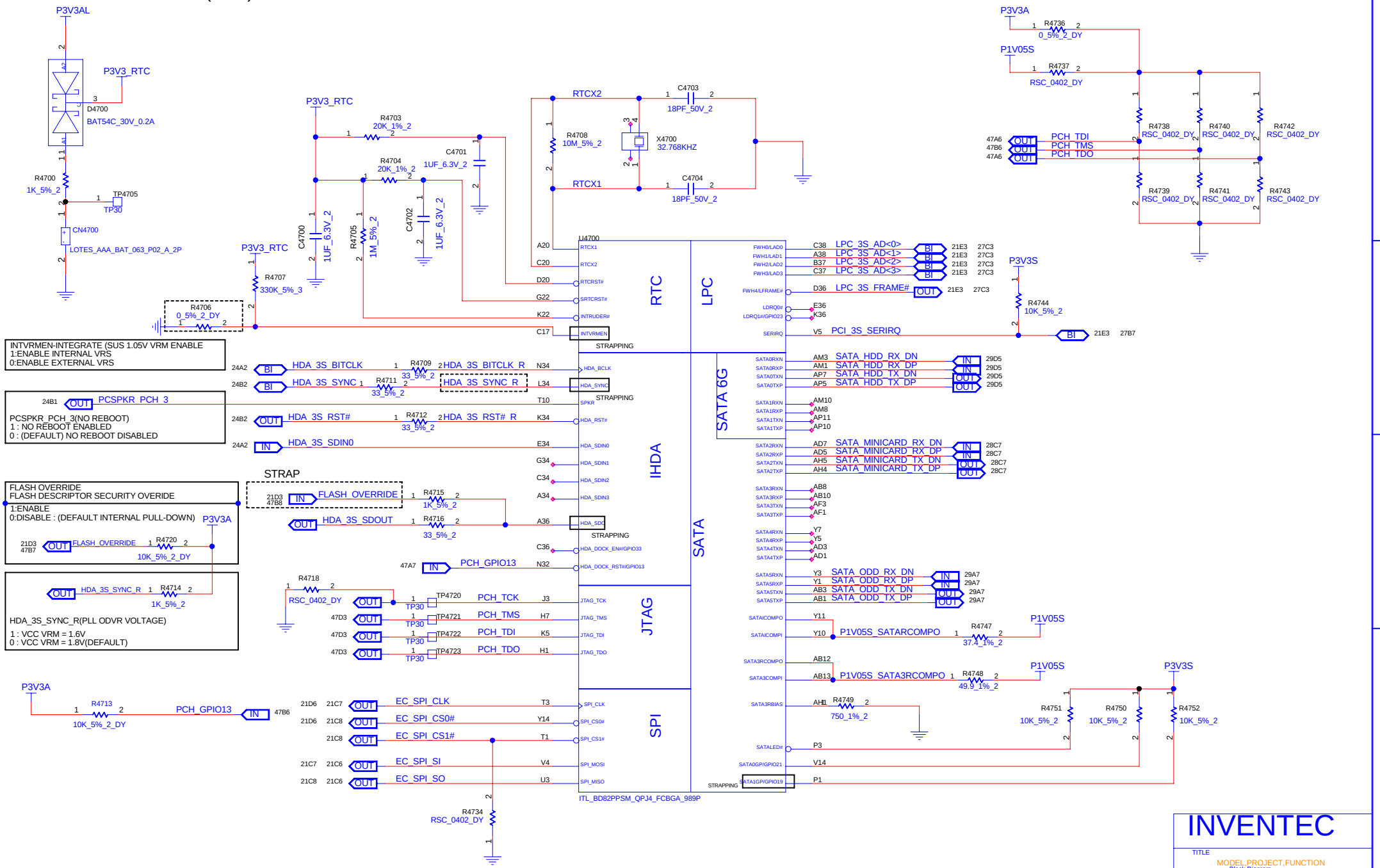
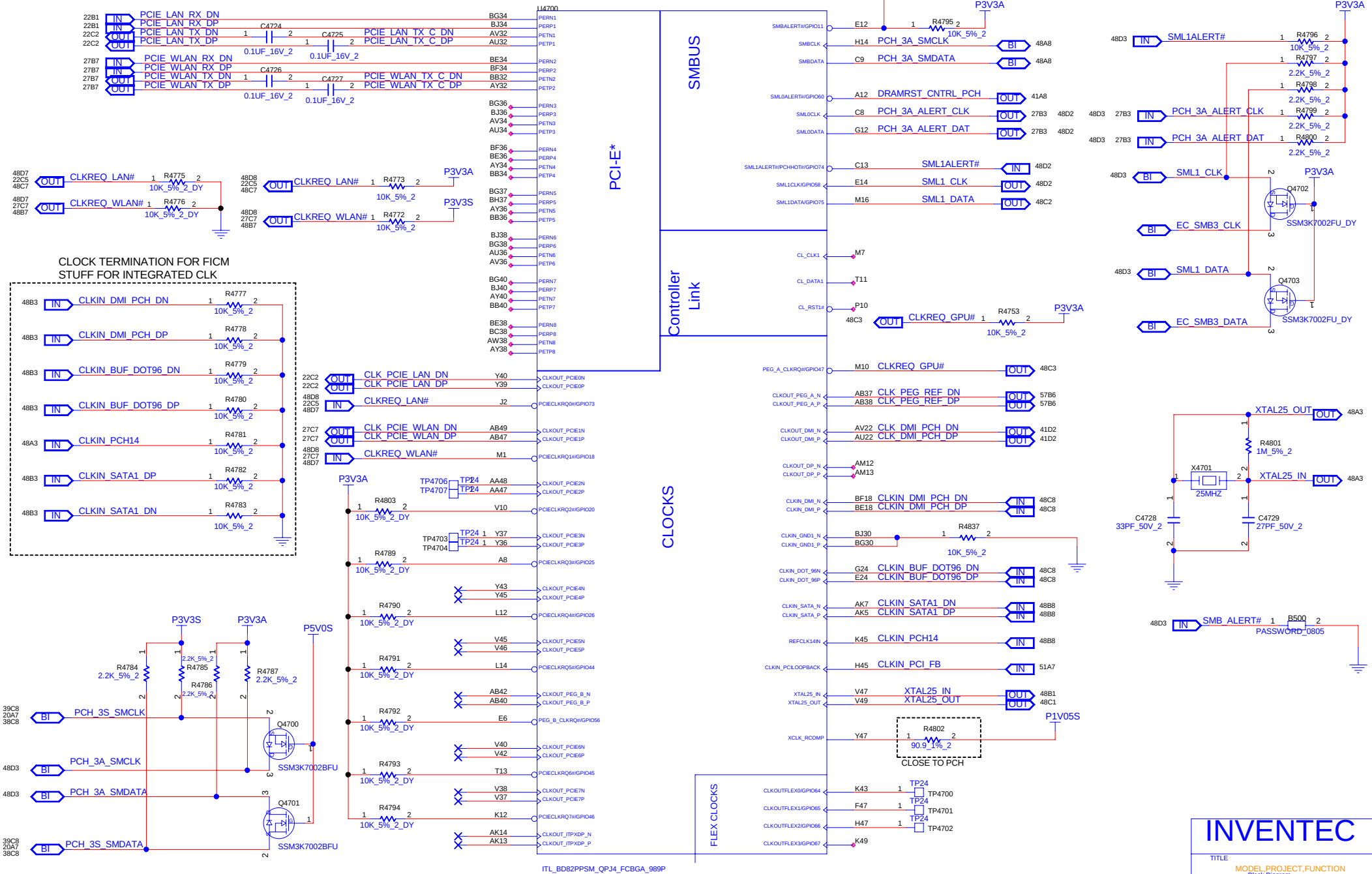
REFERENCE 4700~4949(PCH)



REFERENCE 4700~4949(PCH)



CHANGE by	XXX	DATE	21-OCT-2002

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 48 of 70			

DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE
HIGH-ENABLED(DEFAULT)
LOW-DISABLED

U4700

DMI_RX0_DN BC24
DMI_RX1_DN BE20
DMI_RX2_DN BG18
DMI_RX3_DN BG20
DMI_RX0_DP BE24
DMI_RX1_DP BC20
DMI_RX2_DP BJ18
DMI_RX3_DP BJ20
DMI_TX0_DN AW24
DMI_TX1_DN AW20
DMI_TX2_DN BB18
DMI_TX3_DN AV18
DMI_TX0_DP AY24
DMI_TX1_DP AY20
DMI_TX2_DP AY18
DMI_TX3_DP AU18
BJ24 DMI_ZCOMP
BG25 DMI_IRCOMP
BH21 DMI2RBIAS

R4812 49.9_1%_2
R4814 750_1%_2

FDI_TX0_DN BJ14
FDI_TX1_DN AY14
FDI_TX2_DN BE14
FDI_TX3_DN BH13
FDI_TX4_DN BC12
FDI_TX5_DN BJ12
FDI_TX6_DN BG10
FDI_TX7_DN BG9
FDI_TX0_DP BG14
FDI_TX1_DP BB14
FDI_TX2_DP BF14
FDI_TX3_DP BG13
FDI_TX4_DP BE12
FDI_TX5_DP BG12
FDI_TX6_DP BJ10
FDI_TX7_DP BH9
AW16 FDI_INT
AV12 FDI_FSYNC0
BC10 FDI_FSYNC1
AV14 FDI_LSYNC0
BB10 FDI_LSYNC1

DMI
FDI
System Power Management
ITL_BD82PPSM_QPJ4_FCBGA_989P

STRAPPING
DSWVRMEN A18
DPWROK E22
WAKE# B9
CLKRUN#/GPIO32 N3
SUS_STAT#/GPIO61 G8
SUSCLK/GPIO62 N14
SLP_S5#/GPIO63 D10
SLP_S4# H4
SLP_S3# F4
SLP_A# G10
SLP_SUS# G16
PMSYNCH AP14
SLP_LAN#/GPIO29 K14
SUSACK# C12
SYS_RESET# K3
SYS_PWROK P12
PWROK L22
APWROK L10
DRAMPWROK B13
RSMRST# C21
SUSWARN#/SUSPWRDNACK/GPIO30 K16
PWRBTN# E20 INT. PU 20K
ACPRESENT/GPIO31 H20 INT. PD 20K
BATLOW#/GPIO72 E10 INT. PU 20K
RI# A10

P3V3_RTC
R4829 330K_5%_2
R4830 330K_5%_2_DY

P3V3A
R4832 1K_5%_2_DY
R4831 SHORT_0402
RSMRST# IN 21D1 21D3 49B7

PCIE_WAKE# IN 22B5 27C7 49A5
PCI_3S_CLKRUN# IN 21E3 49A5
EC_32KHZ OUT 21B6
SLP_S5# 3R OUT 14D2 21D3
SLP_S3# IC_3R
SLP_SUS# OUT
H_PM_SYNC BI 41C5
PCH_GPIO29 IN 49A5

P3V3_LDO
R4883 10K_5%_2_DY
SLP_S5_3R OUT
Q4713 SSM3K7002FU_DY
R4834 10K_5%_2
SLP_S3_3R OUT 15B8 15A4 15B4 16A7
Q4714 SSM3K7002BFU

P3V3A
U4704 TC7SZ08FU
SLP_S3#_3R OUT 13A2 45D3 13D2 14A6 14B8 14D2 21D6
R4710 100K_5%_2

P3V3S
R4815 10K_5%_2
SYS_RESET# IN 41C1
R4816 0_5%_2_DY
SUSACK# IN
CORE_PG IN 40B4 11C7 11A4
PCH_PWROK IN 49A6 21B6

P3V3A
R4820 10K_5%_2_DY
PM_DRAM_PWRGD OUT 41C7
RSMRST# IN 49C2 21D1 21D3
SUS_PWR_ACK OUT 49A5
EC_PWRSW# IN 21D6
D4706 BAT54_30V_0.2A
ACPRESENT IN 49A5 21D6
D4707 BAT54_30V_0.2A
LOW_BAT#_3 IN 21D6
PM_RI# IN 49A5

P3V3A
R4822 8.2K_5%_2

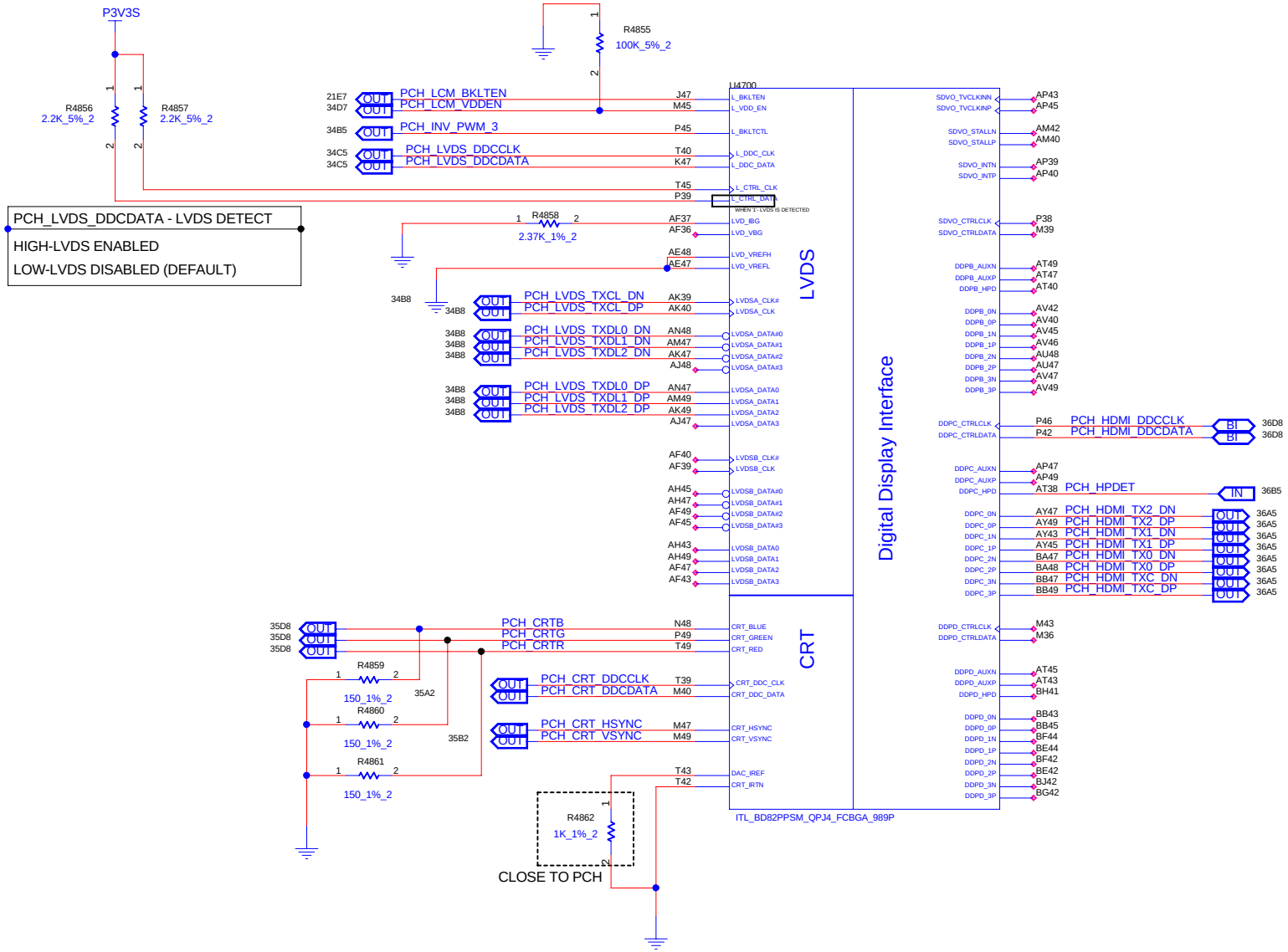
PCH_PWROK IN 49B7 21B6
R4823 10K_5%_2

P3V3A
ACPRESENT IN 49A6 21D6 R4824 10K_5%_2
SUS_PWR_ACK IN 49B7 R4825 10K_5%_2
PM_RI# IN 49A6 R4826 10K_5%_2
PCIE_WAKE# IN 49B3 27C7 22B5 R4827 10K_5%_2
PCH_GPIO29 IN 49A3 R4821 10K_5%_2

P3V3S
PCI_3S_CLKRUN# IN 49B3 21E3 R4828 8.2K_5%_2

INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 49 of 70

REFERENCE 4700~4949(PCH)



INVENTEC			
TITLE: MODEL,PROJECT,FUNCTION Block Diagram			
SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET 50 of 70	

REFERENCE 4700~4949(PCH)

GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	------
1	1	SPI (DEFAULT)
0	0	LPC

P3V3S

R4874 1 2 8.2K_5%_2 PCI_3S_INTA# BI 51B6
R4875 1 2 8.2K_5%_2 PCI_3S_INTB# BI 51B6
R4876 1 2 8.2K_5%_2 PCI_3S_INTC# BI 51B6
R4877 1 2 8.2K_5%_2 PCI_3S_INTD# BI 51B6
R4878 1 2 8.2K_5%_2 RUNSCI0# 3 IN 21E3 52D6

R4880 1 2 10K_5%_2 DGPU_HOLD_RST# IN 51B6 57A6
R4881 1 2 10K_5%_2 PCI_3S_REQ2# IN 51B6
R4882 1 2 10K_5%_2 DGPU_PWR_EN# IN 16A3 51B6

R4838 1 2 10K_5%_2 SATA_ODD_DA# IN 29A5 51B6
R4956 1 2 10K_5%_2 PCI_3S_PIRQG# IN 51B6
R4879 1 2 10K_5%_2 PCI_3S_PIRQH# IN 51B6
R4957 1 2 10K_5%_2 PCI_3S_PIRQE# IN 51B6

ROUTE WITH 90 OHMS IMPEDANCE
TOTAL LENGTH NO LONGER THAN 11 INCHES

32C6 33C4 USB3_PCH_RX1_DN USB3_PCH_RX2_DN
32C6 33C4 USB3_PCH_RX1_DP USB3_PCH_RX2_DP
32B7 33B5 USB3_PCH_TX1_DN USB3_PCH_TX2_DN
32B7 33B5 USB3_PCH_TX1_DP USB3_PCH_TX2_DP

BBS STRAPING
BBS_BIT1
STP_A16OVR
R4885 1K_5%_2_DY
R4886 1K_5%_2_DY 51C7

LOW=A16 SWAP OVERRIDE
STP_A16OVR
TOP-BLOCK SWAP OVERRIDE
HIGH=DEFAULT

P3V3A
R4887 10K_5%_2 P3V3A_PME# K10 PME# INT. PU 20K

41C7 36B2 BI PLT_RST# C6 PLTRST#

P3V3A
U4705 TC7SZ08FU
28C3 27C7 27C3 21E3 57A6 BI BUF_PLT_RST#
R4888 100K_5%_2

21E3 48A3 CLK_KBPCI CLKIN_PCI_FB R4889 R4890 22_5%_2 CLK_KBPCI_R CLK_PCI_FB_R H49 H43
27C7 CLK_PCI_DEBUG R4891 22_5%_2 CLK_PCI_DEBUG_R J48 K42 H40
TP4717 TP24
C4800

MCAHINE ID 0: USB ID0 CSC0402_DY
MACHINE ID 1: POWER EXPRESS (YES:1 NO:0)
MACHINE ID 2: UMA:1 / DIS.:0
MACHINE ID 3: MAINSTREAM:1 / ENTRY:0
MACHINE ID 4: HDMI:1 / NO HDMI:0
MACHINE ID 5: SLEEP&CHARGE&DOLBY:(YES1 / NO 0)
MACHINE ID 6: USB ID1
MACHINE ID 1_DB : 35W CPU ONLY :1 / 35W&45W CPU:0

	USB3.0 X2 / 2.0 X1	USB3.0 X1 / 2.0 X2	USB2.0 X3
USB ID0	1	1	0
USB ID1	1	0	1

U4700

RSVD: BG26 BJ26 BH25 BJ16 BG16 AH38 AH37 AK43 AK45 C18 N30 H3 AH12 AM4 AM5 Y13 K24 L24 AB46 AB45 TP1–TP20
RSVD: B21 M20 AY16 BG46 TP21–TP24
RSVD: AY7 AV7 AU3 BG4 AT10 BC8 AU2 AT4 AT3 AT1 AY3 AT5 AV3 AV1 BB1 BA3 BB5 BB3 BB7 BE8 BD4 BF6 AV5 AV10 AT8 AY5 BA2 AT12 BF3

USB3RN1 BE28
USB3RN2 BC30
USB3RN3 BE32
USB3RN4 BJ32
USB3RP1 BC28
USB3RP2 BE30
USB3RP3 BF32
USB3RP4 BG32
USB3TN1 AV26
USB3TN2 BB26
USB3TN3 AU28
USB3TN4 AY30
USB3TP1 AU26
USB3TP2 AV26
USB3TP3 AV28
USB3TP4 AW30

PCI
51D7 51C7 51C7 51C7 BI PCI_3S_INTA# PCI_3S_INTB# PCI_3S_INTC# PCI_3S_INTD# K40 K38 H38 G38
PIRQA# PIRQB# PIRQC# PIRQD#
51C7 57A6 16A3 51C7 OUT DGPU_HOLD_RST# PCI_3S_REQ2# DGPU_PWR_EN# C46 C44 E40
REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54
D47 E42 F46
GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55
USED AS GPIO ONLY. INT. PU 20K
51B7 29A5 51C7 51B7 BI PCI_3S_PIRQE# SATA_ODD_DA# PCI_3S_PIRQG# PCI_3S_PIRQH# G42 G40 C42 D44
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

CLKOUT_PCI0 H49
CLKOUT_PCI1 H43
CLKOUT_PCI2 J48
CLKOUT_PCI3 K42
CLKOUT_PCI4 H40

ITL_BD82PPSM_QPJ4_FCBGA_989P

NVRAM

USB
DEBUG PORT
USBP0N C24 USB_P0_DN BI 32B8
USBP0P A24 USB_P0_DP BI 32C8
USBP1N C25 USB_P1_DN BI 33C5
USBP1P B25 USB_P1_DP BI 33C5
USBP2N C26 USB_P2_DN BI 30C5
USBP2P A26 USB_P2_DP BI 30C5
32B8 32C8
P0.P1 RESERVER FOR USB3.0

USBP3N K28
USBP3P H28
USBP4N E28
USBP4P D28
USBP5N C28
USBP5P A28
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28

USBP8N L30 USB_CR_DN BI 26A8 CARD READER
USBP8P K30 USB_CR_DP BI 26A8
USBP9N G30 USB_WLAN_DN BI 27B3 WLAN
USBP9P E30 USB_WLAN_DP BI 27B3
USBP10N C30 USB_CAM_DN BI 34B3 WEBCAM
USBP10P A30 USB_CAM_DP BI 34B3
USBP11N L32 USB_3G_DN BI 28C3 3G
USBP11P K32 USB_3G_DP BI 28C3
USBP12N G32
USBP12P E32
USBP13N C32
USBP13P A32

USBRBIAS# C33
USBRBIAS B33
R4835 22.6_1%_3 CLOSE TO PCH

OC0#/GPIO59 A14 MACHINE_ID0 IN 51A3 51A5
OC1#/GPIO40 K20 MACHINE_ID1 IN 51A3 51A5
OC2#/GPIO41 B17 MACHINE_ID2 IN 51A3 51A5
OC3#/GPIO42 C16 MACHINE_ID3 IN 51A3 51A5
OC4#/GPIO43 L16 MACHINE_ID4 IN 51A3 51A5
OC5#/GPIO9 A16 MACHINE_ID5 IN 51A3 51A5
OC6#/GPIO10 D14 MACHINE_ID6 IN 51A3 51A5
OC7#/GPIO14 C14 MACHINE_ID1_DB IN 51A3 51A5
TO BE USED AS GPIO

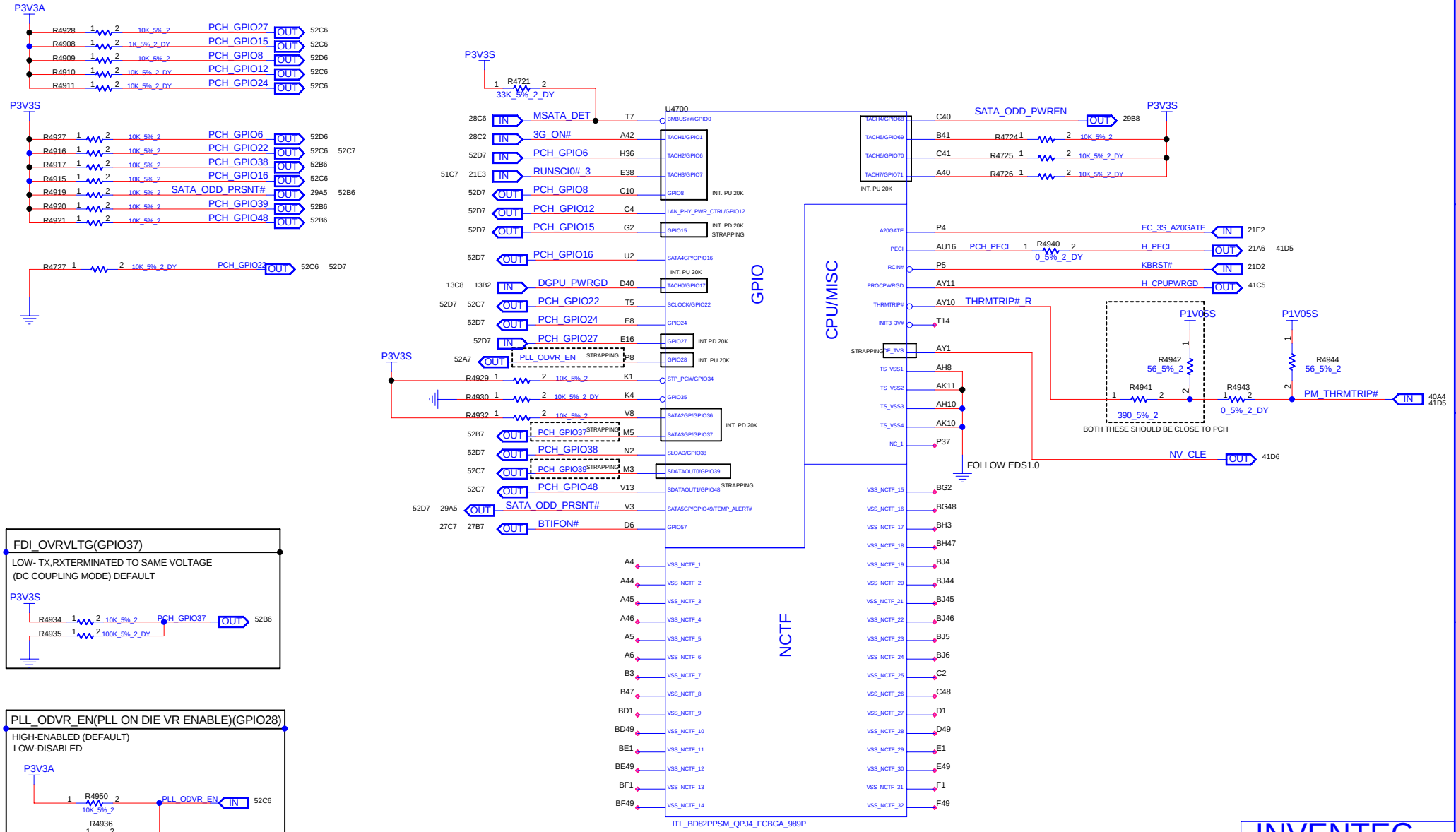
NOTE:
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPEDUSB3.0 PORT 1,2

51A3 51A2 OUT MACHINE_ID0 R4892 10K_5%_2
51A3 51A2 OUT MACHINE_ID1 R4893 10K_5%_2
51A3 51A2 OUT MACHINE_ID2 R4894 10K_5%_2
51A3 51A2 OUT MACHINE_ID3 R4895 10K_5%_2
51A3 51A2 OUT MACHINE_ID4 R4896 10K_5%_2
51A3 51A2 OUT MACHINE_ID5 R4897 10K_5%_2
51A3 51A2 OUT MACHINE_ID6 R4898 10K_5%_2
51A3 51A2 OUT MACHINE_ID1_DB R4899 10K_5%_2_DY
NOTE:10K_5%(60130B1030ZT)

P3V3A
51A2 51A5 OUT MACHINE_ID0 R4900 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID1 R4901 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID2 R4902 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID3 R4903 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID4 R4904 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID5 R4905 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID6 R4906 10K_5%_2_DY
51A2 51A5 OUT MACHINE_ID1_DB R4907 10K_5%_2
NOTE:10K_5%(60130B1030ZT)

INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 51 of 70

REFERENCE 4700~4949(PCH)



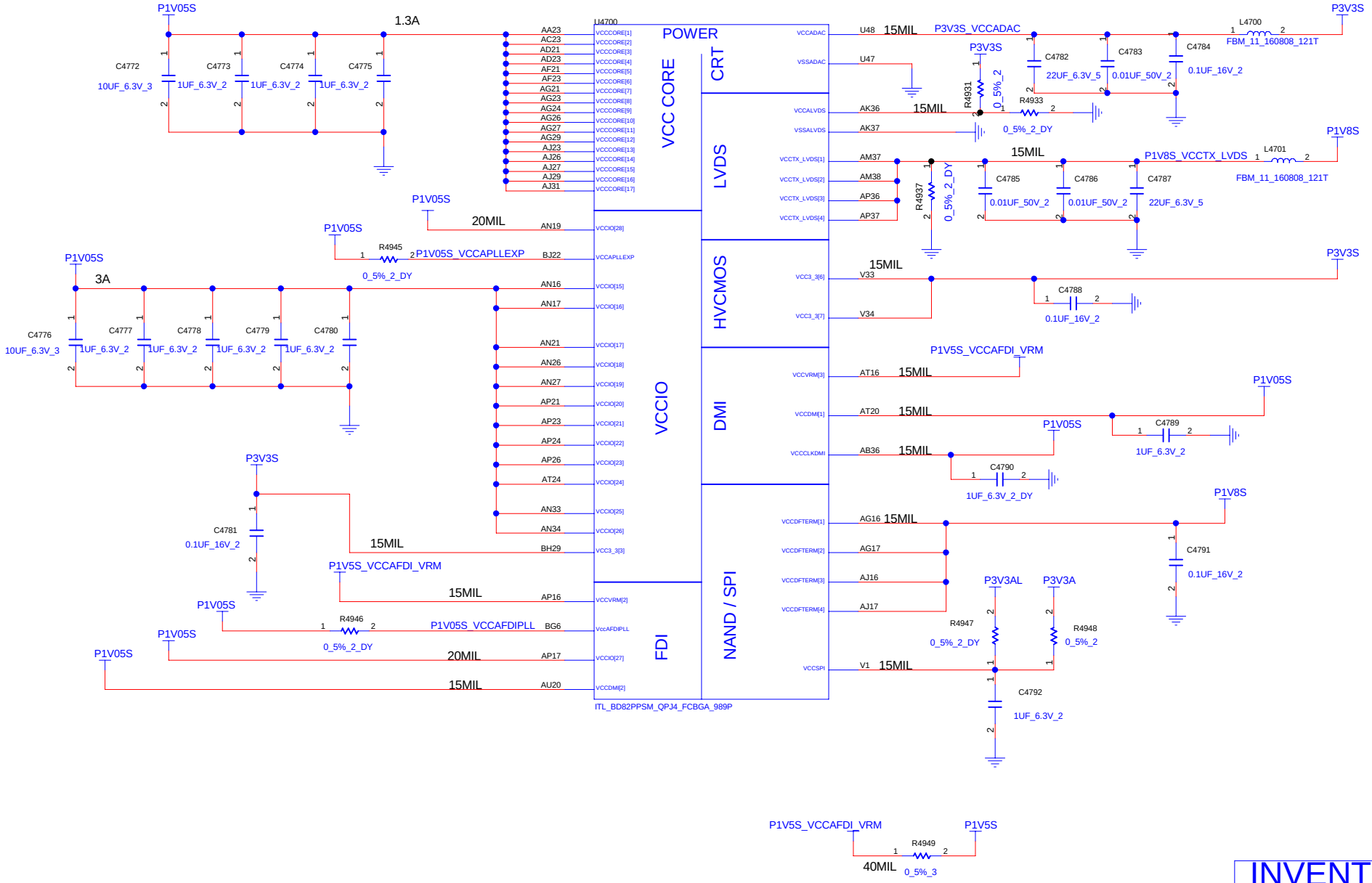
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

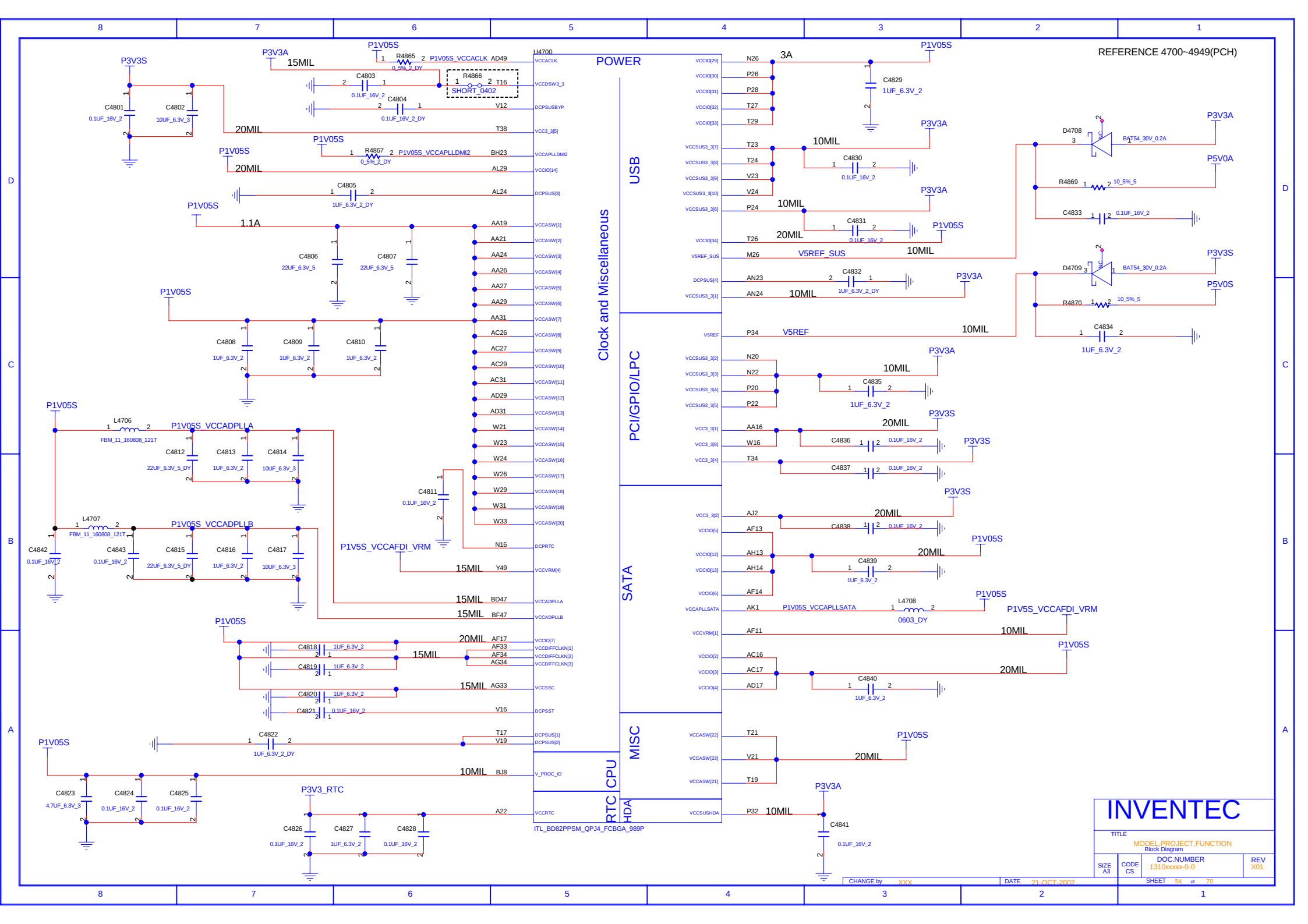
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 52 of 70

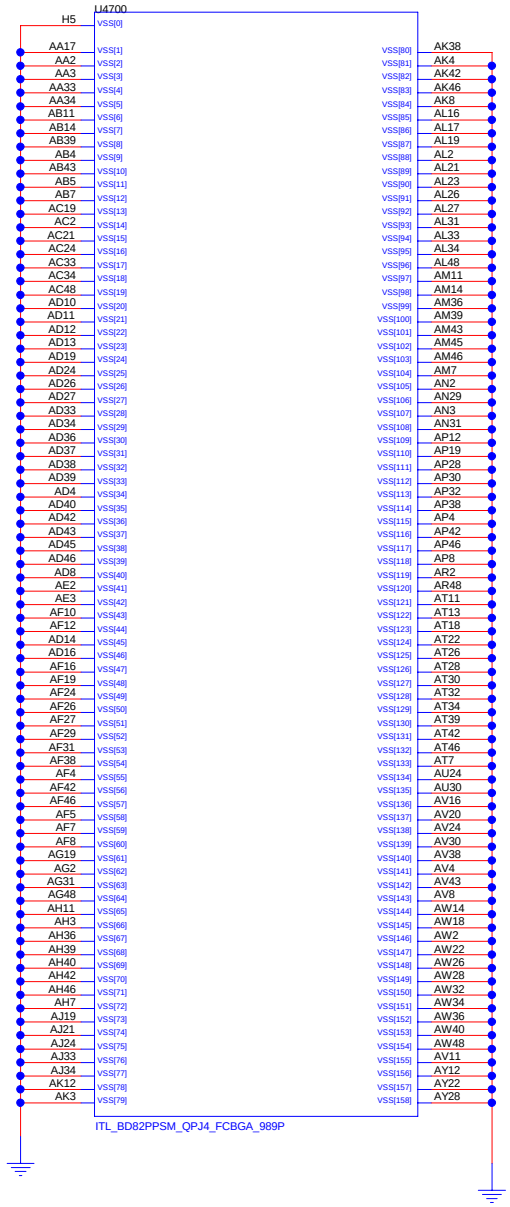
REFERENCE 4700~4949(PCH)

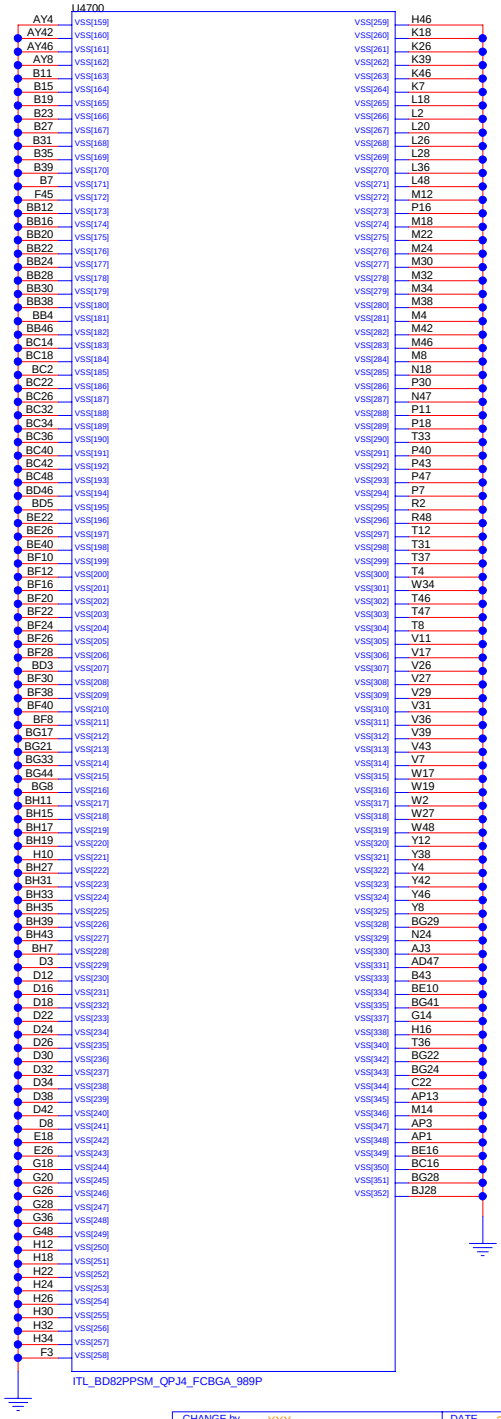


TITLE	INVENTEC
	MODEL,PROJECT,FUNCTION
	Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
CHANGE by	XXX
DATE	21-OCT-2002
SHEET	53 of 70


REFERENCE 4700~4949(PCH)
POWER
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
U4700
ITL_BD82PPSM_QPJ4_FCBGA_989P
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 54 of 70

REFERENCE 4700~4949(PCH)





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 55 of 70

THAMES (6019B0917601)

PIN BASE STRAPS		
GPIO_0	TRANSMITTER POWER SAVING ENABLE	0 : 50% TX OUTPUT SWING (DEFAULT) 1 : FULL TX OUTPUT SWING
GPIO_1	PCIE TRANSMITTER DE-EMPHASIS	0 : DE-EMPHASIS DISABLED (DEFAULT) 1 : DE-EMPHASIS ENABLED
GPIO_2	GEN1/GEN2 ENABLE	0 : GEN1 (DEFAULT) 1 : GEN2
GPIO_8 GPIO_21	MUST BE LOW DURING RESET	LEFT UNCONNECTED
GPIO_9	VGA DISABLE	0 : ENABLE (DEFAULT) 1 : DISABLE
GPIO_[11:13]	MEMORY APERTURE SIZE	GPIO_13 / GPIO_12 / GPIO_11 → MEMORY APERTURE SIZE 0 0 0 → 128M 0 0 1 → 256M 0 1 0 → 64M 0 1 1 → 32M
GPIO_22	ENABLE EXTERNAL BIOS ROM DEVICE	0 : DISABLE (DEFAULT) 1 : ENABLE
HSYNC[1] VSYNC[0]	AUDIO[1:0]	00 : NO AUDIO FUNCTION 01 : AUDIO FOR DP ONLY 10 : AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED 11 : AUDIO FOR BOTH DP AND HDMI

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	0	HYNIX1GDFR*4 512MB
0	0	0	1	HYNIX2GBFR*4 1GB
0	0	1	0	HYNIX2GDFR*41GB
0	0	1	1	RESERVE
0	1	0	0	HYNIX1GDFR*8 1GB
0	1	0	1	HYNIX2GBFR*8 2GB
0	1	1	0	HYNIX2GDFR*82GB
0	1	1	1	RESERVE
1	0	0	0	AMDC11*4 512MB
1	0	0	1	AMDA11*4 1GB
1	0	1	0	AMDB11*4 1GB
1	0	1	1	RESERVE
1	1	0	0	AMDC11*8 1HB
1	1	0	1	AMDA11*8 2GB
1	1	1	0	AMDB11*8 2GB
1	1	1	1	RESERVE

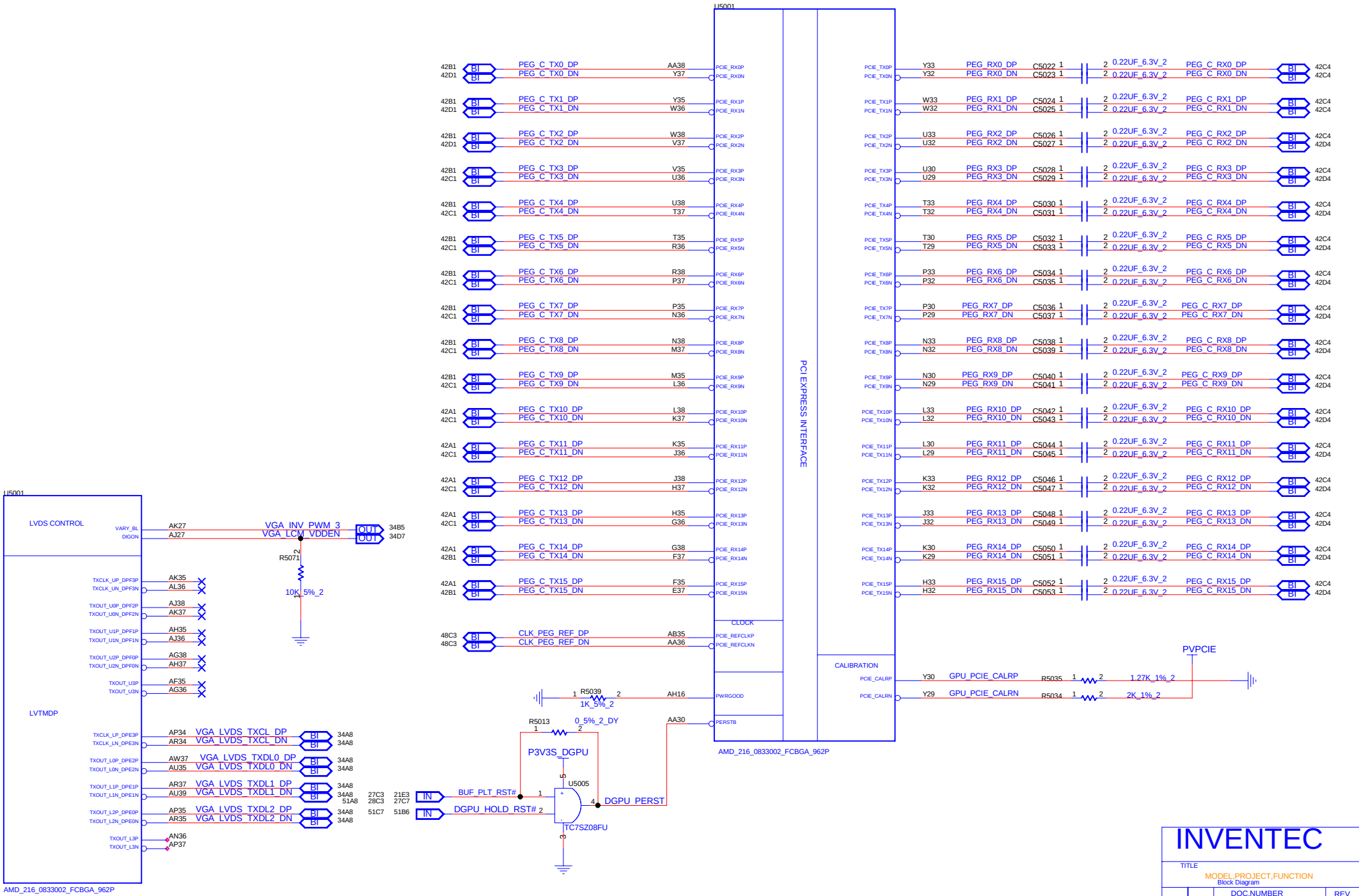
PLACE CLOSE TO ASIC

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE C | CODE CS | DOC NUMBER 1310xxxx-0x0 | REV X01

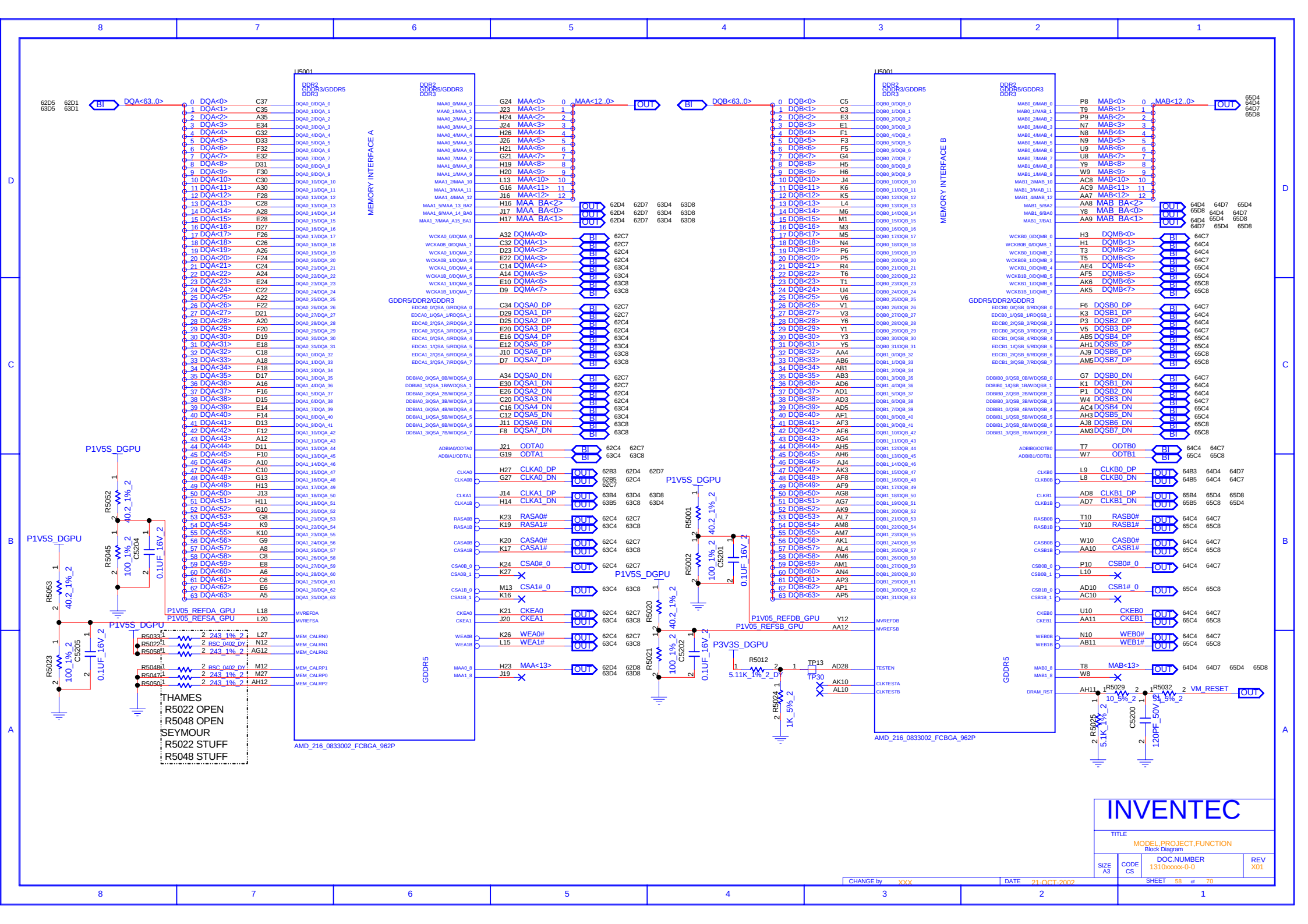
CHANGE by XXX | DATE 21-OCT-2002 | SHEET 56 of 70



CHANGE by	XXX
DATE	21-OCT-2002
SHEET	57 of 70

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01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DDR2 GDDR3/GDDR5 DDR3
MEMORY INTERFACE A
AMD_216_0833002_FCBGA_962P
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MAA<11>
MAA<12>
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MAA_BA<0>
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DQSA1_DP
DQSA2_DP
DQSA3_DP
DQSA4_DP
DQSA5_DP
DQSA6_DP
DQSA7_DP
DQSA0_DN
DQSA1_DN
DQSA2_DN
DQSA3_DN
DQSA4_DN
DQSA5_DN
DQSA6_DN
DQSA7_DN
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DQMA<1>
DQMA<2>
DQMA<3>
DQMA<4>
DQMA<5>
DQMA<6>
DQMA<7>
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CLKA0_DP
CLKA0_DN
CLKA1_DP
CLKA1_DN
RASA0#
RASA1#
CASA0#
CASA1#
CSA0#_0
CSA1#_0
CKEA0
CKEA1
WEA0#
WEA1#
MAA<13>
GDDR5
GDDR5/DDR2/GDDR3
P1V5S_DGPU
P1V05_REFDA_GPU
P1V05_REFSA_GPU
R5052 40.2_1%_2
R5045 100_1%_2
C5204 0.1UF_16V_2
R5053 40.2_1%_2
R5023 100_1%_2
C5205 0.1UF_16V_2
R5033 2_243_1%_2
R5022 RSC_0402_DY
R5058 2_243_1%_2
R5048 RSC_0402_DY
R5047 2_243_1%_2
R5050 2_243_1%_2
MEM_CALRN0
MEM_CALRN1
MEM_CALRN2
MEM_CALRP1
MEM_CALRP0
MEM_CALRP2
THAMES
R5022 OPEN
R5048 OPEN
SEYMOUR
R5022 STUFF
R5048 STUFF
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MAB<12..0>
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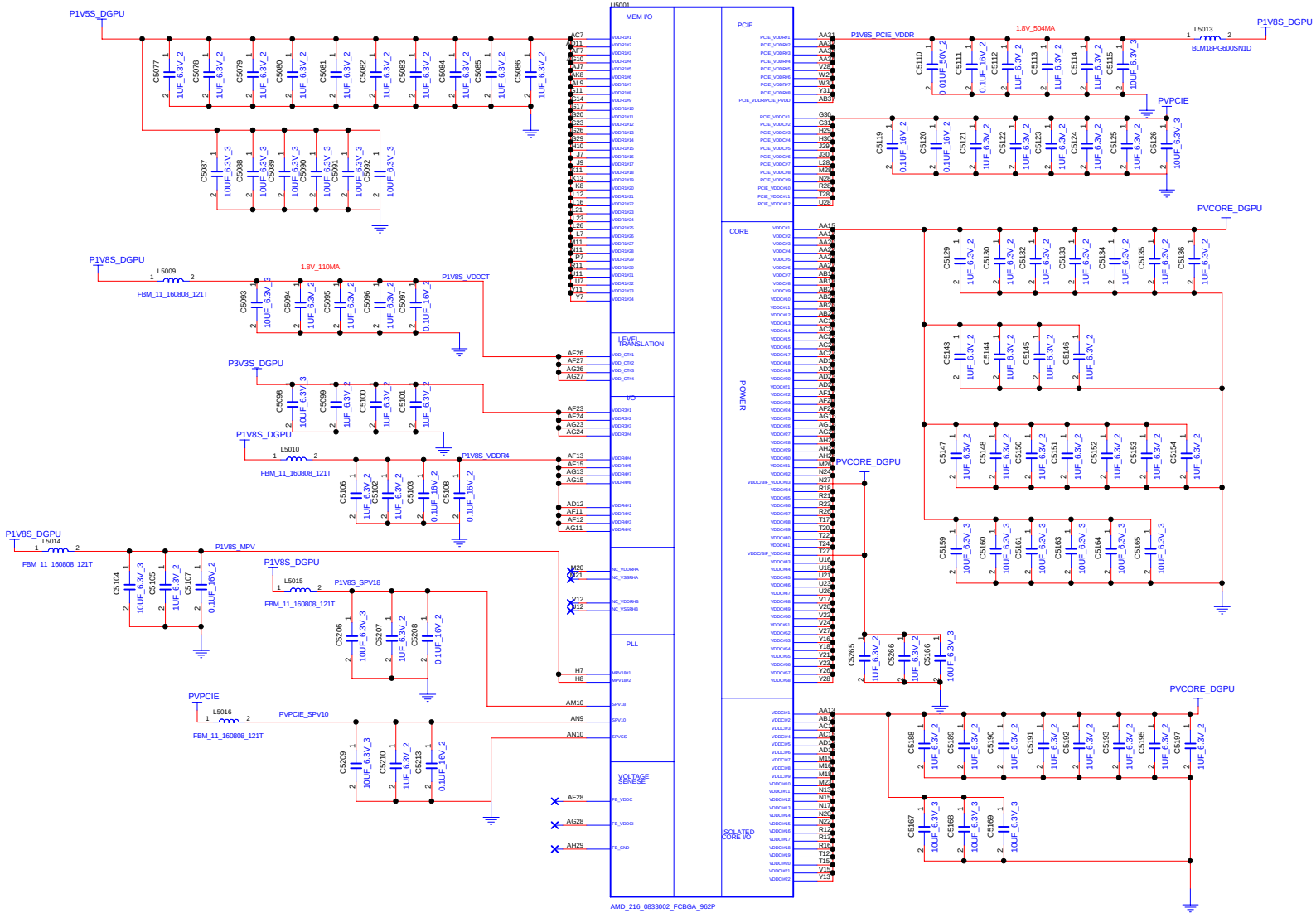
DQSB0_DP
DQSB1_DP
DQSB2_DP
DQSB3_DP
DQSB4_DP
DQSB5_DP
DQSB6_DP
DQSB7_DP
DQSB0_DN
DQSB1_DN
DQSB2_DN
DQSB3_DN
DQSB4_DN
DQSB5_DN
DQSB6_DN
DQSB7_DN
ODTB0
ODTB1
CLKB0_DP
CLKB0_DN
CLKB1_DP
CLKB1_DN
RASB0#
RASB1#
CASB0#
CASB1#
CSB0#_0
CSB1#_0
CKEB0
CKEB1
WEB0#
WEB1#
MAB<13>
MEMORY INTERFACE B
P1V05_REFDB_GPU
P1V05_REFSB_GPU
P3V3S_DGPU
R5001 40.2_1%_2
R5002 100_1%_2
C5201 0.1UF_16V_2
R5020 40.2_1%_2
R5021 100_1%_2
C5202 0.1UF_16V_2
R5012 5.11K_1%_2_DY
TP13
TP30
R5024 1K_5%_2
TESTEN
CLKTESTA
CLKTESTB
DRAM_RST
R5029 10_5%_2
R5032 21_5%_2
VM_RESET
R5025 5.1K_1%_2
C5200 120PF_50V_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 58 of 70

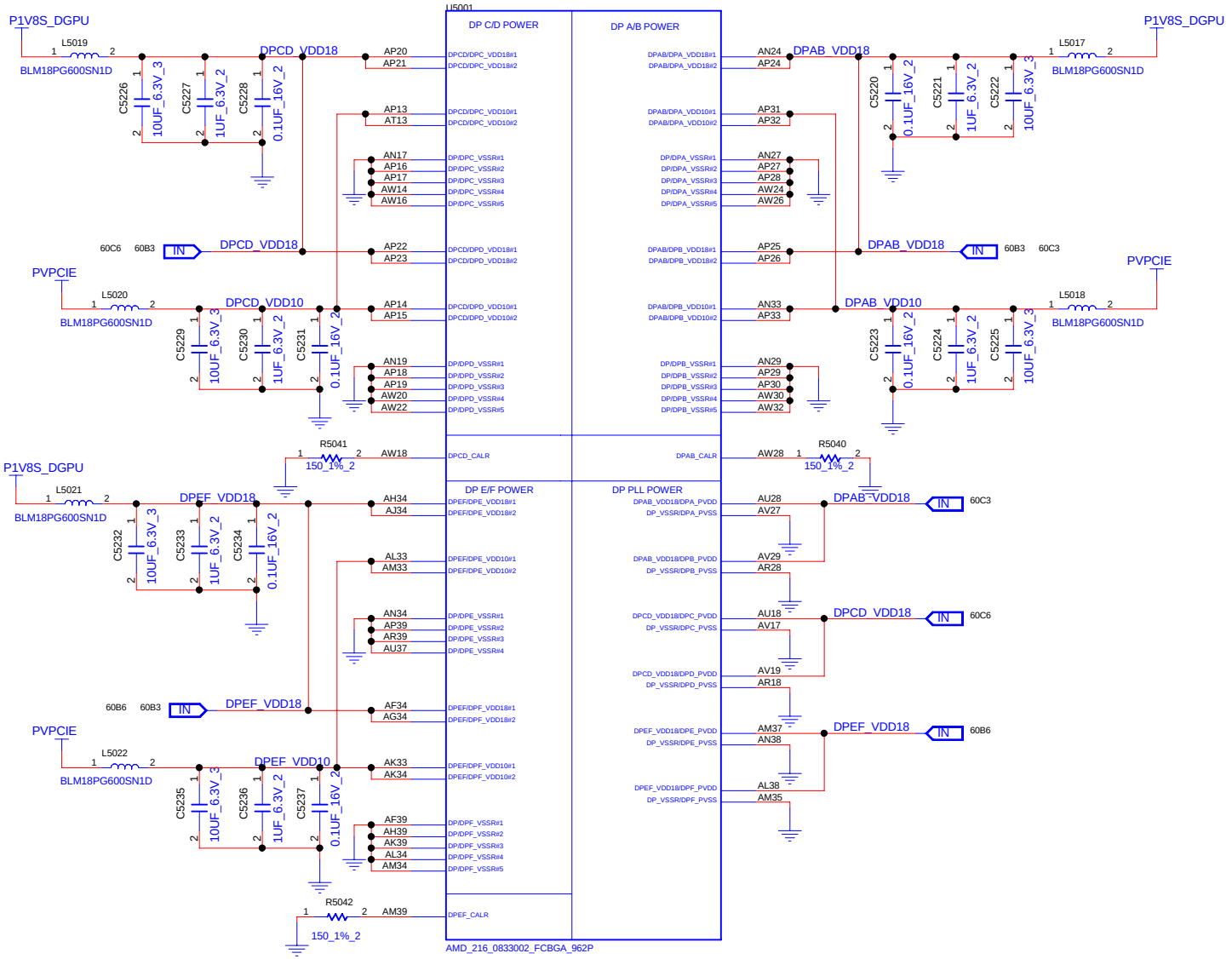


INVENTEC

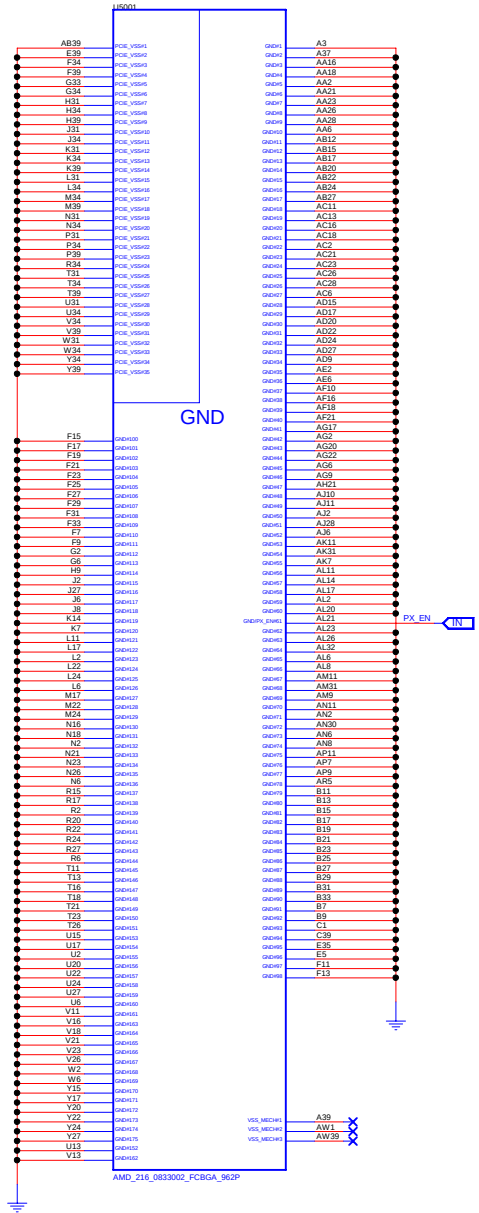
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 59 of 70



TITLE	INVENTEC
	MODEL,PROJECT,FUNCTION
	Block Diagram
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
CHANGE by	XXX
DATE	21-OCT-2002
SHEET	60 of 70

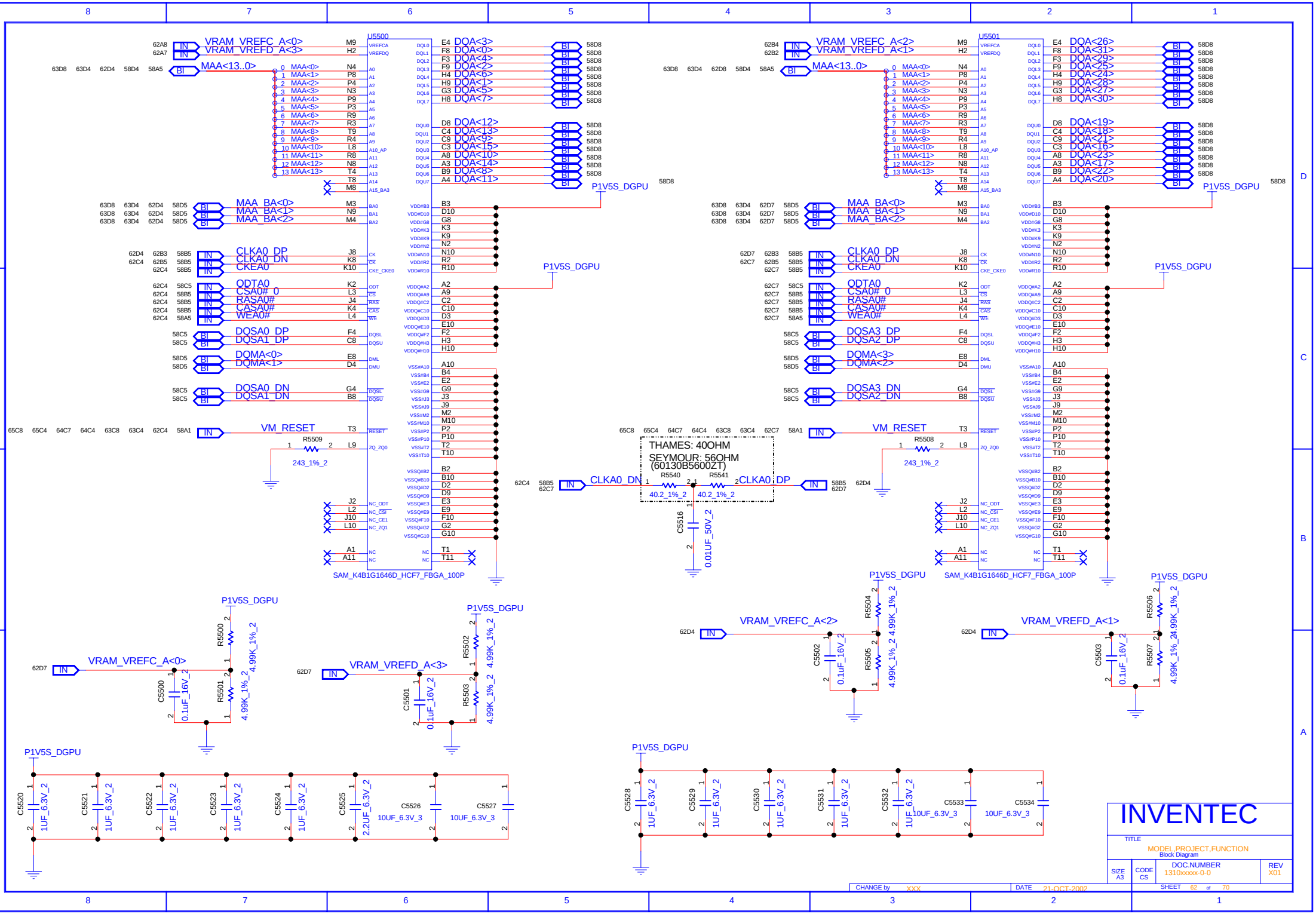


INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002 | SHEET 61 of 70


U5500
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VRAM_VREFD_A<3>
MAA<13..0>
MAA_BA<0>
MAA_BA<1>
MAA_BA<2>
CLKA0_DP
CLKA0_DN
CKEA0
ODTA0
CSA0#_0
RASA0#
CASA0#
WEA0#
DQSA0_DP
DQSA1_DP
DQMA<0>
DQMA<1>
DQSA0_DN
DQSA1_DN
VM_RESET
R5509
243_1%_2
P1V5S_DGPU
SAM_K4B1G1646D_HCF7_FBGA_100P
U5501
VRAM_VREFC_A<2>
VRAM_VREFD_A<1>
DQSA3_DP
DQSA2_DP
DQMA<3>
DQMA<2>
DQSA3_DN
DQSA2_DN
R5508
THAMES: 40OHM
SEYMOUR: 56OHM
(60130B5600ZT)
R5540
R5541
40.2_1%_2
CLKA0_DN
CLKA0_DP
C5516
0.01UF_50V_2
VRAM_VREFC_A<0>
VRAM_VREFD_A<3>
R5500
R5501
R5502
R5503
C5500
C5501
0.1uF_16V_2
4.99K_1%_2
VRAM_VREFC_A<2>
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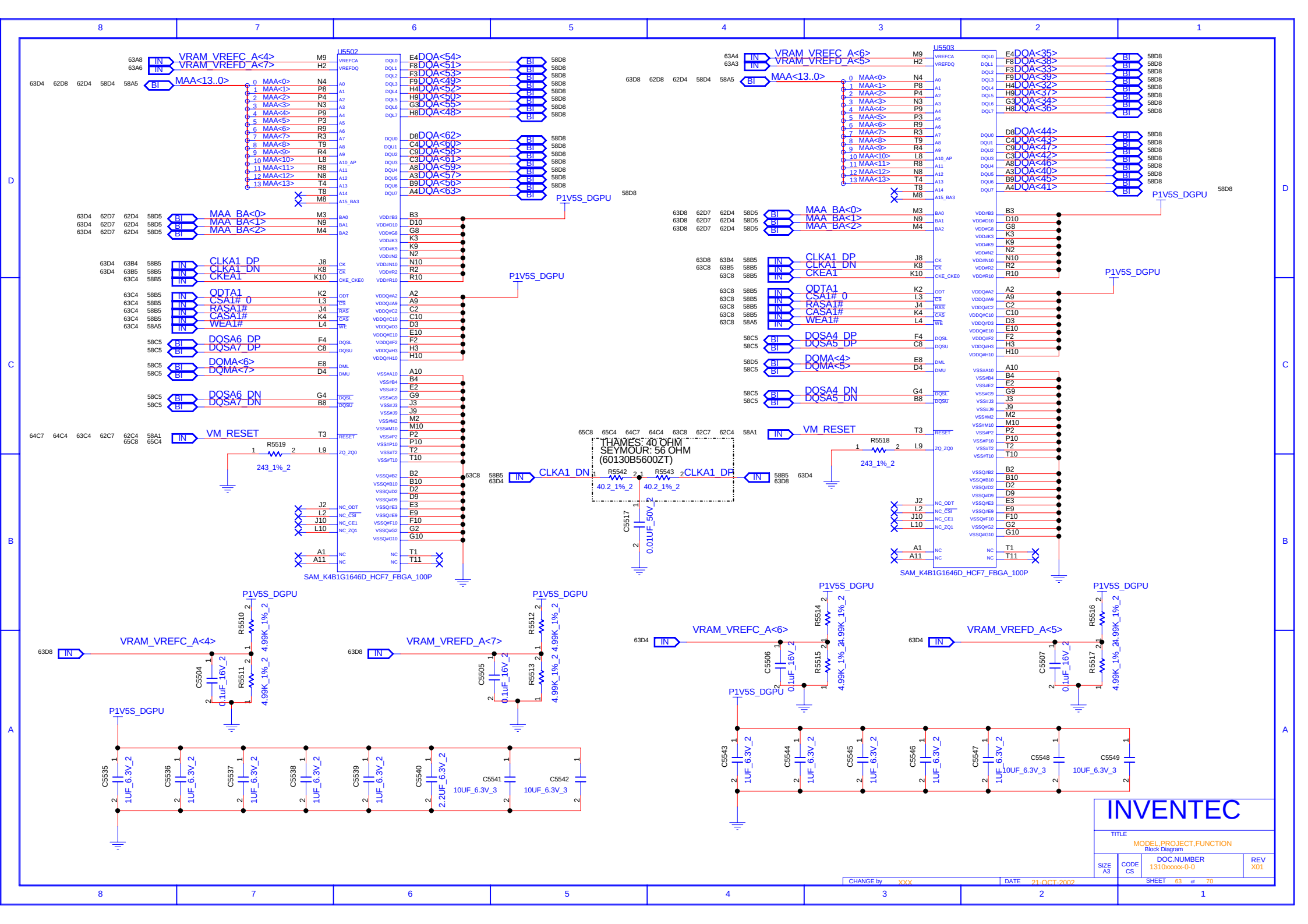
R5504
R5505
R5506
R5507
C5502
C5503
4.99K_1%_24.99K_1%_2
C5520
C5521
C5522
C5523
C5524
C5525
C5526
C5527
C5528
C5529
C5530
C5531
C5532
C5533
C5534
1UF_6.3V_2
2.2UF_6.3V_2
10UF_6.3V_3
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
DATE 21-OCT-2002
SHEET 62 of 70


U5502
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VRAM_VREFD_A<7>
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MAA_BA<0>
MAA_BA<1>
MAA_BA<2>
CLKA1_DP
CLKA1_DN
CKEA1
ODTA1
CSA1#_0
RASA1#
CASA1#
WEA1#
DQSA6_DP
DQSA7_DP
DQMA<6>
DQMA<7>
DQSA6_DN
DQSA7_DN
VM_RESET
R5519
243_1%_2
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SAM_K4B1G1646D_HCF7_FBGA_100P
U5503
VRAM_VREFC_A<6>
VRAM_VREFD_A<5>
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DQSA5_DP
DQMA<4>
DQMA<5>
DQSA4_DN
DQSA5_DN
R5518
THAMES: 40 OHM
SEYMOUR: 56 OHM
(60130B5600ZT)
R5542
R5543
40.2_1%_2
C5517
0.01UF_50V_2
R5510
R5511
4.99K_1%_2
C5504
0.1uF_16V_2
R5512
R5513
C5505
R5514
R5515
C5506
R5516
R5517
C5507
C5535
C5536
C5537
C5538
C5539
C5540
C5541
C5542
C5543
C5544
C5545
C5546
C5547
C5548
C5549
1UF_6.3V_2
2.2UF_6.3V_2
10UF_6.3V_3
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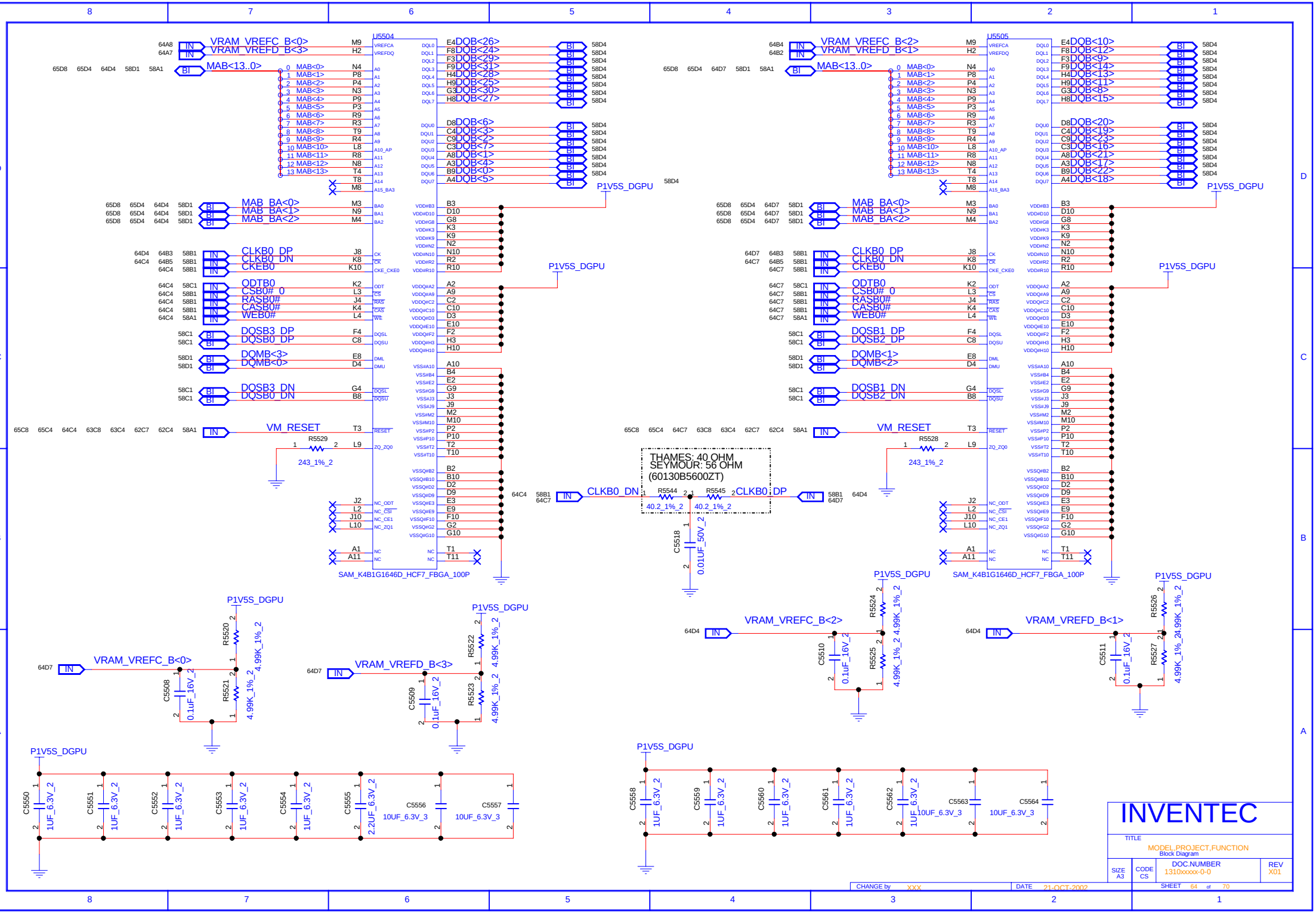
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U5505
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VRAM_VREFD_B<3>
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MAB_BA<0>
MAB_BA<1>
MAB_BA<2>
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CLKB0_DN
CKEB0
ODTB0
CSB0#_0
RASB0#
CASB0#
WEB0#
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DQSB0_DN
VM_RESET
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243_1%_2
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P1V5S_DGPU
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VRAM_VREFD_B<1>
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THAMES: 40 OHM
SEYMOUR: 56 OHM
(60130B5600ZT)
R5544
R5545
40.2_1%_2
C5518
0.01UF_50V_2
R5520
R5521
R5522
R5523
R5524
R5525
R5526
R5527
C5508
C5509
C5510
C5511
0.1uF_16V_2
4.99K_1%_2
C5550
C5551
C5552
C5553
C5554
C5555
C5556
C5557
C5558
C5559
C5560
C5561
C5562
C5563
C5564
1UF_6.3V_2
2.2UF_6.3V_2
10UF_6.3V_3
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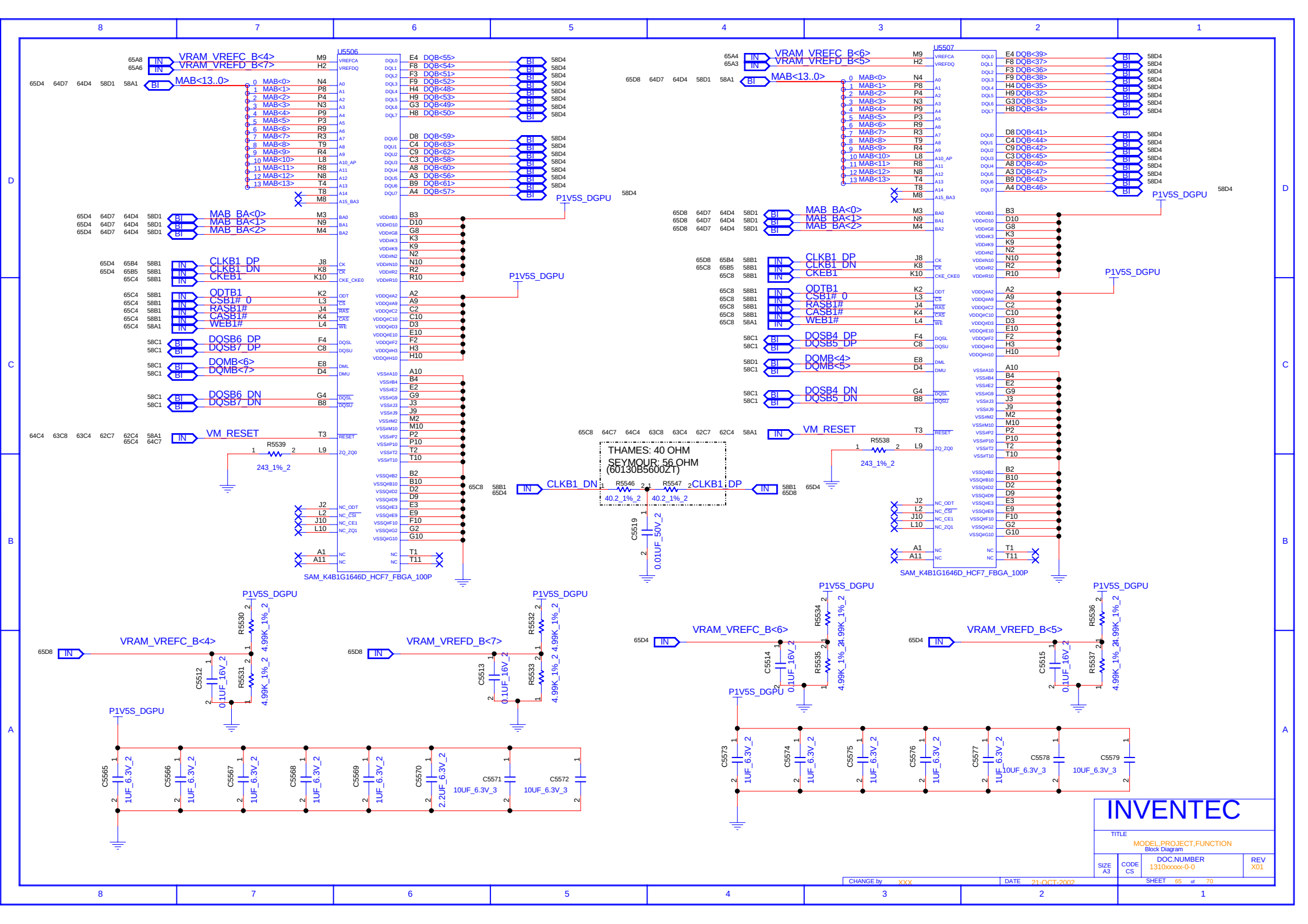
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VRAM_VREFD_B<7>
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MAB_BA<0>
MAB_BA<1>
MAB_BA<2>
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CLKB1_DN
CKEB1
ODTB1
CSB1#_0
RASB1#
CASB1#
WEB1#
DQSB6_DP
DQSB7_DP
DQMB<6>
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DQSB6_DN
DQSB7_DN
VM_RESET
P1V5S_DGPU
SAM_K4B1G1646D_HCF7_FBGA_100P
U5507
VRAM_VREFC_B<6>
VRAM_VREFD_B<5>
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MAB_BA<0>
MAB_BA<1>
MAB_BA<2>
CLKB1_DP
CLKB1_DN
CKEB1
ODTB1
CSB1#_0
RASB1#
CASB1#
WEB1#
DQSB4_DP
DQSB5_DP
DQMB<4>
DQMB<5>
DQSB4_DN
DQSB5_DN
VM_RESET
P1V5S_DGPU
SAM_K4B1G1646D_HCF7_FBGA_100P
THAMES: 40 OHM
SEYMOUR: 56 OHM
(60130B5600ZT)
CLKB1_DN
CLKB1_DP
R5546
R5547
40.2_1%_2
C5519
0.01UF_50V_2
R5538
243_1%_2
R5539
243_1%_2
VRAM_VREFC_B<4>
VRAM_VREFD_B<7>
VRAM_VREFC_B<6>
VRAM_VREFD_B<5>
R5530
R5531
R5532
R5533
R5534
R5535
R5536
R5537
4.99K_1%_2
C5512
C5513
C5514
C5515
0.1UF_16V_2
C5565
C5566
C5567
C5568
C5569
C5570
C5571
C5572
C5573
C5574
C5575
C5576
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C5579
1UF_6.3V_2
2.2UF_6.3V_2
10UF_6.3V_3
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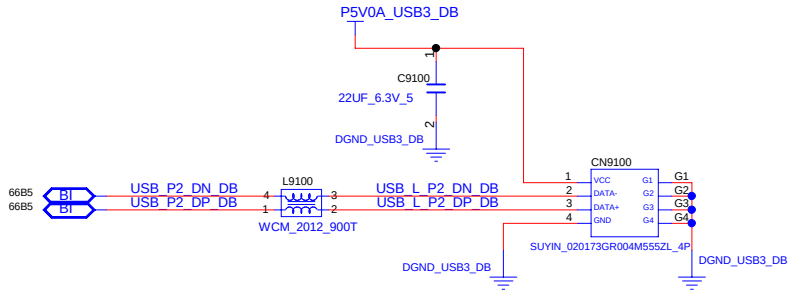
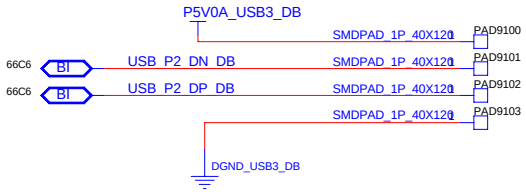
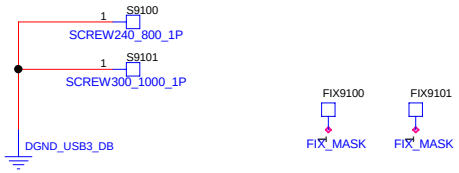
USB BOARD







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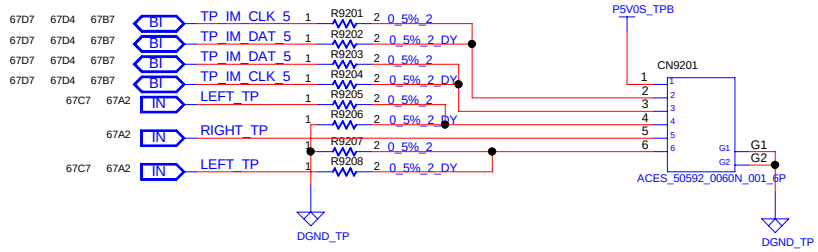
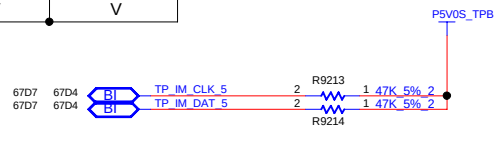
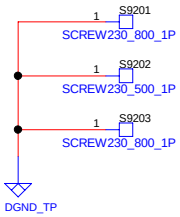
TOUCH PAD BOARD 4 PIN

TOUCHPAD TO MODULE CONN

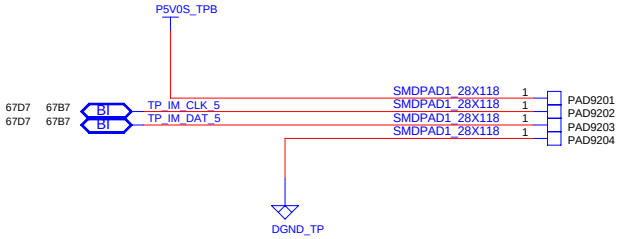


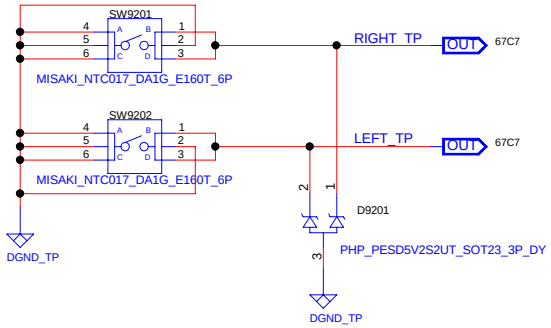
4PIN	IMR/METAL	TEXTURE
R9201		V
R9202	V	
R9203		V
R9204	V	
R9205		V
R9206	V	
R9207		V
R9208	V	
R9213	V	V
R9214	V	V





TOUCHPAD TO MB CONN





INVENTEC

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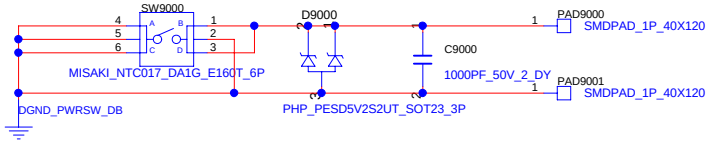
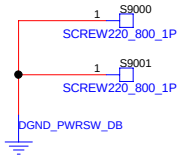
REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON





INVENTEC

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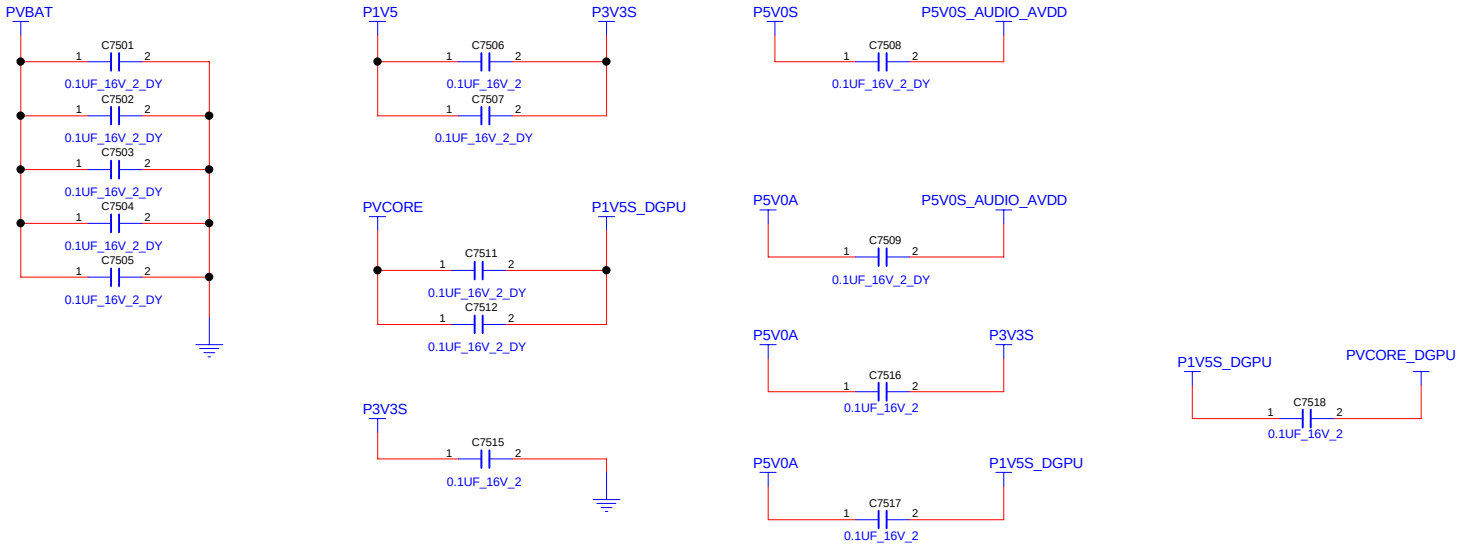

INVENTEC

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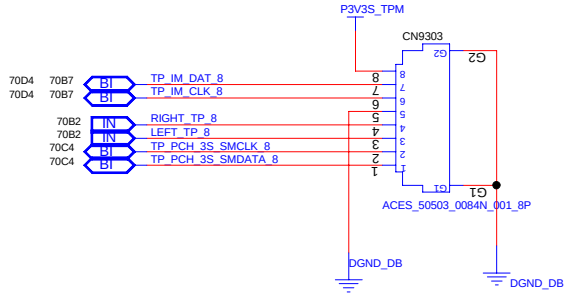
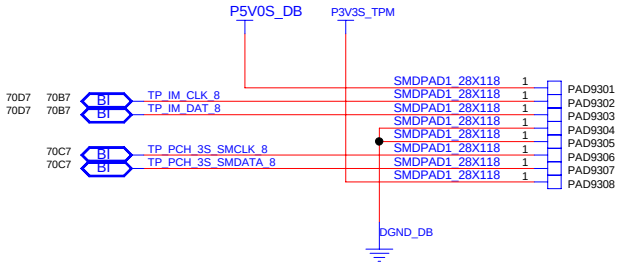
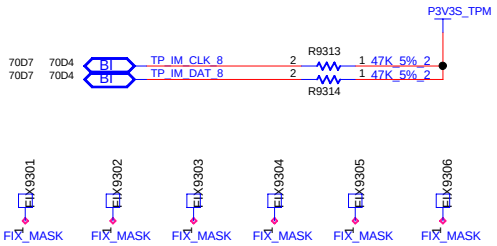
TOUCH PAD BOARD 8 PIN

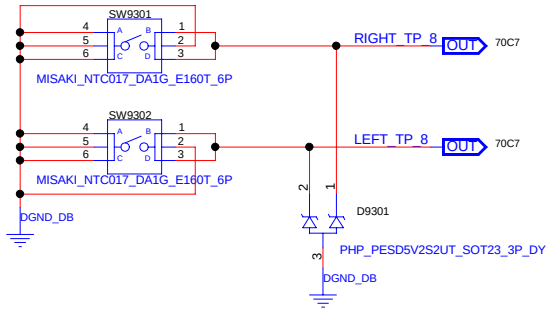
TOUCHPAD TO MODULE CONN

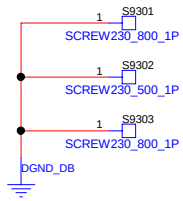


TOUCHPAD TO MB CONN









INVENTEC

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