Modeling and simulation of Power Consumption on Heterogenous CPU Cores under varying workloads and operating conditions

Atharv Arun Desai
Department of CSA
Indian Institute of Science (IISc)
Bangalore, India
atharvarun@iisc.ac.in

Boul Chandra Garai
Department of CSA
Indian Institute of Science (IISc)
Bangalore, India
chandraboul@iisc.ac.in

Himanshu Srivastava
Department of CSA
Indian Institute of Science (IISc)
Bangalore, India
himanshusriv@iisc.ac.in

Vaisakh P S
Department of CSA
Indian Institute of Science (IISc)
Bangalore, India
vaisakhp@iisc.ac.in

***Abstract*—Phase-2 report for E0-240 - Modeling and Simulation course project. The main objective of this project is to apply concepts learned in E0-240 course in to Modeling and simulation of a real-world system, which in this case is Multi-core, Heterogenous CPU. This project, will focus on developing a Power Consumption Model for simulated Full-System [1] under varying workloads. This model will be developed taking in consideration various operating conditions of the CPU such as Dynamic Frequency Scaling, Heterogenous Cores [2]**

***Index Terms*—Modeling, simulation, heterogenous CPU cores, power consumption**

I. Background

Power consumption is one of the key performance indices of any embedded or mobile device which operate of power budget, as this directly impacts on user experience and usability of any such devices. Hence, the need for accurate power models in simulation environment has increased as well, to enable designer and manufacturers to measure the impact of any new functionality or optimization that is being prototyped. Insights from such models, will allow all key stakeholders in an embedded product development arena for evaluation without waiting hardware fabrication and rollout, there by saving resources and investment.

One of the main motivations for this project is the top-down power modeling approach [3] that utilized Performance Monitoring Counters(PMCs) in an actual hardware along with overall power consumption data to develop an empirical power model in Gem5 simulator [1]. The average error achieved by this approach is claimed to be less than 6%. We will further explore in to additional enhancement over this said approach by factoring in additional CPU performance metrics.

II. Methodology

As mentioned in previous work [3], a similar method is followed in developing a Top-down Power model that will be integrated in to Gem5. ODROID-XU4 [4] Big-Little development board is chosen as first target for experimentation, data gathering and validation efforts. An overview of this hardware is show in Figure. 1. ODROID-XU4 offers minimalistic development platform with a Samsung Exynos 5422 Octa ARM Cortex™-A15 Quad 2GHz and Cortex™-A7 Quad 1.3GHz CPUs, with a 2GB LPDDR3 RAM operating at 933MHz stacked along with CPU package. Both Cortex-A15 and Cortex-A7 cores has 32KB Instruction and Data caches each. For L2 cache, the Cortex-A15 and Cortex-A7 cores makes use of 2MB and 512 KB respectively.

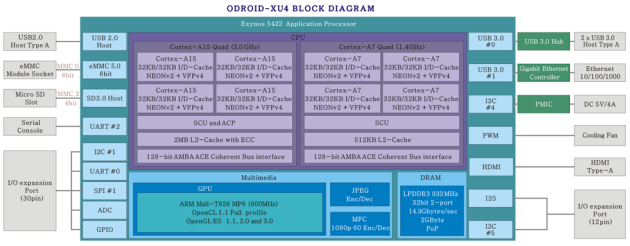

Fig. 1. ODroid XU4 board overview

A. Modeling and Development Strategy

Simulation of the ODROID-XU4/Exynos5422 will be integrated in to Gem5, that would closely resemble its CPU operating parameters. A SmartPower3 [5], power monitor unit will be used along ODROID-XU4 as represented in Figure. 2, to measure overall power consumption on the hardware, while most of the peripheral modules on it will be kept to reduce any variation or impact on the measured data. In addition, the perf [6] is used to gather PMC data-points. A summary of data-points being gathered for this modeling exercise is listed

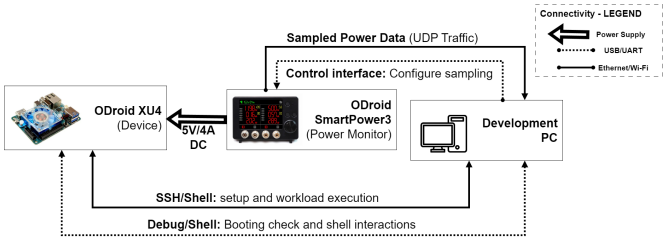

Fig. 2. Experiment setup for power data gathering from ODROID-XU4 [4] hardware

in Table I. These data-points are sampled at an interval of 100ms from both perf and SmartPower2 modules.

TABLE I
POWER AND PERFORMANCE FEATURE GATHERED FROM MENTIONED EXPERIMENT SETUP

Statistics Type	**Feature details**	
	Source	***Details***
CPU Clock Cycles	perf [6]	CPU cycles, us cycles, instructions, CPU frequency, CPU idle state statistics
Instruction Branches	perf	Branch instruction and speculative operation statistics
Caches	perf	Data/Instruction cache references, misses at L1, Last-Level-Cache levels
Board Level Power consumption	SmartPower3 [5]	Current, Power drawn from power supply.
Misc. Performance	perf	CPU Migrations, Context switches, Virtual memory

A set of preliminary workloads that would induce resource load for CPU and memory will be executed on the ODROID-XU4 device, while the power consumption and PMC data are simultaneously recorded. Few of the workloads that are being considered as listed in Table II. As of now, a total of 5 workloads have been employed. Furthermore, integration of SPEC2017 will allow inclusion of up to 43 feasible benchmarks to improve quantity of data.

TABLE II
LIST OF WORKLOADS BEING USED FOR DATA GATHERING AND VALIDATION

Workload Type	**Workload details and status of integration**	
	Workloads	***Integrated***
Stress Test	stress command [7]	✓
Video Encoding	ffmpeg encode [7]	✓
File Compression	gzip, bzip2, xz on complex datasets [8]	✓
Benchmark Suite	SPEC2017 CPU Benchmarks [9]	*Planned*

III. PHASE-2 PROGRESS

So far, team has completed, ramping up in to Gem5 simulator and its internals. In terms of actual hardware data gathering, the experiment setup shown in Figure 2 is established and data gathering of integrated workloads mentioned in Table II on ODROID-XU4 hardware is also completed as well.

Mathematical modeling with the data obtained is progressing, we are expecting to arrive at the empirical mathematical model soon and will be integrated in to the simulated Gem5 Exynos5422 instance for validation and further refinement.

IV. DISCUSSION ON PHASE-2 OUTCOMES

In terms workload execution, these workloads can get executed on any of the available CPU cores in Big and Little clusters, thereby greatly influencing the runtime performance and the power consumption behavior of the same workload. This can be a problem on accuracy of the empirical model being developed. In order avoid the same, we will be restricting execution of workloads to specific code by making use of affinity management primitives available in Linux.

The variations in power consumption seems to be also being influenced by the CPU Dynamic Clock Performance Governors [10] and associated modules in Linux Performance management. We may investigate in to the influence of one or more governors on the power consumption and integrate the same in to the empirical model being developed.

V. NEXT STEP

For integrating an empirical power model in to Gem5, the key features will be identified through feature engineering on obtained data-set, along with the coefficients required in to the same. The CPU model available in Gem5, will be extended to closely resemble the specification of Cortex-A15 and Cortex A-7 CPU cores.

With SPEC2017 workloads, further more data will be gathered covering CPU frequencies of different cores/clusters influencing power consumption, so as to improve accuracy of the power model against ODROID-XU4.

REFERENCES

[1] A. Akram and L. Sawalha, "A survey of computer architecture simulation techniques and tools," *IEEE Access*, vol. 7, pp. 78 120–78 145, 2019.

[2] A. Inc., ""big. little technology: The future of mobile", white paper," ONLINE, 2013. [Online]. Available: https://www.arm.com/

[3] B. K. Reddy, M. J. Walker, D. Balsamo, S. Diestelhorst, B. M. Al-Hashimi, and G. V. Merrett, "Empirical cpu power modelling and estimation in the gem5 simulator," *2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pp. 1–8, 2017. [Online]. Available: https://api.semanticscholar.org/CorpusID:10100084

[4] "Odroid-xu4: Big.little development board," Apr 2023. [Online]. Available: https://wiki.odroid.com/odroid-xu4/odroid-xu4

[5] "Smartpower3: Power monitor," May 2023. [Online]. Available: https://wiki.odroid.com/accessory/power_supply_battery/smartpower3

[6] "Chapter 8 - perf," in *Power and Performance*, J. Kukunas, Ed. Boston: Morgan Kaufmann, 2015, pp. 137–165. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128007266000082

[7] A. L. Wiki, "Stress testing," ONLINE, Aug 2023. [Online]. Available: https://wiki.archlinux.org/title/Stress_testing

[8] P. PeaZip project TOS, "Compression benchmark: 7-zip, peazip, winrar, winzip comparison," ONLINE, Aug 2023. [Online]. Available: https://peazip.github.io/peazip-compression-benchmark.html

[9] J. Bucek, K.-D. Lange, and J. v. Kistowski, "Spec cpu2017: Next-generation compute benchmark," in *Companion of the 2018 ACM/SPEC International Conference on Performance Engineering*, ser. ICPE '18. New York, NY, USA: Association for Computing Machinery, 2018, p. 41–42. [Online]. Available: https://doi.org/10.1145/3185768.3185771

[10] C. Scordino, L. Abeni, and J. Lelli, “Energy-aware real-time scheduling in the linux kernel,” in *Proceedings of the 33rd Annual ACM Symposium on Applied Computing*, ser. SAC ’18. New York, NY, USA: Association for Computing Machinery, 2018, p. 601–608. [Online]. Available: https://doi.org/10.1145/3167132.3167198