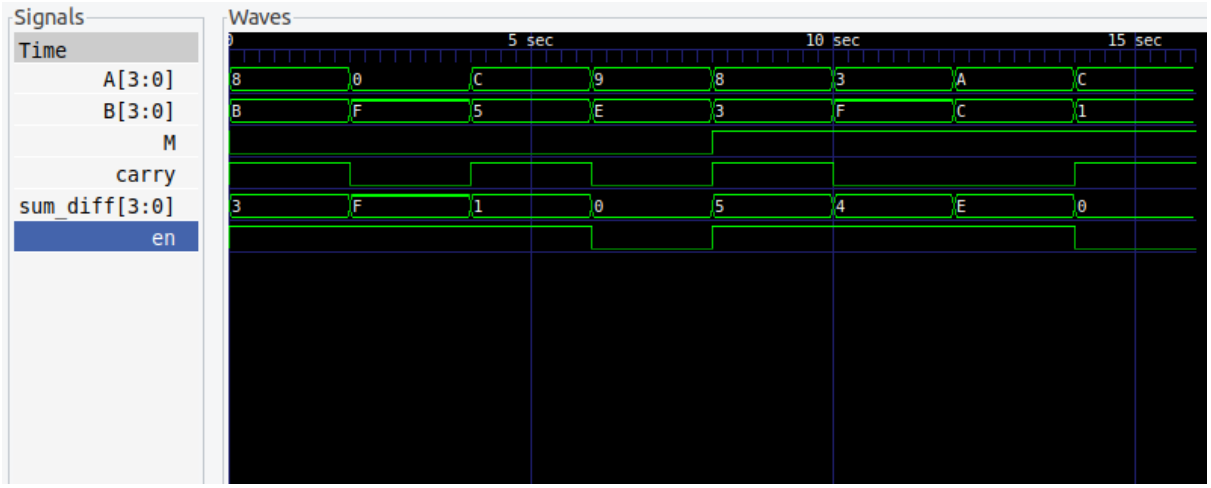
VLSI Project Monsoon 2023

Name:Vaishnavi Poldasu

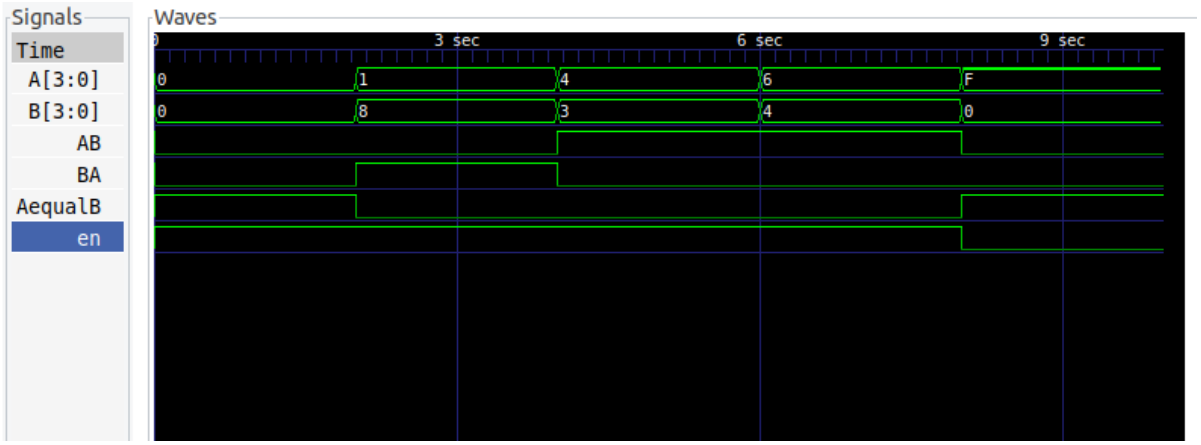
Roll No:2022102068

Verilog:

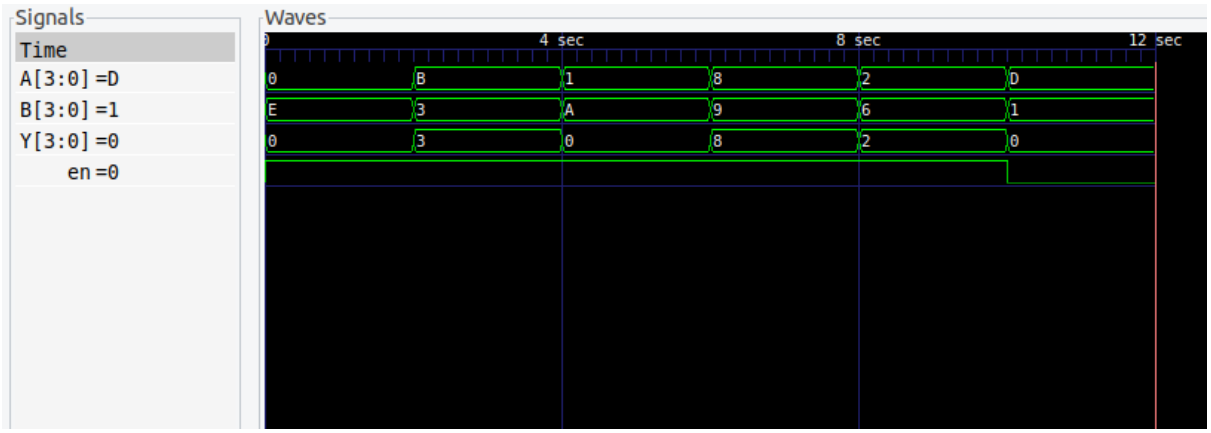
Adder/Subtractor:



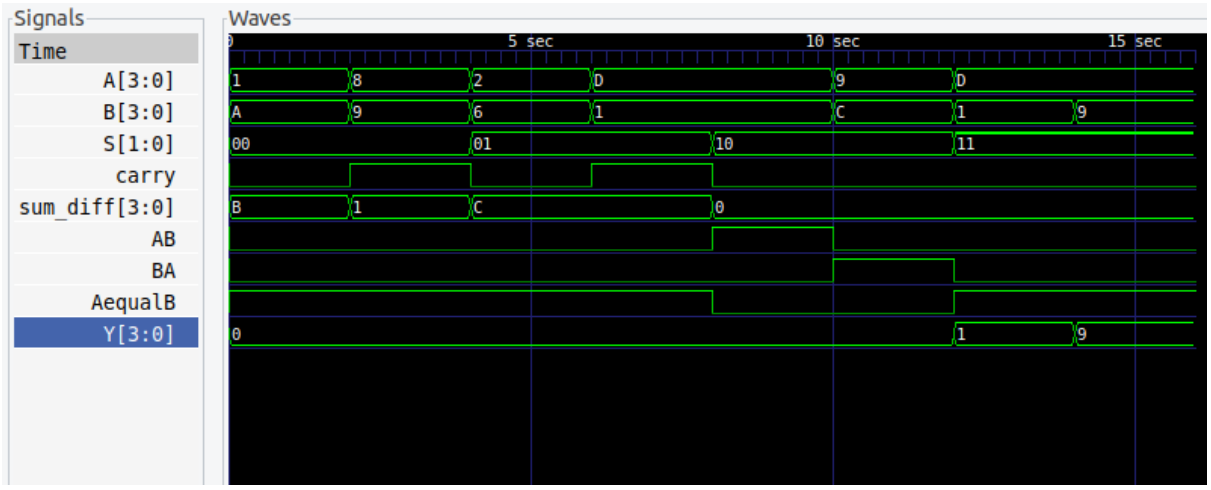
Comparator:



AND Block:



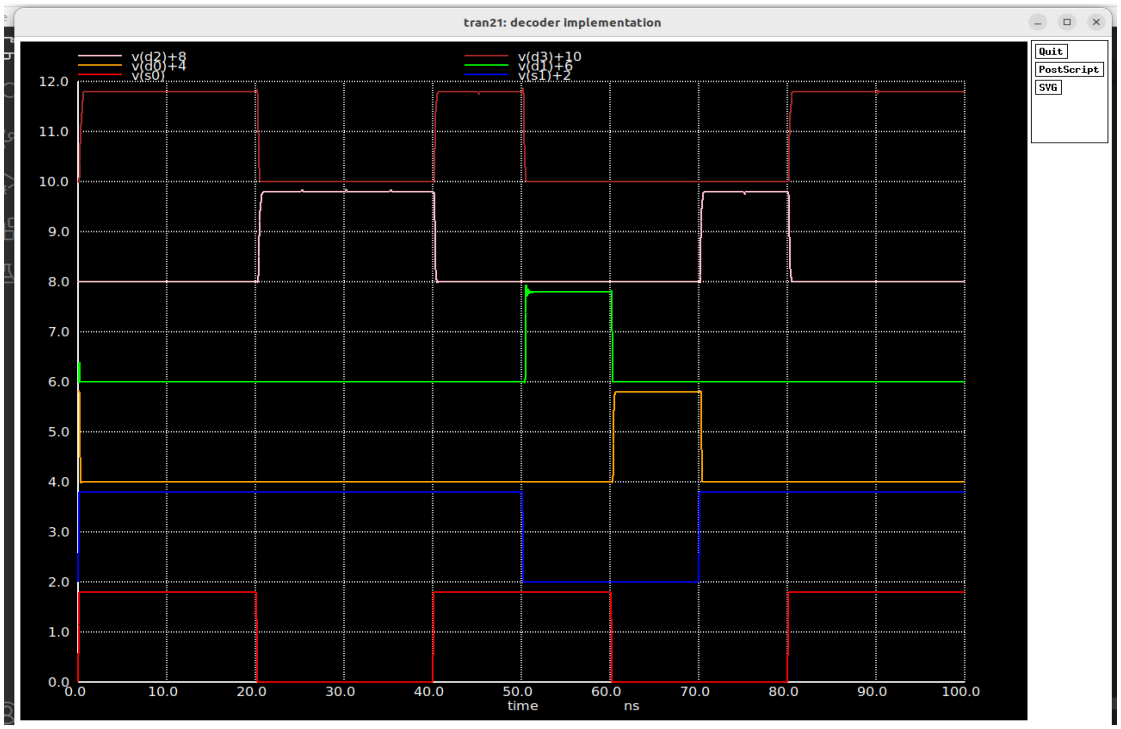
ALU Block:



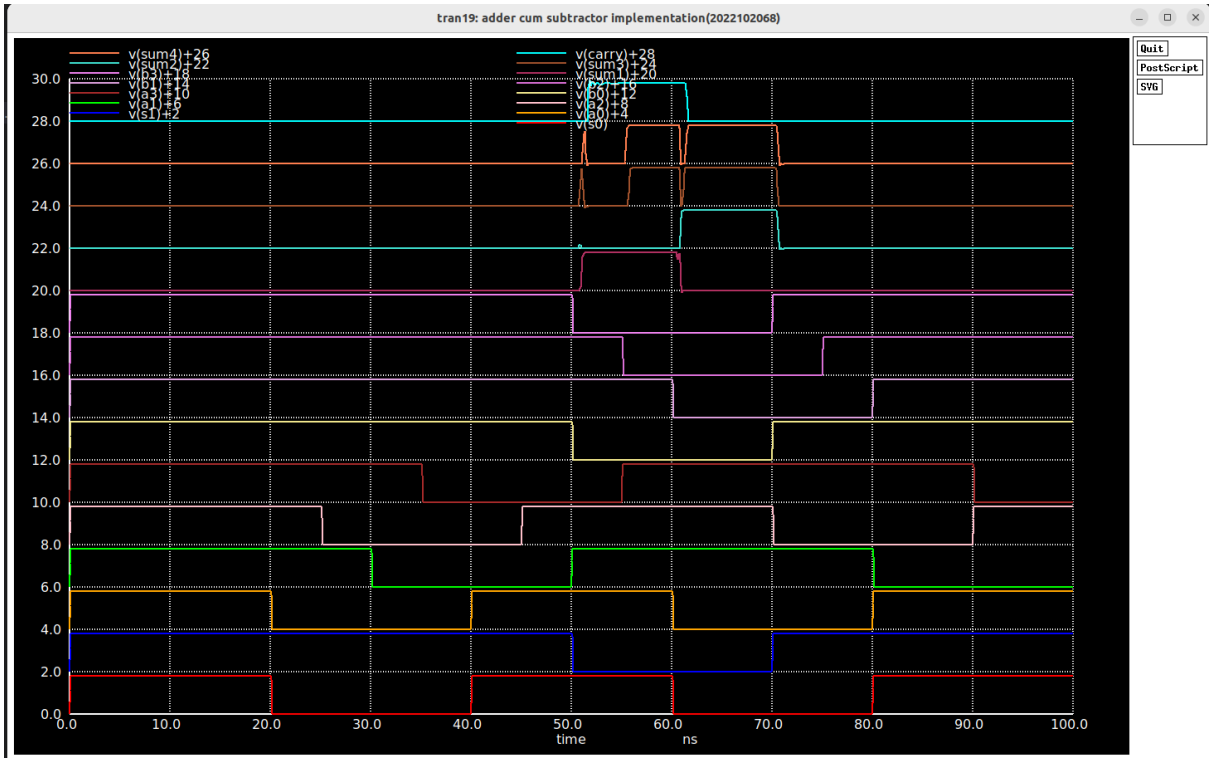
Ngspice:

In ngspice circuits, the overshoots resulted in the outputs due to delay in inputs has been resolved by taking appropriate output capcitors.Subcircuits are taken for full adder for simplifying the entire circuit.

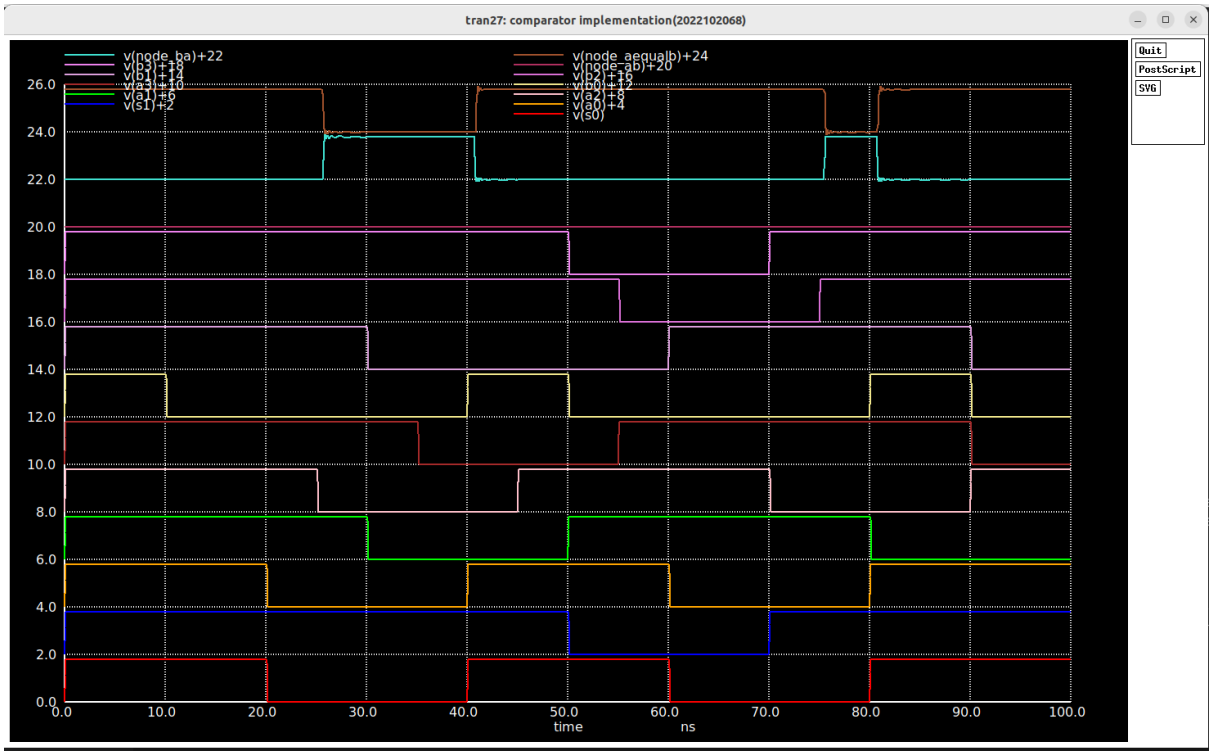
2:4 Decoder:



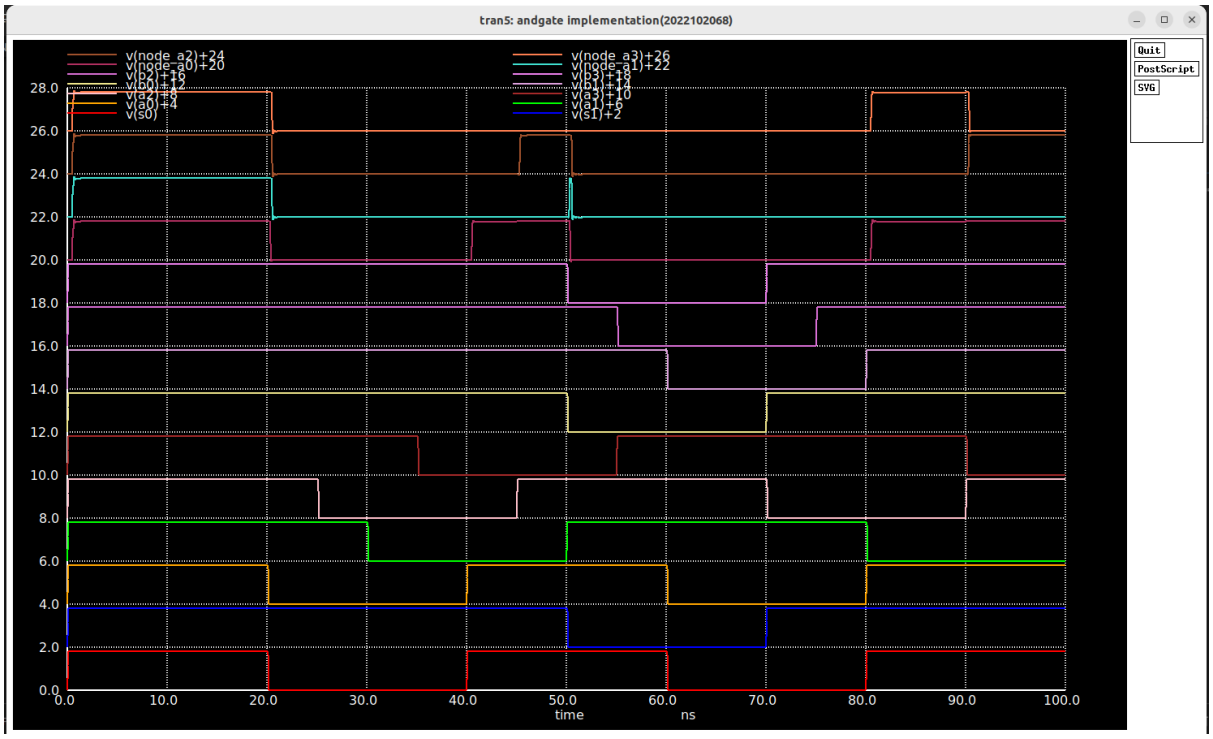
Adder/Subtractor:



Comparator:



AND Block:



MAGIC Layout:

→For layouts,first all the required blocks are made individually to check their working then all of the layouts are joined together in single layout with single VDD and GND.

→The contacts have been made in order polysilicon-metal1-metal2 and appropriate contacts have been made to avoid any floating nodes after extraction.

→After entire ALU is built it is extracted and ngspice file is been created in order to plot the outputs and for delay analysis.

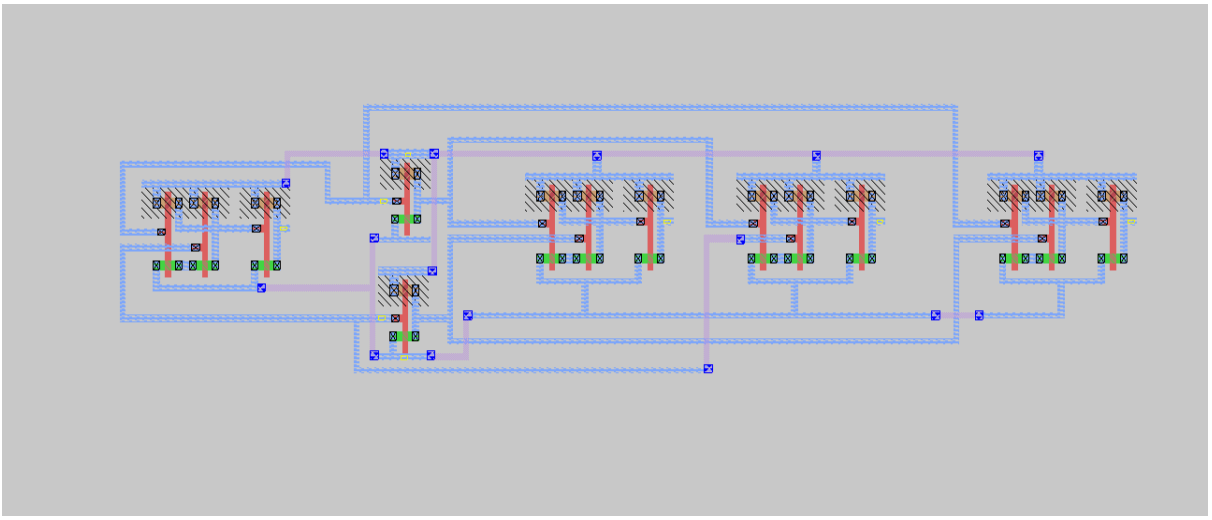
→The technology file TSMC_180nm and SCN6M_DEEP.09.tech27 files are included in the extracted file.

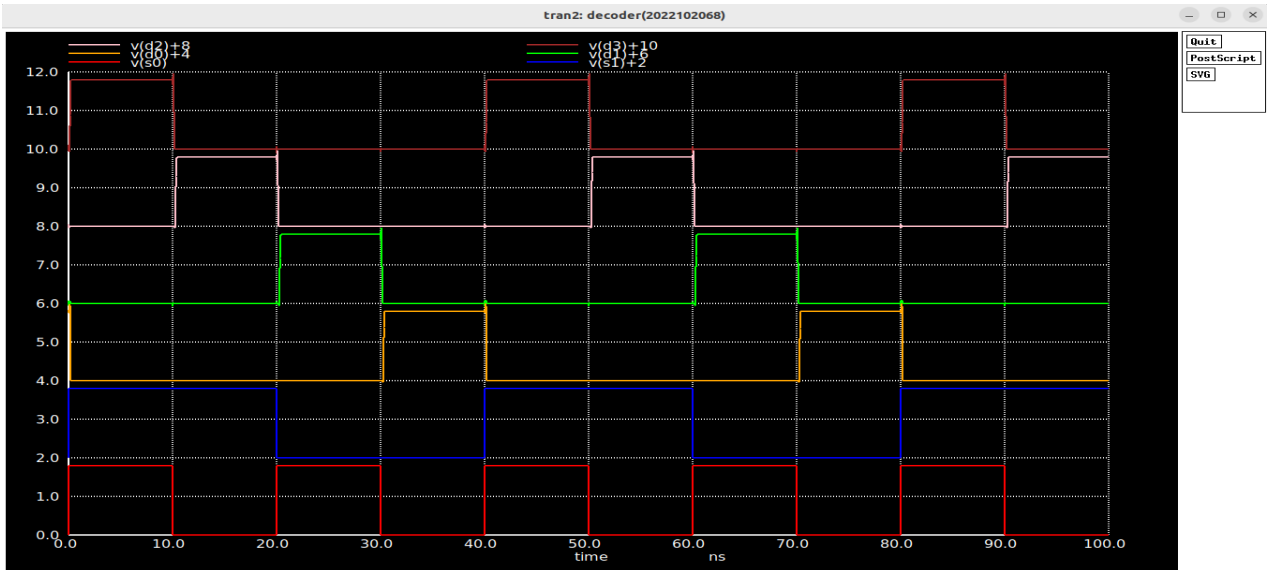
→The decoder inputs and 4 bit inputs are added to the SPICE file along with the plot and delay analysis part and nfet,pfet are changed to CMOSN and CMOSP repsectively with regard to TSMC_180nm file

→Python files are made for delay analysis part to reduce the complexity of finding delays for all possible input and output combinations.

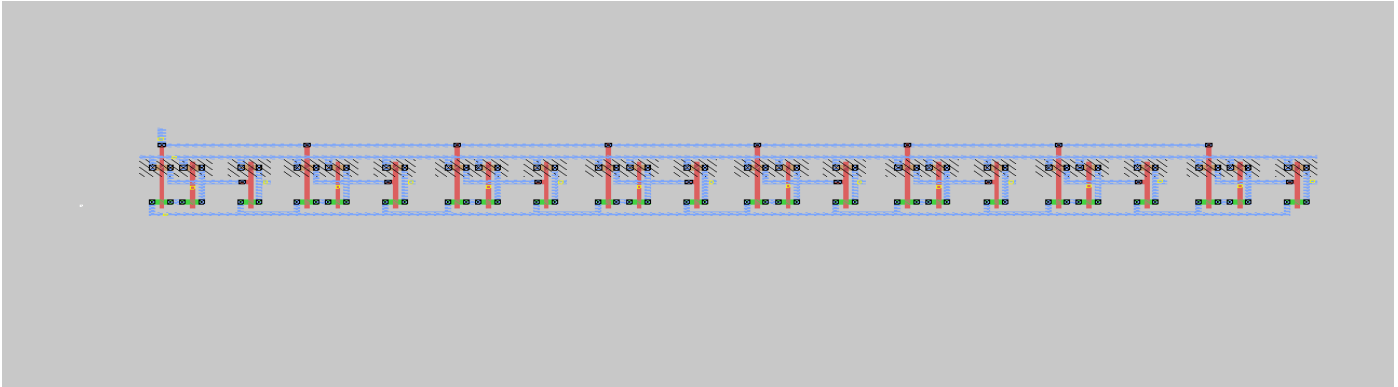
→From delay analysis,the critical path is determined,which indicates the longest delay path taken.

2:4 Decoder:

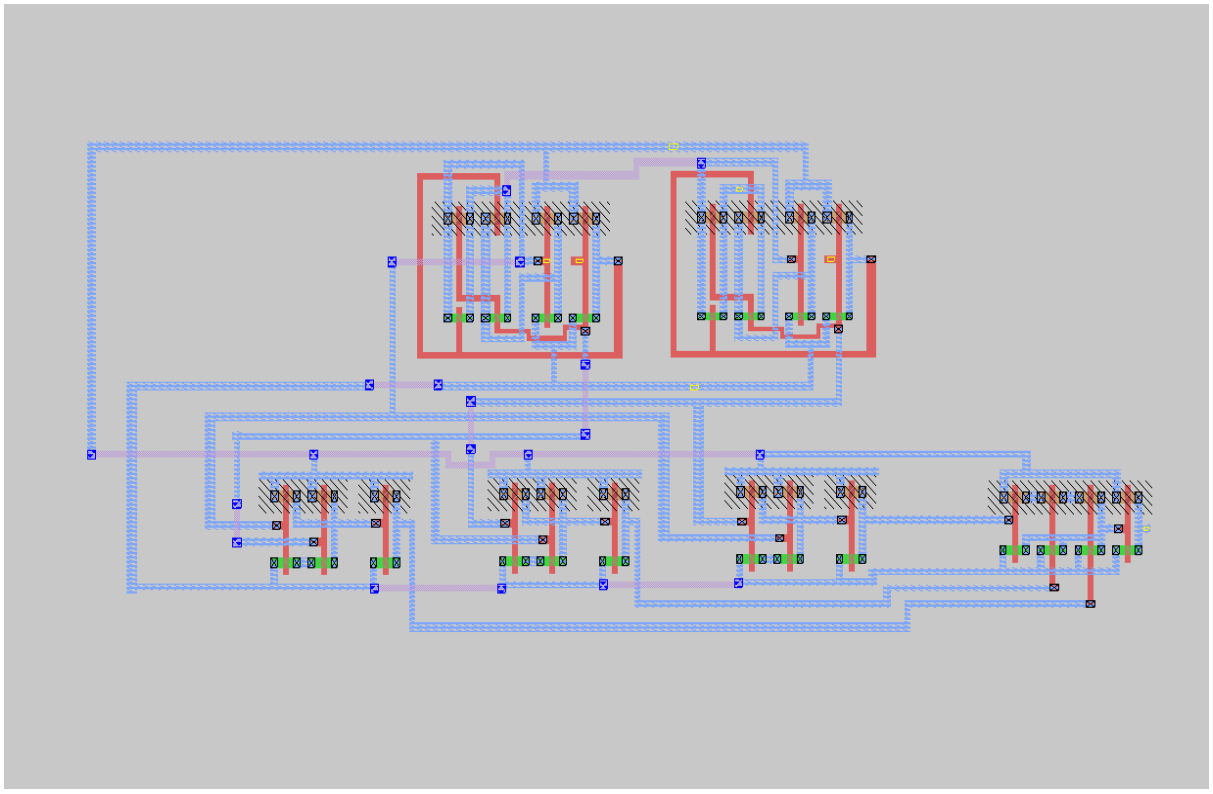


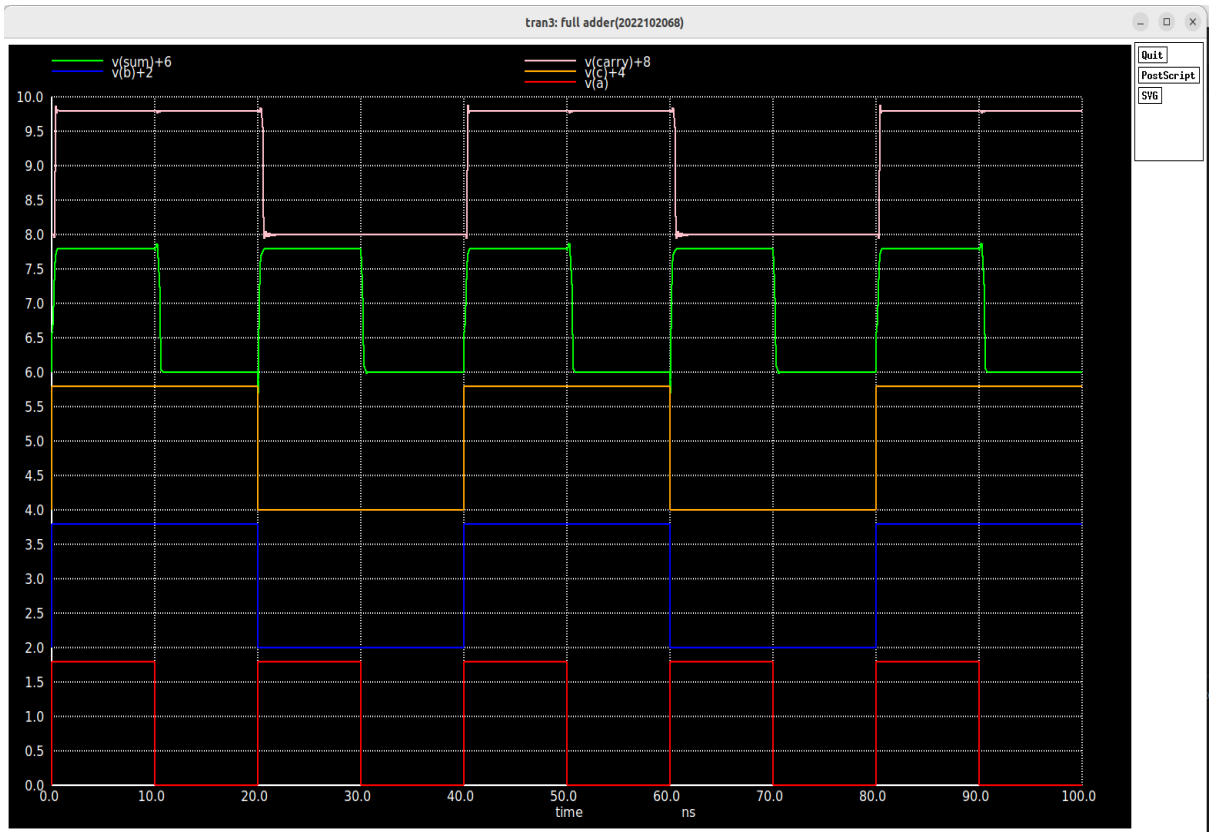


Enable block:

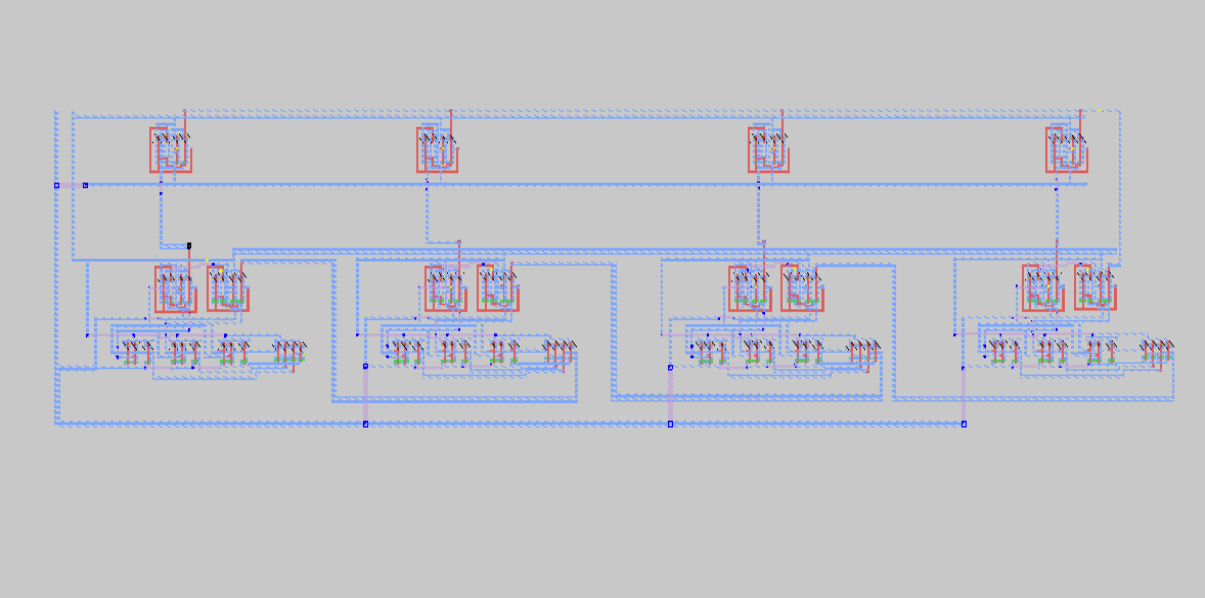


Full Adder:

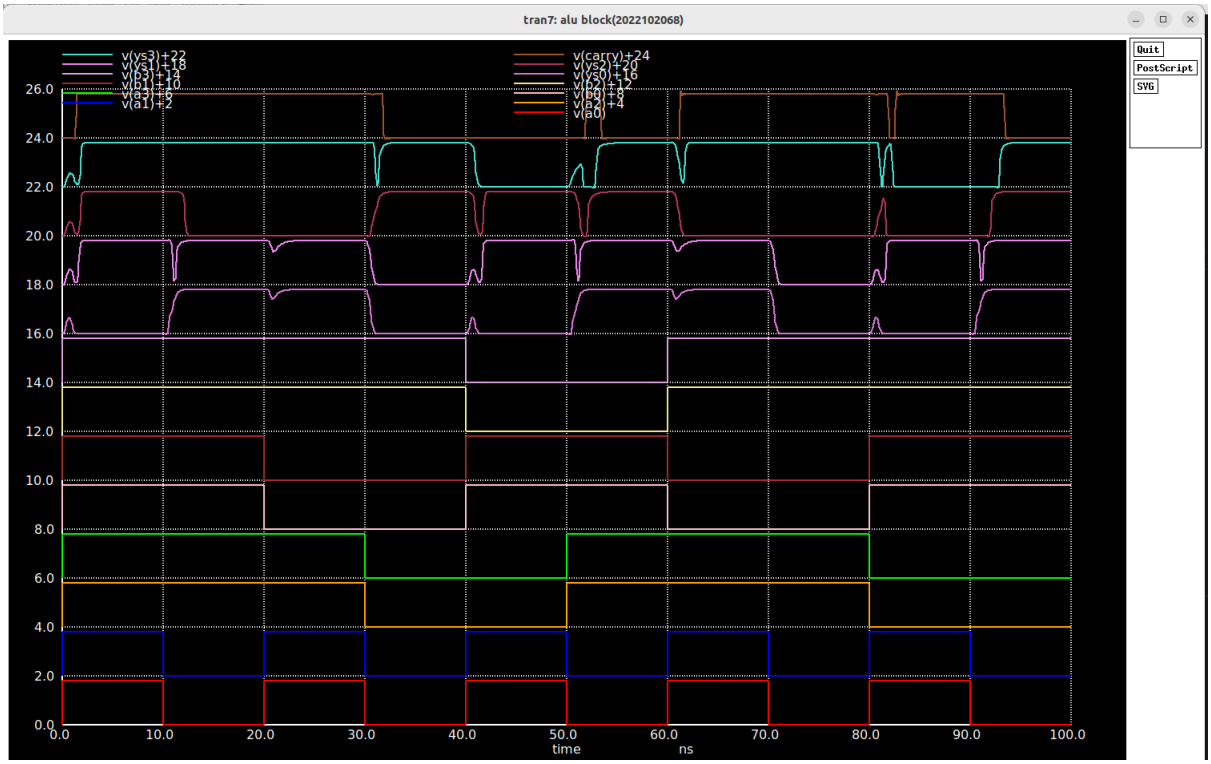



tran3: full adder(2022102068)
v(sum)+6
v(b)+2
v(carry)+8
v(c)+4
v(a)
Quit
PostScript
SVG
10.0
9.5
9.0
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
ns

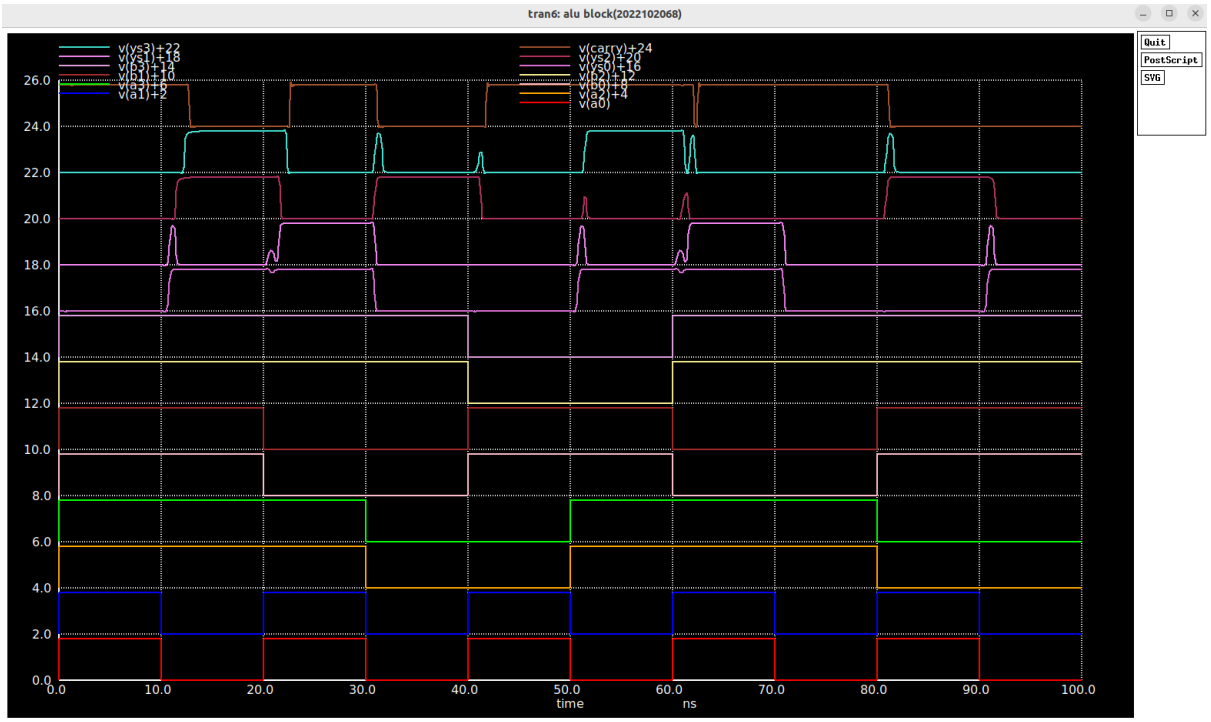
Adder/Subtractor:



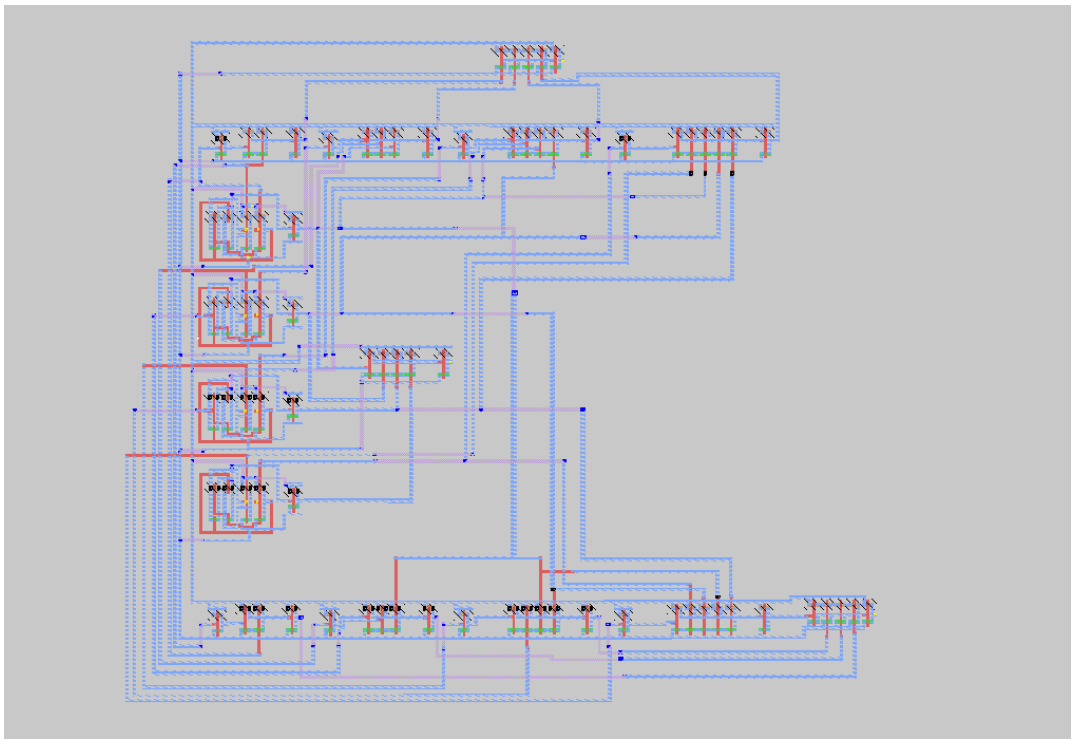
Adder:

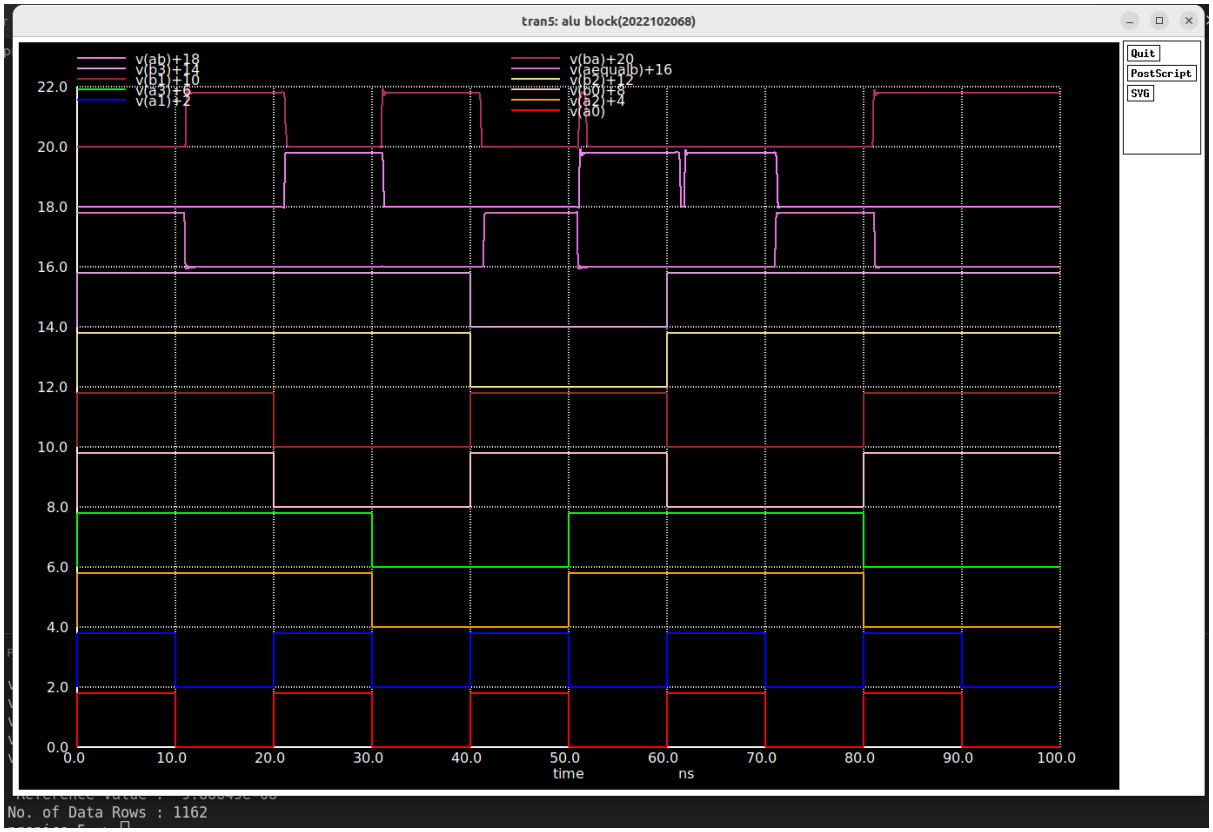


Subtractor:

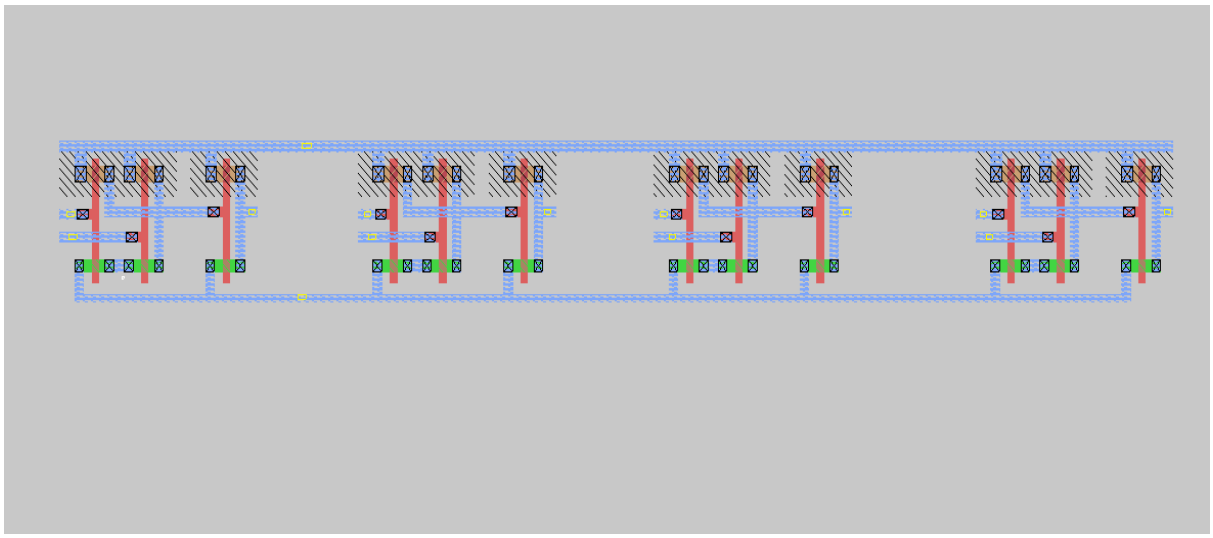


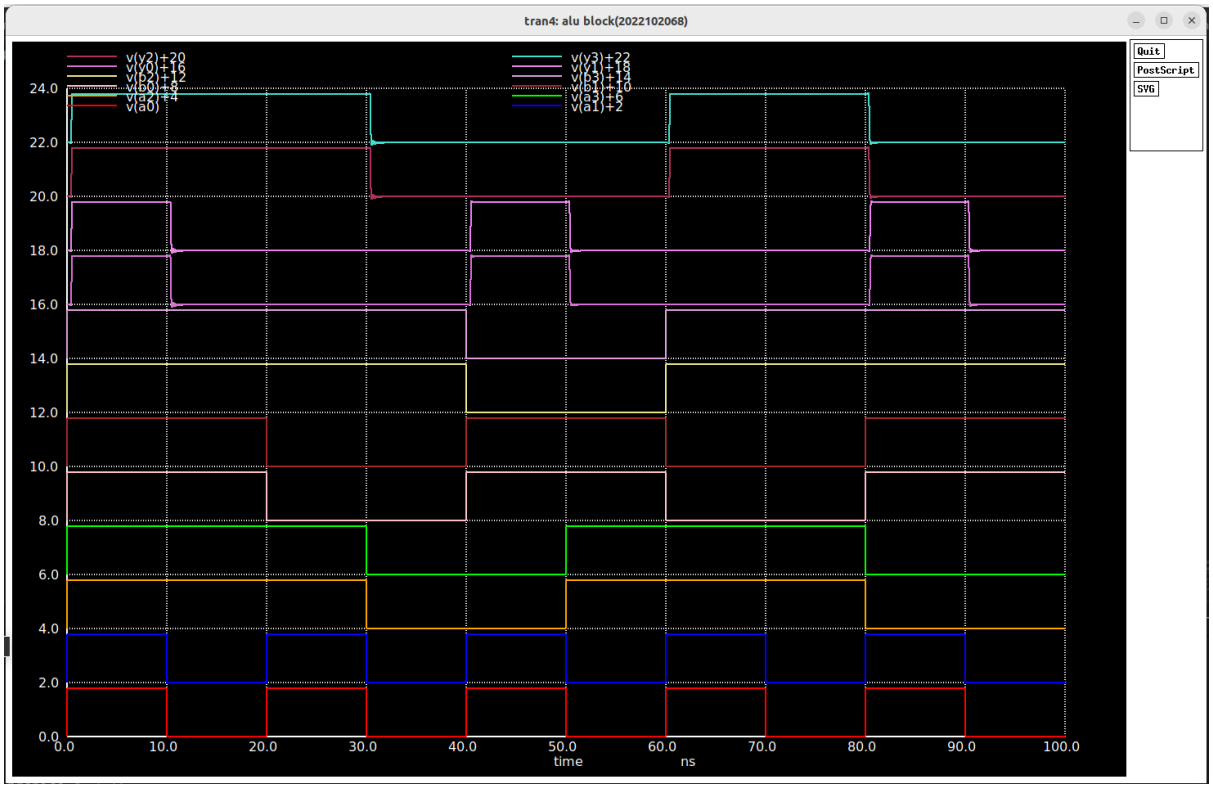
Comparator:



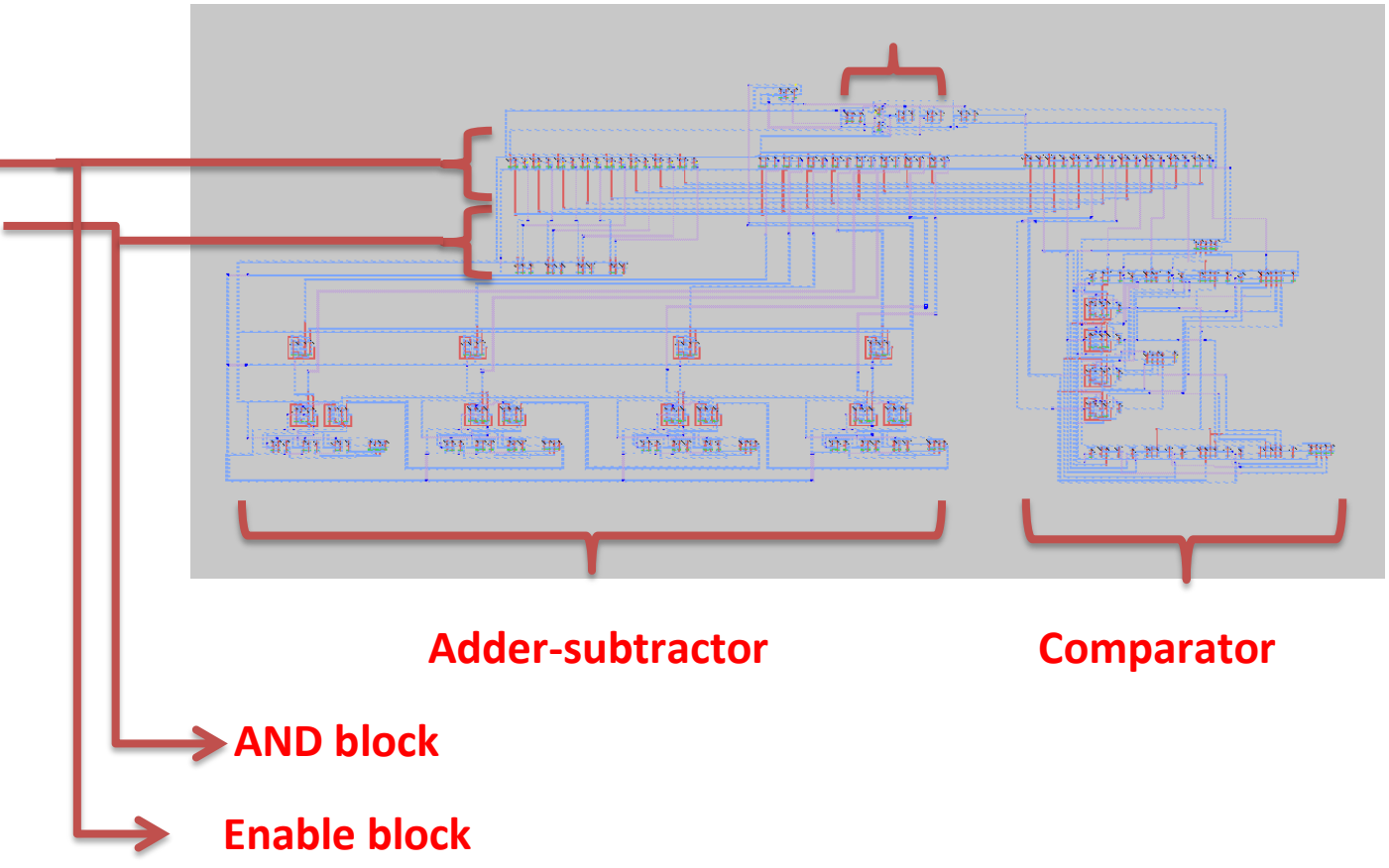

tran5: alu block(2022102068)
Quit
PostScript
SVG
v(ab)+18
v(b3)+14
v(b1)+10
v(a3)+6
v(a1)+2
v(ba)+20
v(aequalb)+16
v(b2)+12
v(b0)+8
v(a2)+4
v(a0)
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
ns
No. of Data Rows : 1162

AND Block:




tran4: alu block(2022102068)
Quit
PostScript
SVG
v(y2)+20
v(y0)+16
v(b2)+12
v(b0)+8
v(a2)+4
v(a0)
v(y3)+22
v(y1)+18
v(b3)+14
v(b1)+10
v(a3)+6
v(a1)+2
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
ns

ALU BLOCK:


Decoder
Adder-subtractor
Comparator
AND block
Enable block

Delay Analysis:

Adder Block:

delay_analysis > add_output.txt

```
tpd                    =  7.20384e-10 input = A0 output = YS0
tpd                    =  8.24070e-10 input = A0 output = YS1
tpd                    =  9.21338e-10 input = A0 output = YS2
tpd                    =  9.81066e-10 input = A0 output = YS3
tpd                    =  7.20384e-10 input = A1 output = YS0
tpd                    =  8.24070e-10 input = A1 output = YS1
tpd                    =  9.21338e-10 input = A1 output = YS2
tpd                    =  9.81066e-10 input = A1 output = YS3
tpd                    =  7.20384e-10 input = A2 output = YS0
tpd                    =  8.24070e-10 input = A2 output = YS1
tpd                    =  9.21338e-10 input = A2 output = YS2
tpd                    =  9.81066e-10 input = A2 output = YS3
tpd                    =  7.20384e-10 input = A3 output = YS0
tpd                    =  8.24070e-10 input = A3 output = YS1
tpd                    =  9.21338e-10 input = A3 output = YS2
tpd                    =  9.81066e-10 input = A3 output = YS3
tpd                    =  9.68814e-10 input = B0 output = YS0
tpd                    =  1.01340e-09 input = B0 output = YS1
tpd                    =  1.04293e-09 input = B0 output = YS2
tpd                    =  1.05596e-09 input = B0 output = YS3
tpd                    =  9.68814e-10 input = B1 output = YS0
tpd                    =  1.01340e-09 input = B1 output = YS1
tpd                    =  1.04293e-09 input = B1 output = YS2
tpd                    =  1.05596e-09 input = B1 output = YS3
tpd                    =  9.68814e-10 input = B2 output = YS0
tpd                    =  1.01340e-09 input = B2 output = YS1
tpd                    =  1.04293e-09 input = B2 output = YS2
tpd                    =  1.05596e-09 input = B2 output = YS3
tpd                    =  9.68814e-10 input = B3 output = YS0
tpd                    =  1.01340e-09 input = B3 output = YS1
tpd                    =  1.04293e-09 input = B3 output = YS2
tpd                    =  1.05596e-09 input = B3 output = YS3

```

Method of Implementation:

→In order to get maximum combinations of delays(i.e, 32),two inputs files have been created keeping the enable constant.

→In,first file all the 4-bit B input is kept constant(i.e, dc 0) and 4-bit A input is given as pulse(i.e, getting values of 0,1) and for the second file vice-versa is taken.

→So,in the two files the input and output combination will be of the type (1111 + 0000 = 1111).

→So,as one of the inputs rises keeping other constant ,the output also rises.Hence the delay type is taken to be average of **rise-rise** and **fall-fall.**

→On considering the delay values,the overall maximum delay is occurred for B3-YS3 combination with value of 1.05596e^-09

→Each input bit and corresponding output delays are:

A0-YS0 :7.20384e^-10

A1-YS1 :8.24070e^-10

A2-YS2 :9.21338e^-10

A3-YS3 :9.81066e^-10

B0-YS0 :9.68814e^-10

B1-YS1 :1.01340e^-09

B2-YS2 :1.04293e^-09

B3-YS3 :1.05596e^-09

Subtractor Block:

delay_analysis > sub_output.txt

```
tpd                    =  9.30245e-10 input = A0 output = YS0
tpd                    =  1.04290e-09 input = A0 output = YS1
tpd                    =  1.12014e-09 input = A0 output = YS2
tpd                    =  1.18577e-09 input = A0 output = YS3
tpd                    =  9.30245e-10 input = A1 output = YS0
tpd                    =  1.04290e-09 input = A1 output = YS1
tpd                    =  1.12014e-09 input = A1 output = YS2
tpd                    =  1.18577e-09 input = A1 output = YS3
tpd                    =  9.30245e-10 input = A2 output = YS0
tpd                    =  1.04290e-09 input = A2 output = YS1
tpd                    =  1.12014e-09 input = A2 output = YS2
tpd                    =  1.18577e-09 input = A2 output = YS3
tpd                    =  9.30245e-10 input = A3 output = YS0
tpd                    =  1.04290e-09 input = A3 output = YS1
tpd                    =  1.12014e-09 input = A3 output = YS2
tpd                    =  1.18577e-09 input = A3 output = YS3
tpd                    =  1.16516e-09 input = B0 output = YS0
tpd                    =  1.19065e-09 input = B0 output = YS1
tpd                    =  1.17944e-09 input = B0 output = YS2
tpd                    =  1.19029e-09 input = B0 output = YS3
tpd                    =  1.16516e-09 input = B1 output = YS0
tpd                    =  1.19065e-09 input = B1 output = YS1
tpd                    =  1.17944e-09 input = B1 output = YS2
tpd                    =  1.19029e-09 input = B1 output = YS3
tpd                    =  1.16516e-09 input = B2 output = YS0
tpd                    =  1.19065e-09 input = B2 output = YS1
tpd                    =  1.17944e-09 input = B2 output = YS2
tpd                    =  1.19029e-09 input = B2 output = YS3
tpd                    =  1.16516e-09 input = B3 output = YS0
tpd                    =  1.19065e-09 input = B3 output = YS1
tpd                    =  1.17944e-09 input = B3 output = YS2
tpd                    =  1.19029e-09 input = B3 output = YS3

```

Method of Implementation:

→In order to get maximum combinations of delays(i.e, 32),two inputs files have been created keeping the enable constant.

→In,first file all the 4-bit B input is kept constant(i.e, dc 0) and 4-bit A input is given as pulse(i.e, getting values of 0,1) and for the second file 4-bit A input is kept constant(i.e, dc SUPPLY) and 4-bit B input as pulse(since A-B = 1111 – pulse).

→So,whenever the B = 0000 ,output will be 1111 and when B=1111,output will be 0000.Hence,the delays are calculated by using the average of **rise-fall** and **fall-rise** for second file and **rise-rise** and **fall-fall** average for first file.

→ On considering the delay values,the overall maximum delay is occurred for B1-YS1 combination with value of 1.19065e^-09

→Each input bit and corresponding output delays are:

A0-YS0 :9.30245e^-10

A1-YS1 :1.04290e^-09

A2-YS2 :1.12014e^-09

A3-YS3 :1.18577e^-09

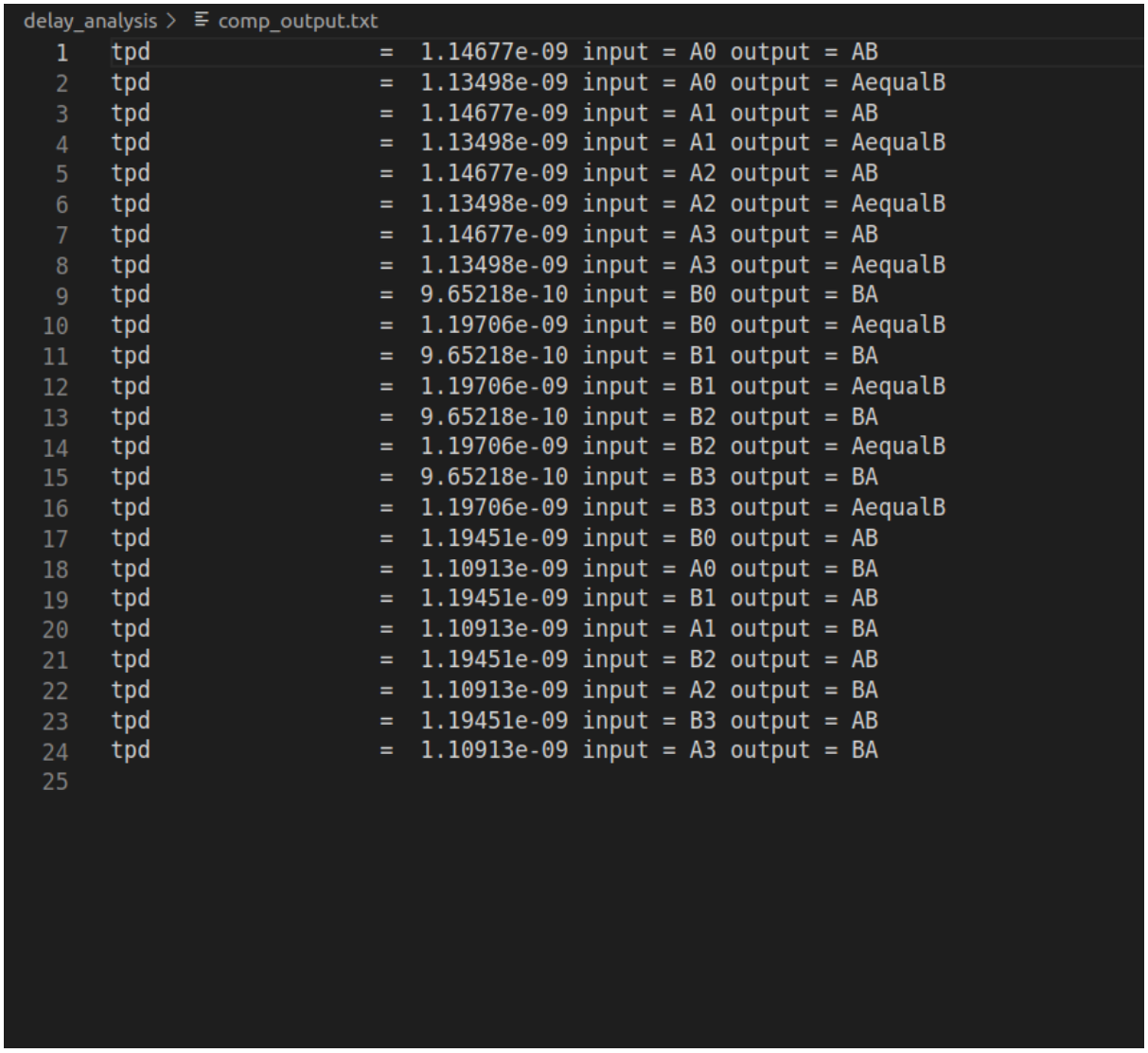
B0-YS0 :1.16516e^-09

B1-YS1 :1.19065e^-09

B2-YS2 :1.17944e^-09

B3-YS3 :1.19029e^-09

Comparator Block:



Method of Implementation:

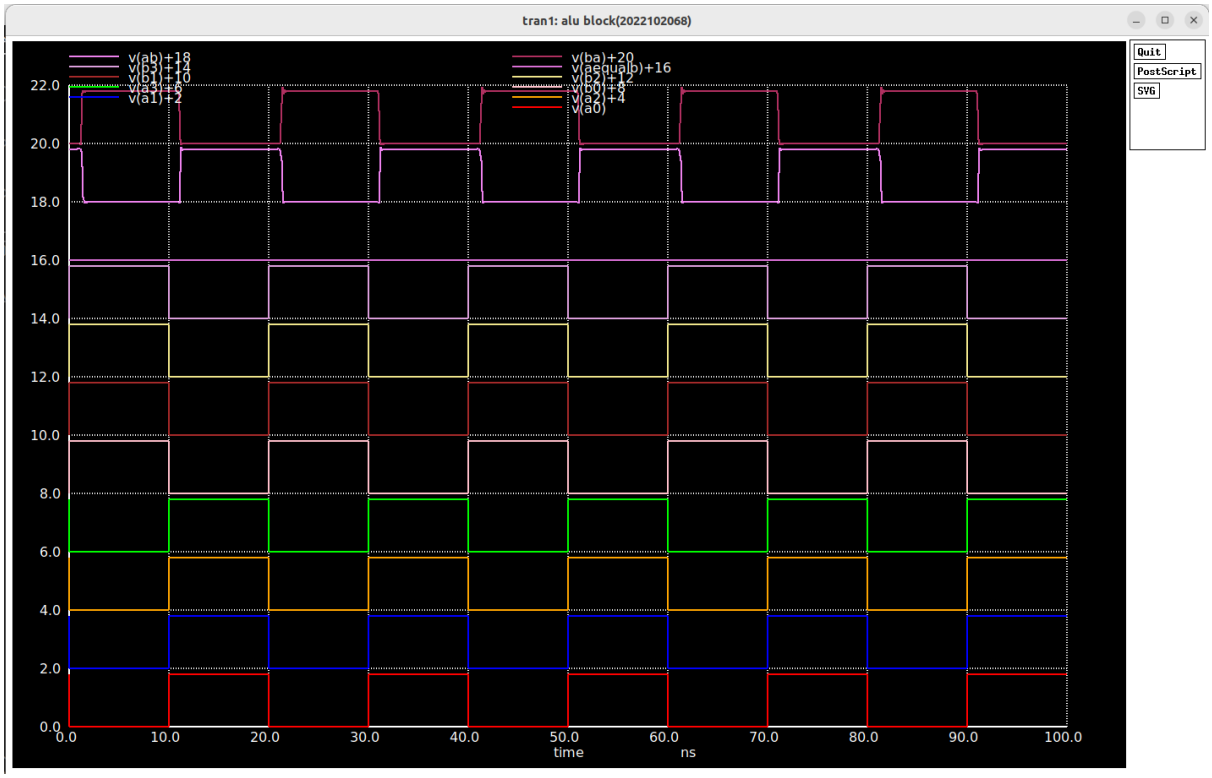
→In order to get maximum combinations of delays(i.e, 24),three inputs files have been created keeping the enable constant.

→In,first file all the 4-bit B input is kept constant(i.e, dc 0) and 4-bit A input is given as pulse(i.e, getting values of 0,1) and for the second file vice-versa is taken.So, from first file where either A>B (when A=1111) or A=B(when A=0000)

hence we can calculate delays for A and AequalB(**rise-fall** and **fall-rise**) ,A and AB.(**rise-rise** and **fall-fall**)

→Similarly for second file we get either B>A then delay calculated for B and BA(**rise-rise** and **fall-fall**) or A=B then delay calculated for B and AequalB(**rise-fall** and **fall-rise**).

→In order to calculate delays for B-AB and A-BA,third input file is taken where both the inputs are given as pulses but complementary of each other so the inputs will be either 1111-0000 or 0000-1111 (A-B) so **rise-fall** and **fall-rise** average is taken.Third input file is shown below:



→ On considering the delay values,the overall maximum delay is occurred for B-AequalB combination with value of 1.19706e^-09

And Block:

delay_analysis > and_output.txt

```
tpd                    =  3.68847e-10 input = A0 output = Y0
tpd                    =  3.71048e-10 input = A0 output = Y1
tpd                    =  3.71090e-10 input = A0 output = Y2
tpd                    =  3.71530e-10 input = A0 output = Y3
tpd                    =  3.68847e-10 input = A1 output = Y0
tpd                    =  3.71048e-10 input = A1 output = Y1
tpd                    =  3.71090e-10 input = A1 output = Y2
tpd                    =  3.71530e-10 input = A1 output = Y3
tpd                    =  3.68847e-10 input = A2 output = Y0
tpd                    =  3.71048e-10 input = A2 output = Y1
tpd                    =  3.71090e-10 input = A2 output = Y2
tpd                    =  3.71530e-10 input = A2 output = Y3
tpd                    =  3.68847e-10 input = A3 output = Y0
tpd                    =  3.71048e-10 input = A3 output = Y1
tpd                    =  3.71090e-10 input = A3 output = Y2
tpd                    =  3.71530e-10 input = A3 output = Y3
tpd                    =  3.53709e-10 input = B0 output = Y0
tpd                    =  3.50910e-10 input = B0 output = Y1
tpd                    =  3.50335e-10 input = B0 output = Y2
tpd                    =  3.50104e-10 input = B0 output = Y3
tpd                    =  3.53709e-10 input = B1 output = Y0
tpd                    =  3.50910e-10 input = B1 output = Y1
tpd                    =  3.50335e-10 input = B1 output = Y2
tpd                    =  3.50104e-10 input = B1 output = Y3
tpd                    =  3.53709e-10 input = B2 output = Y0
tpd                    =  3.50910e-10 input = B2 output = Y1
tpd                    =  3.50335e-10 input = B2 output = Y2
tpd                    =  3.50104e-10 input = B2 output = Y3
tpd                    =  3.53709e-10 input = B3 output = Y0
tpd                    =  3.50910e-10 input = B3 output = Y1
tpd                    =  3.50335e-10 input = B3 output = Y2
tpd                    =  3.50104e-10 input = B3 output = Y3

```

Method of Implementation:

→In order to get maximum combinations of delays(i.e, 32),two inputs files have been created keeping the enable constant.

→In,first file all the 4-bit B input is kept constant(i.e, dc SUPPLY) and 4-bit A input is given as pulse(i.e, getting values of 0,1) and for the second file vice-versa is taken.(since output will be high if both inputs are high hence dc SUPPLY)

→So,whenever the B = 0000 ,output will be 0000 and when B=1111,output will be 1111,same for A.Hence,the delays are calculated by using **rise-rise** and **fall-fall** average for both files.

→ On considering the delay values,the overall maximum delay is occurred for A3-Y3 combination with value of 3.71530e^-10

→Each input bit and corresponding output delays are:

A0-Y0 :3.68847e^-10

A1-Y1 :3.71048e^-10

A2-Y2 :3.71090e^-10

A3-Y3 :3.71530e^-10

B0-Y0 :3.53709e^-10

B1-Y1 :3.50910e^-10

B2-Y2 :3.50335e^-10

B3-Y3 :3.50104e^-10

Observations:

The critical path,which is the longest path from start to end of the project.If we consider all the blocks the maximum delay occurs in the comparator block 1.19706e^-09s since comparator block has complex combinational circuit involving more logic gates and each gate contributing to delay which leads to overall increase in the delay.

Conclusion:

Hence, an ALU is designed which can perform addition,subtraction,comparison and ANDing of the two 4-bit inputs through magic layout and also the elays are calculated for each block to estimate the critical path. The functionality is also successfully verified using NGSPICE and Verilog.