Design for Testability

Mid Term Exam, Monsoon 2024

Instructions:

- This is a closed book exam. The students are allowed **one A4 sheet of handwritten** notes.
- The exam is for a duration of 90 minutes and 50 points.
- Answer legibly. Answer all parts of a question contiguously.
- No clarifications shall be given in the exam. If you have to make any assumptions, state those assumptions clearly. Points awarded will depend on the nature of the assumptions.

1. For the circuit shown in figure 1: [5+2+5=12 points]
   a. Derive the probability-based controllability and observability (COP) for each of the signal lines.
   b. Calculate the probability of detecting the "c s-a-0" fault.
   c. Use Boolean Difference method to find all the test vectors that can detect "c s-a-0" fault.

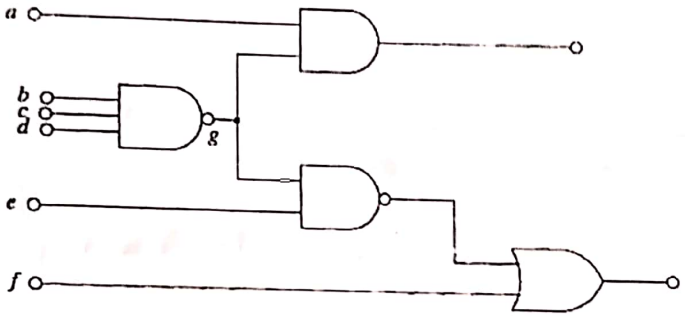

Figure 1

2. For the circuit shown in figure 2: [2+3+8+5=18 points]
   a. How many single stuck at faults and checkpoints do you see in the circuit?
   b. Draw the truth table for a 2-input XOR gate including the fault free and faulty outputs for each of the SSFs. Determine the equivalent and dominant set of faults for the XOR gate.
   c. Use D-algorithm to find a test pattern that detects the f s-a-1 fault in figure 2. List all the steps and tabulate the logic values for each signal, along with the comments (keywords) on what is being done in each step.
   d. Use fault simulation to determine which other faults can be detected by the test pattern obtained in part (c).

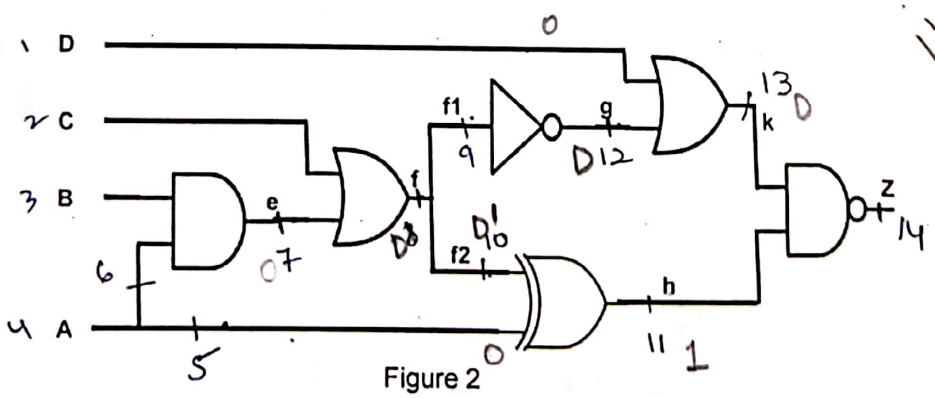

Figure 2

3. For the circuit in figure 3: [4+6=10 points]
   a. Compute the combinational SCOAP controllability and observability measures.
   b. Perform ATPG using PODEM algorithm for the h s-a-1 fault. List all the steps in the algorithm, including comments (keywords) on what is being done in each step.

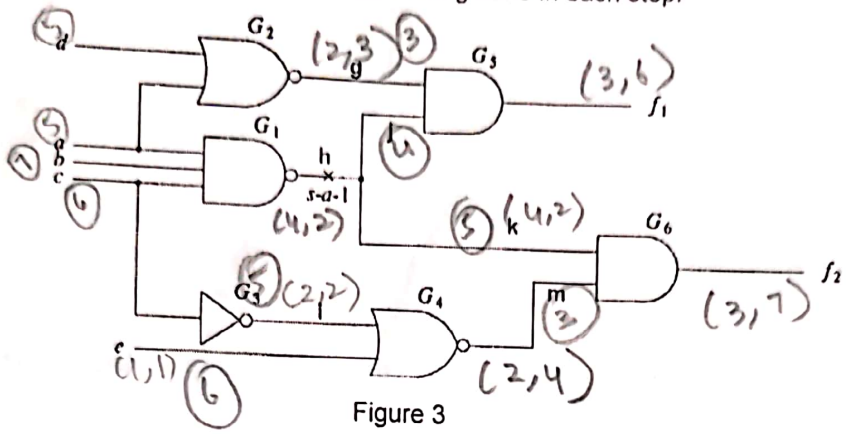

Figure 3

4. [2+3=5 points]
   a. List the differences between PODEM and FAN algorithms.
   b. For the circuit shown in Figure 4, indicate which of the signal lines are bound lines, free lines and head lines.

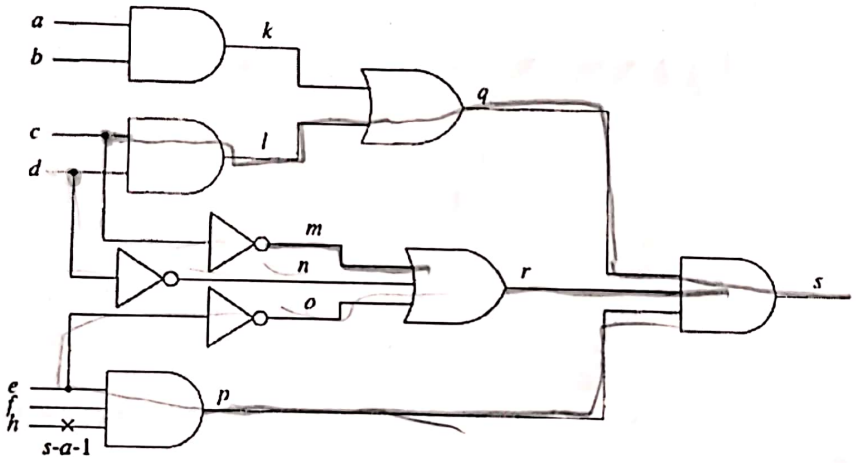

Figure 4

5. For the circuit shown in Figure 5, calculate the SCOAP combinational and sequential controllability and observability for each signal. No need to calculate the observability for the clock signal. [5 points]

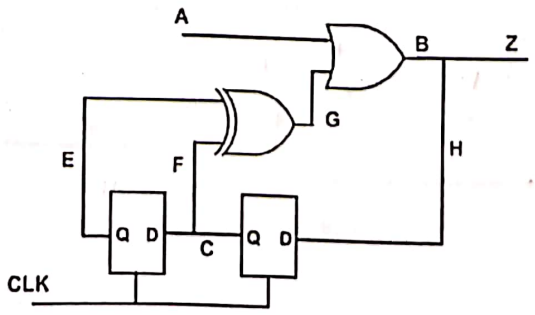

Figure 5