DFT Quiz -1

27th August 2024

Total: 40 Marks
Duration: 45 minutes

Instructions:

- This is a closed book exam.
- Answer legibly. Answer all parts of a question contiguously.
- If you have to make any assumptions, state those assumptions clearly. Points awarded will depend on the nature of the assumptions.

1. Answer the following questions:
   a. Differentiate between Verification, Validation and Testing. (3 Marks)
   b. Explain the difference between characterization test and production test. (2 Marks)
   c. State the main assumptions in the Single Stuck at Fault Model. (3 marks)
   d. How do we test for reliability in integrated circuits? (2 Marks)
   e. Differentiate between functional and structural faults. (2 Marks)
   f. Which fault would be best detected using IDDQ testing? (1 Mark)
   g. Which fault model is best suitable for testing a critical path in a high-speed digital circuit? (1 Mark)
   h. Which type of fault is the hardest to detect using traditional stuck-at-fault testing techniques? (1 Mark)

2. Answer the following questions for the circuit shown in Figure 1: (10 Marks)
   (a) What is the total number of **single** stuck-at faults in the circuit?
   (b) How many **multiple** stuck at faults are possible in the circuit?
   (c) What is the number of checkpoints in the circuit?
   (d) Derive the equivalence collapsed set of faults. List all faults that remain after equivalence collapsing.
   (e) Derive the dominance collapsed set of faults. List all faults that remain after equivalence and dominance collapsing.

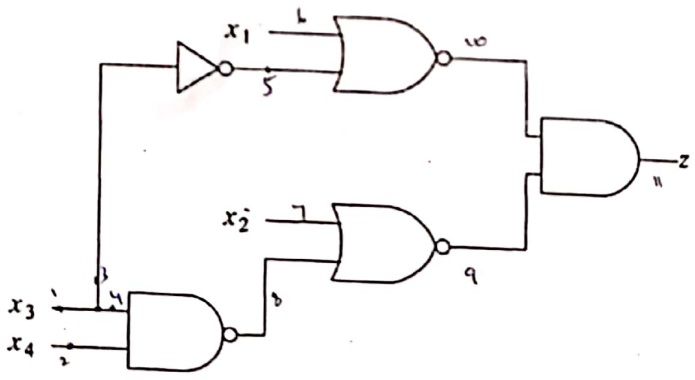

Figure 1

3. For the circuit in Figure 1, (5 Marks)

   Perform **Deductive Fault Simulation** and determine all faults that would be detected at the output z by the test pattern $x_1\, x_2\, x_3\, x_4$ = {1 1 1 0}. Clearly show the fault lists associated with each signal.

4. For the circuit in Figure 2: (10 Marks)

a. Perform **Concurrent fault simulation** to determine all the faults that would be detected by the test pattern abcde=10110.

b. For the same test pattern as in part a, perform **critical path tracing** and list the critical paths of the circuit (you might need to figure out if a stem is critical through analysis).

c. Determine all faults detected using critical path tracing.

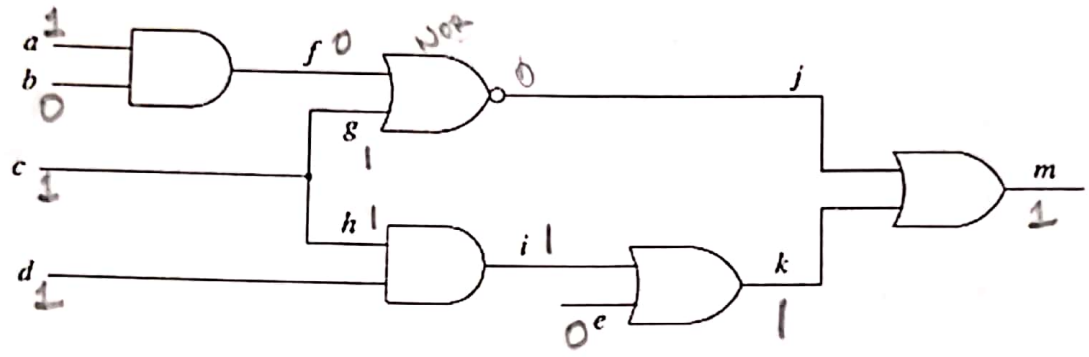

Figure 2