Design for Testability

Final Exam, Monsoon 2024

Instructions:

- This is a closed book exam. The students are allowed **one A4 sheet of handwritten notes.**
- The exam is for a duration of 3 hours and 100 points.
- Answer legibly. Answer all parts of a question contiguously.
- No clarifications shall be given in the exam. If you have to make any assumptions, state those assumptions clearly. Points awarded will depend on the nature of the assumptions.

1. Answer the following questions for the circuit in Figure 1: [3+4+3+5+5=20 points]
   a. What is the total number of single stuck at faults, multiple stuck at faults and checkpoint faults in the circuit?
   b. Derive the equivalence collapsed set of faults. What is the collapse ratio after EFC?
   c. Derive the dominance collapsed set of faults. What is the collapse ratio after DFC?
   d. Use PODEM to determine the test pattern required to detect the J stuck-at-1 fault. Clearly mention the steps in the PODEM algorithm.
   e. Use concurrent fault simulation to determine all the stuck-at-faults that can be detected using the test pattern 1110.

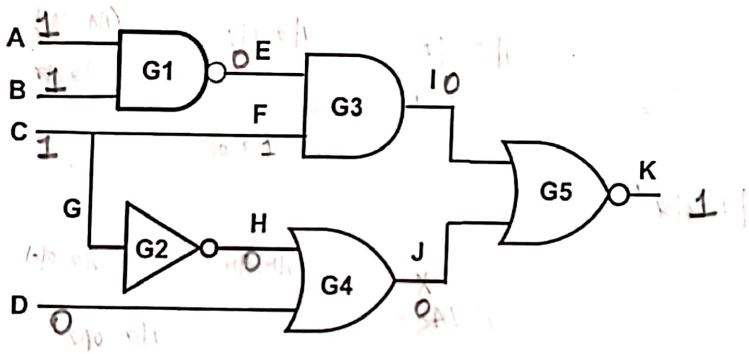

Figure 1

2. Memory Testing: [10+1+3+3+3=20 points]
   a. State the meaning of each of these memory faults and how you can test them: (i) transition faults, (ii) Address decoder fault, (iii) Passive neighborhood pattern sensitive fault, (iv) Stuck at fault, (v) State coupling fault.
   b. What is the best algorithm for detecting neighborhood pattern sensitive faults?
   c. The March C- algorithm can be written as {↕(w0); ↑(r0,w1); ↑(r1,w0) ; ↓ (r0,w1); ↓(r1,w0); ↕ (r0)}. How many march elements does this algorithm have? What is the time complexity? Which faults are detected by this algorithm?
   d. What is test compression and why do you need it?
   e. What are the features of a good test response compactor?

3. Logic BIST: [2+3+3+2+6+1=17 points]

a. Draw a standard LFSR for the characteristic polynomial x^3+x+1. Write the companion matrix for this LFSR.

b. Write out the test patterns generated by the LFSR for 7 clock cycles (treat the seed as the first clock cycle). Assume a seed value of 001 (1 being the least significant bit).

c. The test patterns generated by the LFSR are applied to the circuit shown in Figure 2 and used to detect the A stuck-at-1 fault. Write out the good and faulty responses of the circuit for the 7 test patterns from part (b) and determine the test patterns that can detect the A sa1 fault.

d. The test responses are compacted using an SISR formed using a modular LFSR with the characteristic polynomial x^3+x+1. Draw the SISR and write the companion matrix for the modular LFSR.

e. Determine the signature for the good and faulty responses from (c). Would the A sa1 fault be detected using this SISR?

f. What is the aliasing probability of the SISR?

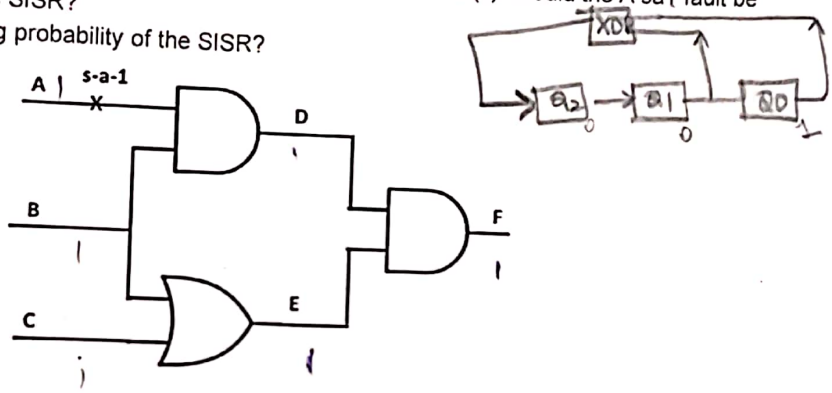

Figure 2

4. Delay Faults: [2+2+5+6=15 points]

a. Differentiate between the two types of delay fault models.

b. How many Path Delay Faults and Transition Delay Faults are in the circuit shown in Figure 3.

c. Generate a robust test for a rising transition at B through the path BEIM.

d. List all the transition delay faults that can be tested using the test vectors obtained in part (c).

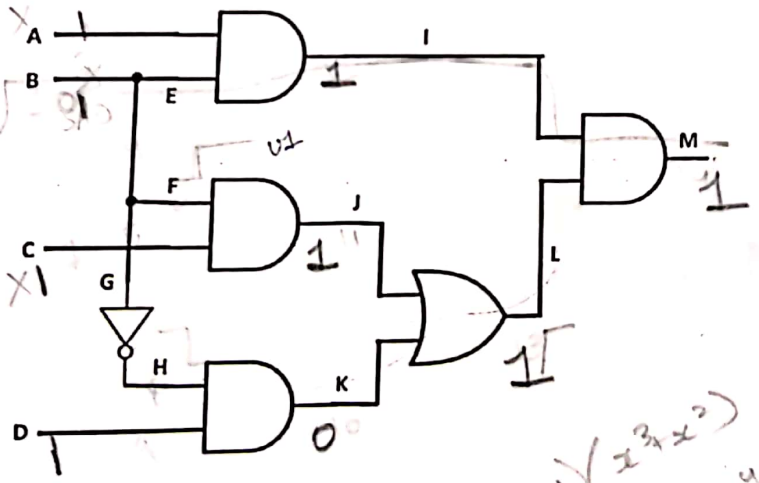

Figure 3

5. [5+2+2+4=13 points]

(a) Compute the combinational and sequential SCOAP testability measures (both controllability and observability) for the circuit in Figure 4. You can assume a synchronous clock and do not need to compute the observability of the clock signal.

(b) Redraw the circuit after scan-insertion using the Muxed-D architecture.

(c) Redraw the circuit for combinational ATPG using pseudo-primary inputs and outputs.

(d) Find a test pattern for detecting the e-s-a-0 fault. Also indicate the required scan-in/scan-out patterns for detecting the fault.

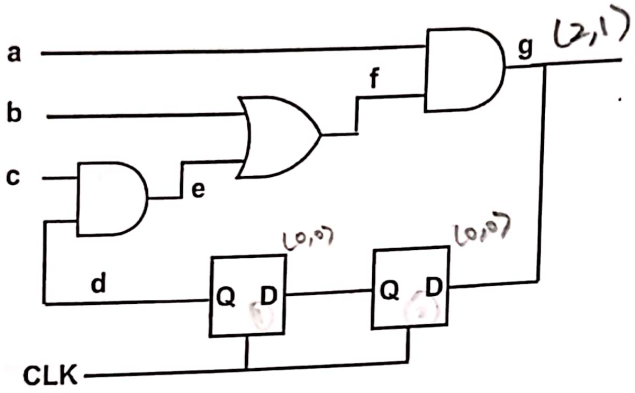

Figure 4

6. Boundary Scan Architecture: (info in page 4 to help answer this question) [5+5+5=15 points]

a. Consider testing the logic inside chip 2 while bypassing chip 1 (Figure 5). What is the TMS and TDI sequences you would use to load the instruction into the Instruction register? Explain why you are using that sequence. Assume that the INTEST instruction is a sequence of 1010 and the BYPASS instruction is a sequence of all ones. Also assume that chip1 has a 3 bit Instruction Register (IR) and chip2 has a 4 bit IR. Remember to initialize the TAPS controller before loading in the instruction.

b. Assume that the circuit in chip2 is that shown in Figure 2. You want to test the D stuck-at-0 fault. Explain how you would test this fault through the boundary scan architecture.

c. Write the TMS, TDI and TDO sequences needed for part (b)

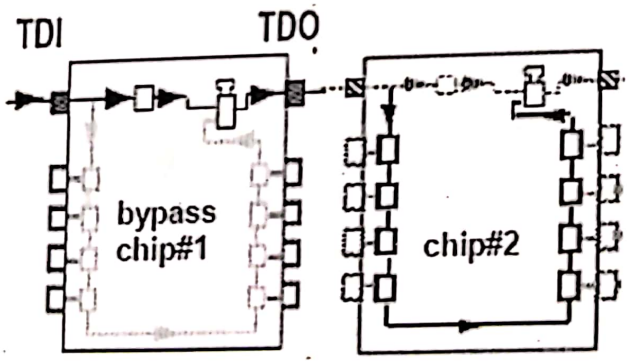

Figure 5