Scaled 2-Input CMOS Nand Gate using 28nm technology

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Abstract

Nowadays, we observe that a complementary-metal-oxide-semiconductor (CMOS) is widely used in large scale integrated circuits. In this paper, we aim to design a scaled 2-input CMOS NAND Gate on a 28 nm scale and analyze its output behavior along with the delay analysis for the same in comparison to a conventional 2-input CMOS NAND Gate. NAND gates are basic universal gates because with the help of these gates, we can create any digital circuit. Most of the CMOS Nand gate design techniques need either a p-logic block or an n-logic block for evaluation of input and output behavior at a transistor level.

1. Reference Circuit Details

Any basic CMOS design involves concatenation of a pMOS or an nMOS with a nMOS source being connected to GND directly or indirectly side by side with a pMOS source connected to the supply voltage (Vdd) directly or indirectly. Fig 1 shows the conventional circuit diagram of a NAND gate implemented using the pMOS and an nMOS. Fig 2 represents the reference circuit diagram for the 2 input Scaled Nand gate. Considering the truth table; Case:1) When p1.1=p1.2=p2=0, both the NMOS are in OFF condition and PMOS are in ON condition. Therefore, the output is connected to VDD 1.8v and 1.1v HIGH logic is present at the output terminal. Case:2) When p1.1=p1.2=0 and p2=1, the upper NMOS are in OFF and lower NMOS in ON condition. Left PMOS are in ON and right PMOS in OFF condition. Therefore, the output is connected to VDD and HIGH logic is present at the output terminal. Case:3) When p1.1=p1.2=1 and p2=0, upper NMOS are in ON and lower NMOS in OFF condition. Left PMOS are in OFF and right PMOS in ON condition. Therefore, the output is connected to VDD and HIGH logic is present at the output terminal. Case:4) When p1.1=p1.2=p2=1, both the NMOS are in ON condition and PMOS are in OFF condition. Therefore, the output is connected to VDD and LOW logic is present at the output terminal. With this we can observe that the output seen as in simulation, is in relation to the truth table of a NAND Gate, that is, a low output for both high inputs and vice versa.

2. Reference Circuit

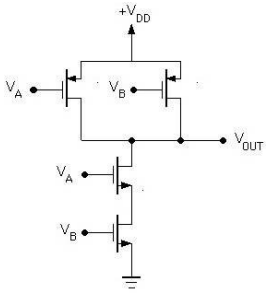

Fig. 1 Conventional CMOS NAND Gate

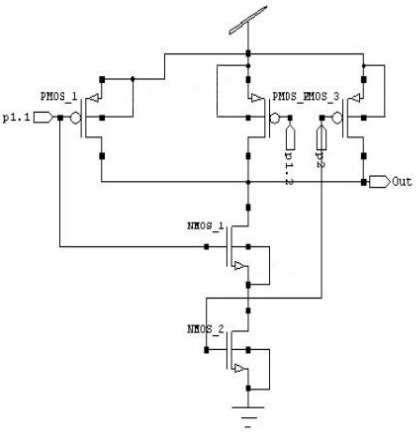

Fig. 2 Reference Circuit Diagram of Scaled 2-Input CMOS NAND Gate

3. Reference Circuit Waveform

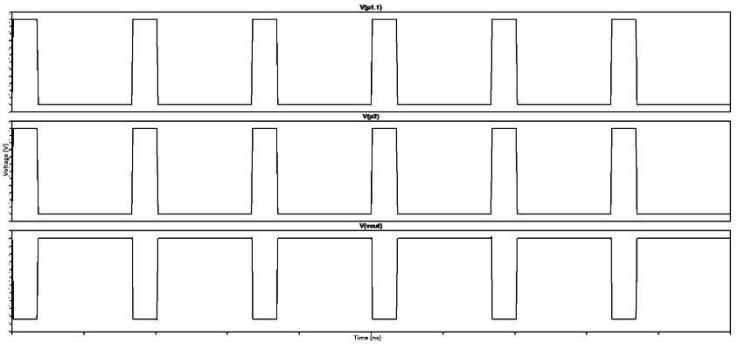

Figure 2: Reference waveform of Scaled CMOS NAND Gate

References

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