SDM COLLEGE OF ENGINEERING AND TECHNOLOGY,DHARWAD-580002

(An autonomous Institution affiliated to
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Department of Electronics and Communication Engineering

MAJOR PROJECT ON

STUDY AND ANALYSIS OF CMOS PERFORMANCE FACTORS

PROPOSED BY:

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Contents

Introduction

•**Study and Analysis of CMOS (Complementary Metal-Oxide-Semiconductor) performance factors** are crucial in understanding and enhancing the **efficiency** of modern **electronic devices**.

•Widely used in **integrated circuits (ICs)** due to its **low power consumption**, **high noise immunity**, and **scaling potential**.

•Essential for optimizing **performance** as device dimensions shrink and the demand for **higher speed** and **lower power** increases.

Motivation

- The motivation behind studying and analyzing CMOS performance factors stems from the **rapid advancements** and **evolving demands in modern electronics**.
- As technology progresses, the need for **highly efficient, low-power**, and **high-speed devices** has grown exponentially, particularly in fields such as **telecommunications, computing, and portable electronics.**

Literature survey

SI No.	Authors	Year Of Publication	Title	Techniques Employed
1.	Yuan Taur and Tak H. Ning	2022	Fundamentals of modern VLSI Devices	Scaling techniques
2.	Sarthak Talwara , B. Mohapatrab and Mohammad Rashid Ansari	2020	Performance Analysis of CMOS Technology	Reduction of Parasitic
3.	Zitong Han	2020	The power-delay product and its implication to CMOS Inverter	Gate sizing and transistor sizing
4.	Vikas Singhai, Saima Ayyub, Paresh Rawat	2016	Comparison of Leakage Power Reduction Techniques in 65nm Technologies	Leakage Power Reduction Techniques

Objectives

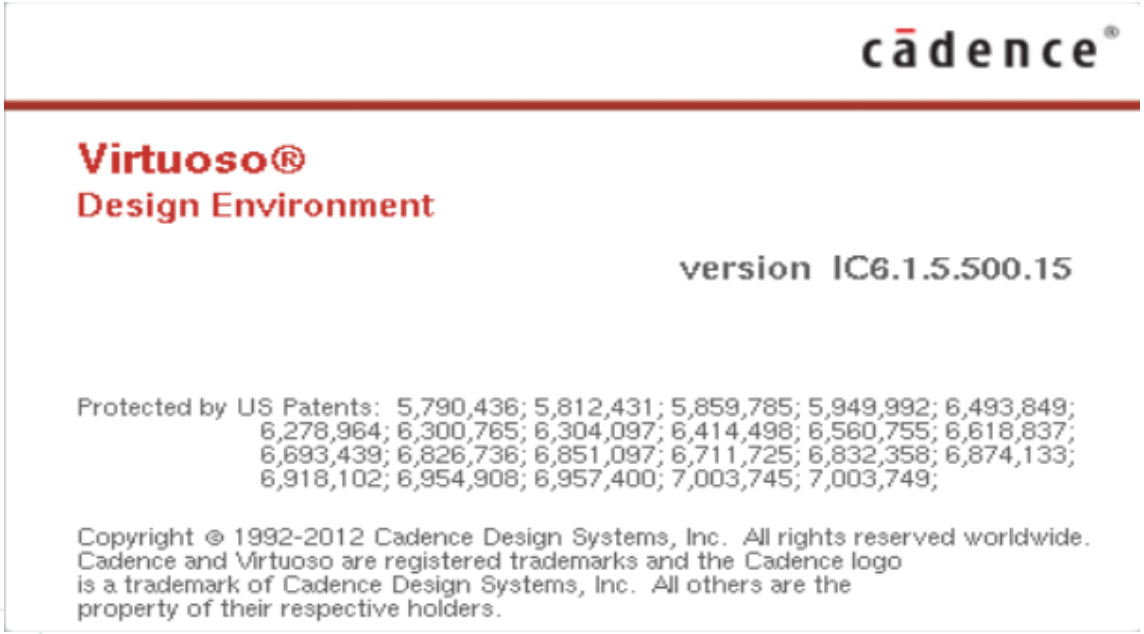
- To perform detailed literature survey on various CMOS performance factors.
- To investigate sensitivity of CMOS delay to device parameters.

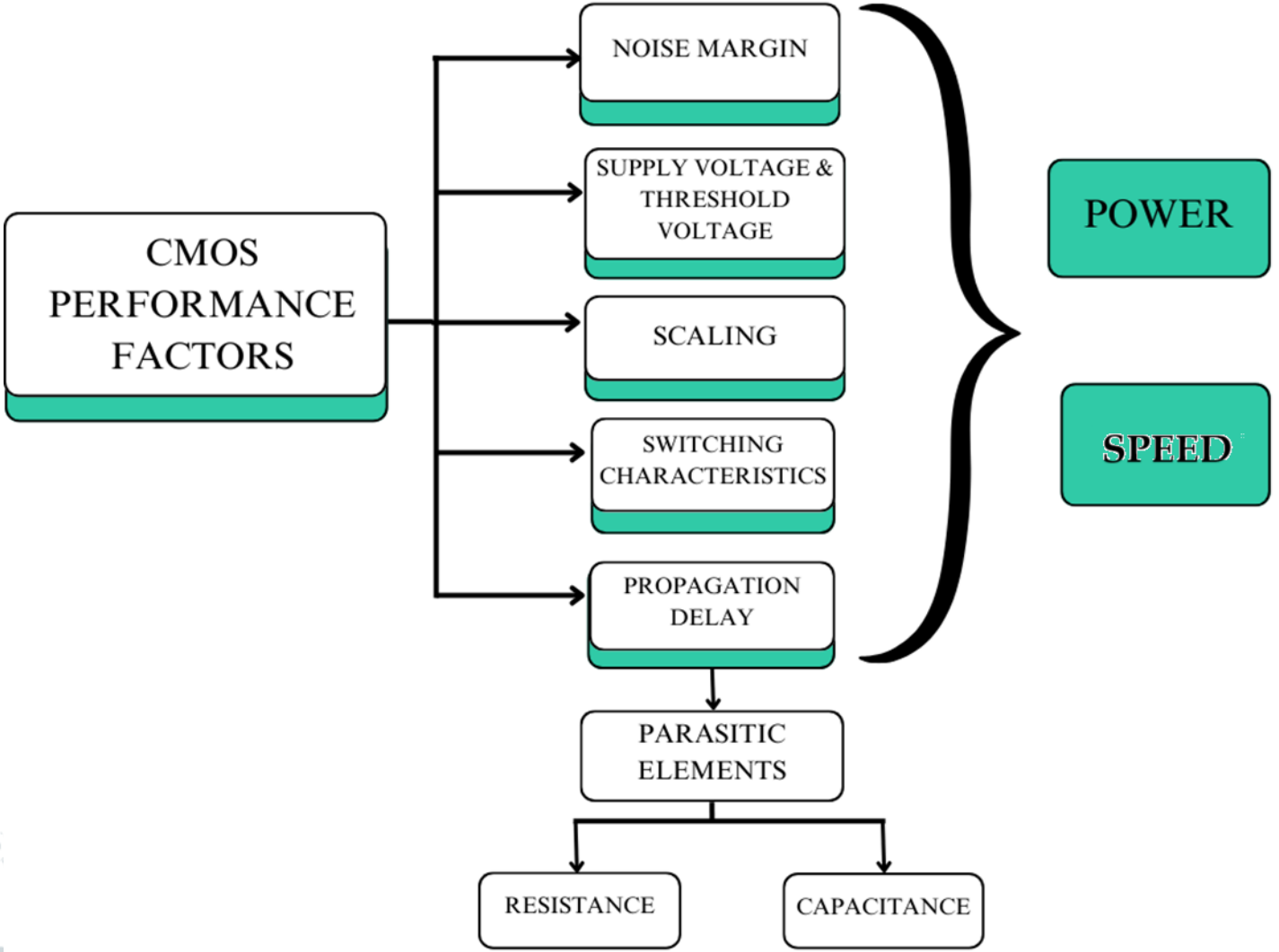
Problem statement

- To perform detailed study, analysis on various CMOS performance factors in VLSI technology.
- To perform performance related simulations using CADENCE virtuoso (90nm).

Technologies Used

- Cadence Virtuoso (Electronic Design Automation (EDA) tool suite)
  Technology node : 90 nm




CMOS PERFORMANCE FACTORS
NOISE MARGIN
SUPPLY VOLTAGE & THRESHOLD VOLTAGE
SCALING
SWITCHING CHARACTERISTICS
PROPAGATION DELAY
POWER
SPEED
PARASITIC ELEMENTS
RESISTANCE
CAPACITANCE

Preliminary Study Done

- **Noise Margin**

Noise margin is the tolerance level for unwanted voltage (noise) that can be present on an input signal without causing errors in the output.

Impact on Power

- Reduced noise margin: Decreased power consumption.

- Increased noise margin: Increased power consumption.

Impact on Delay

- Reduced noise margin: Decreased delay.

- Increased noise margin: Increased delay.

Preliminary Study Done

- **Switching Characteristics**

Switching characteristics in CMOS refers to behaviour of the signal when they change their states from 0 to 1 and 1 to 0 .

Impact on Power

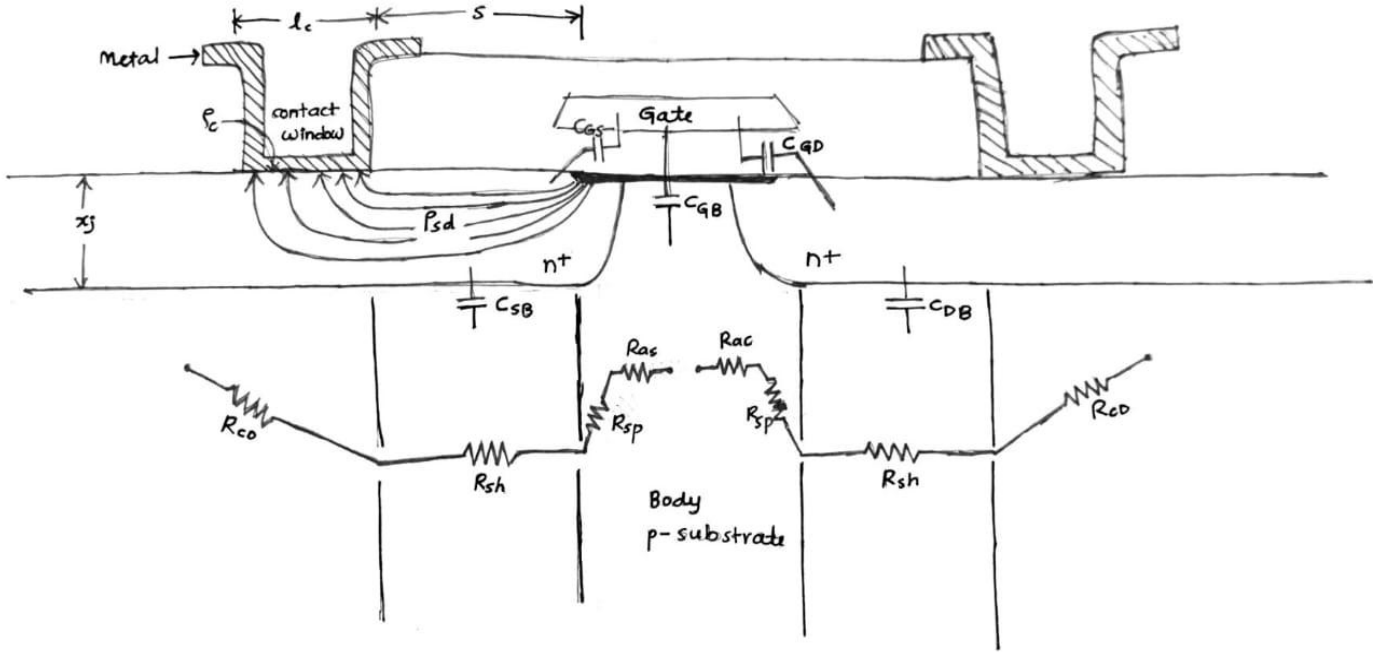
- Increased switching activity – increases power consumption

Impact on Delay

- Longer transition times (increased switching activity) increases the delay

Preliminary Study Done

- **Parasitic Elements (resistance, capacitance)**



Preliminary Study Done

- **Propagation delay of CMOS inverter**

Propagation delay refers to the time taken by the signal to reach from input to output.

Impact on Power

- Increased propagation delay leads to lower power consumption.

Impact on Delay

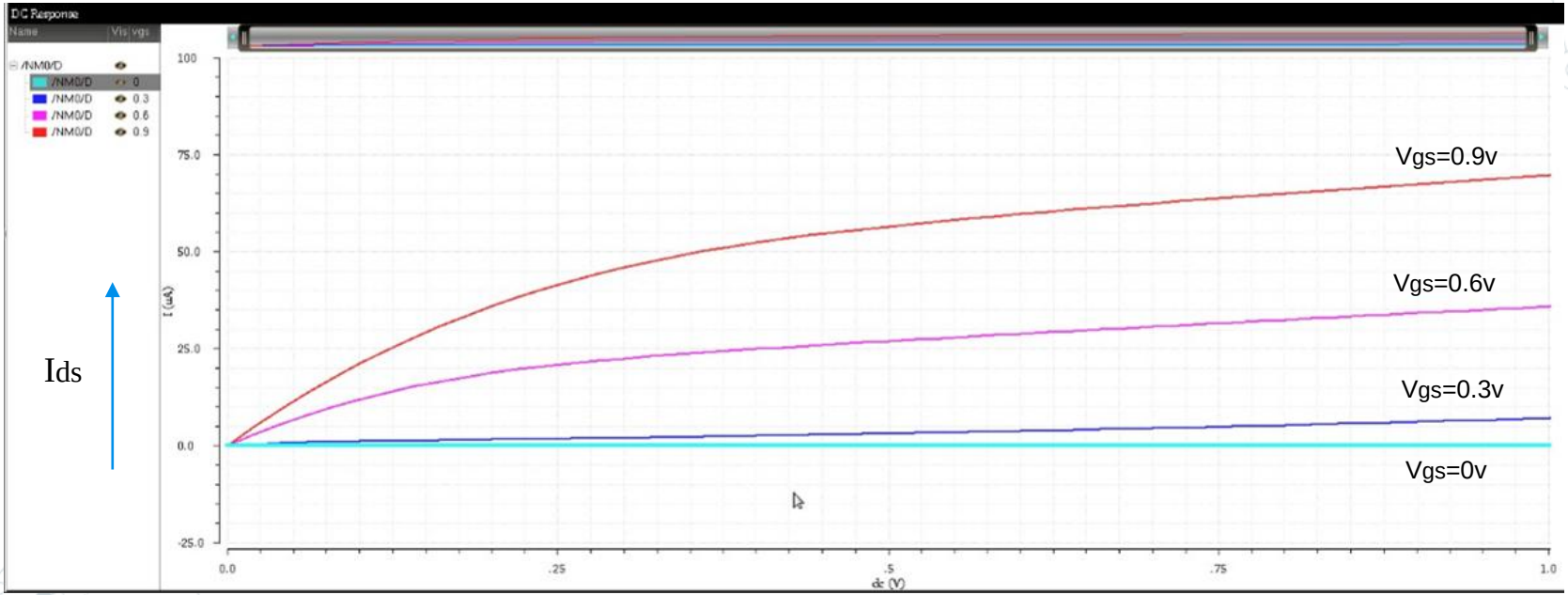
- Increased propagation delay leads to longer signal path delays and takes more time to reach output.

Preliminary Results

CMOS LOGIC CIRCUITS	POWER	DELAY
INVERTER	46nW	16.33ps
NAND	40.35nW	26.71ps
NOR	52.7nW	31.718ps

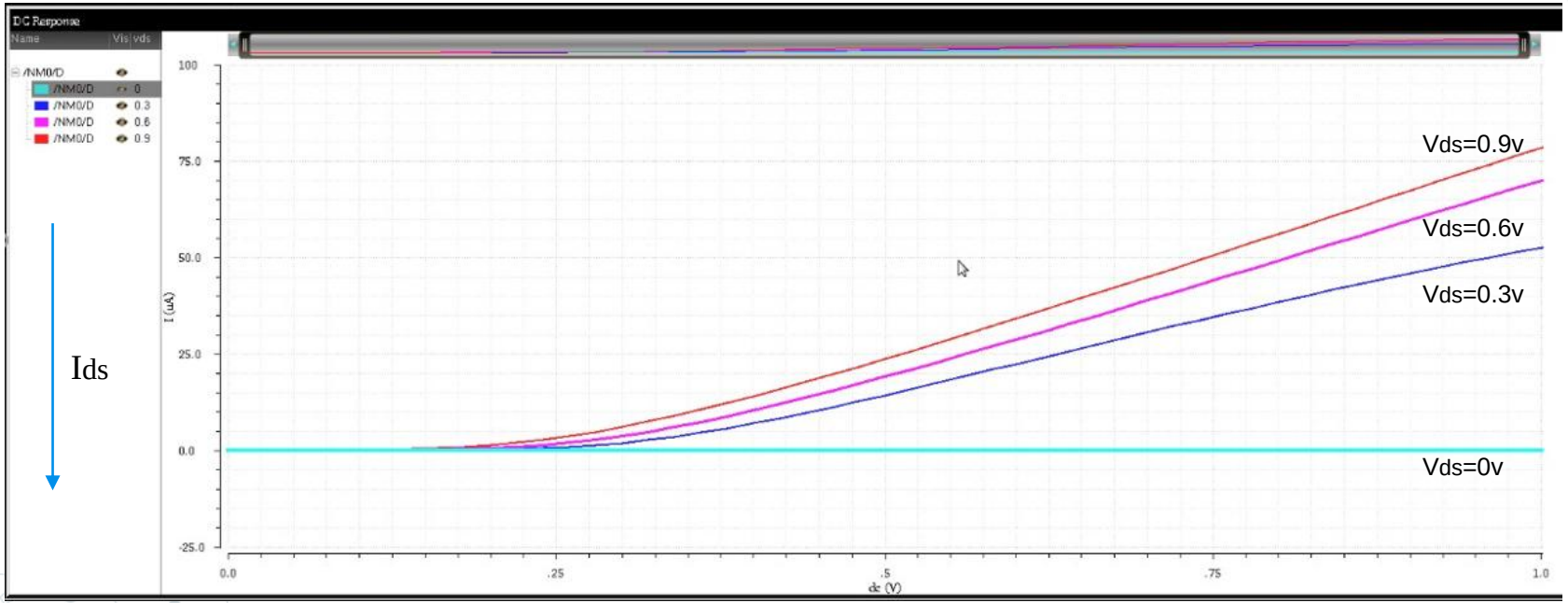
Preliminary Results

NMOS – Vds vs Ids



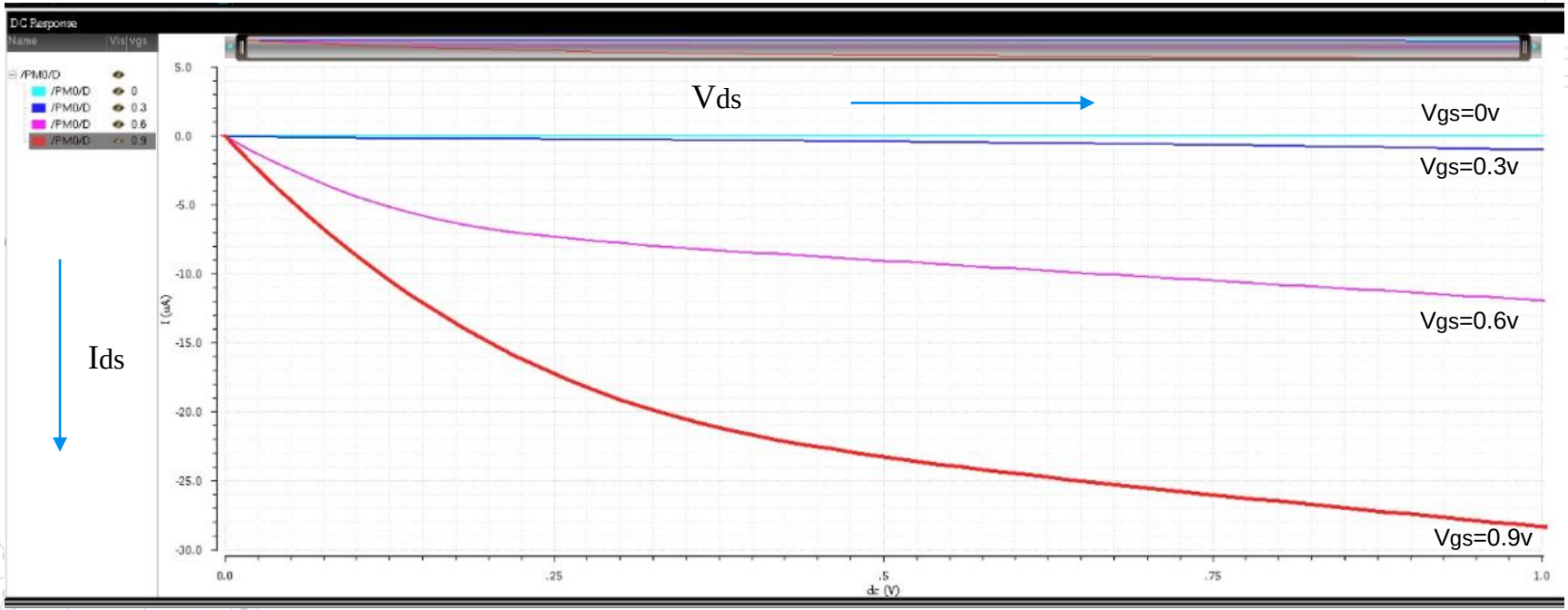
Preliminary Results

NMOS – Vgs vs Ids



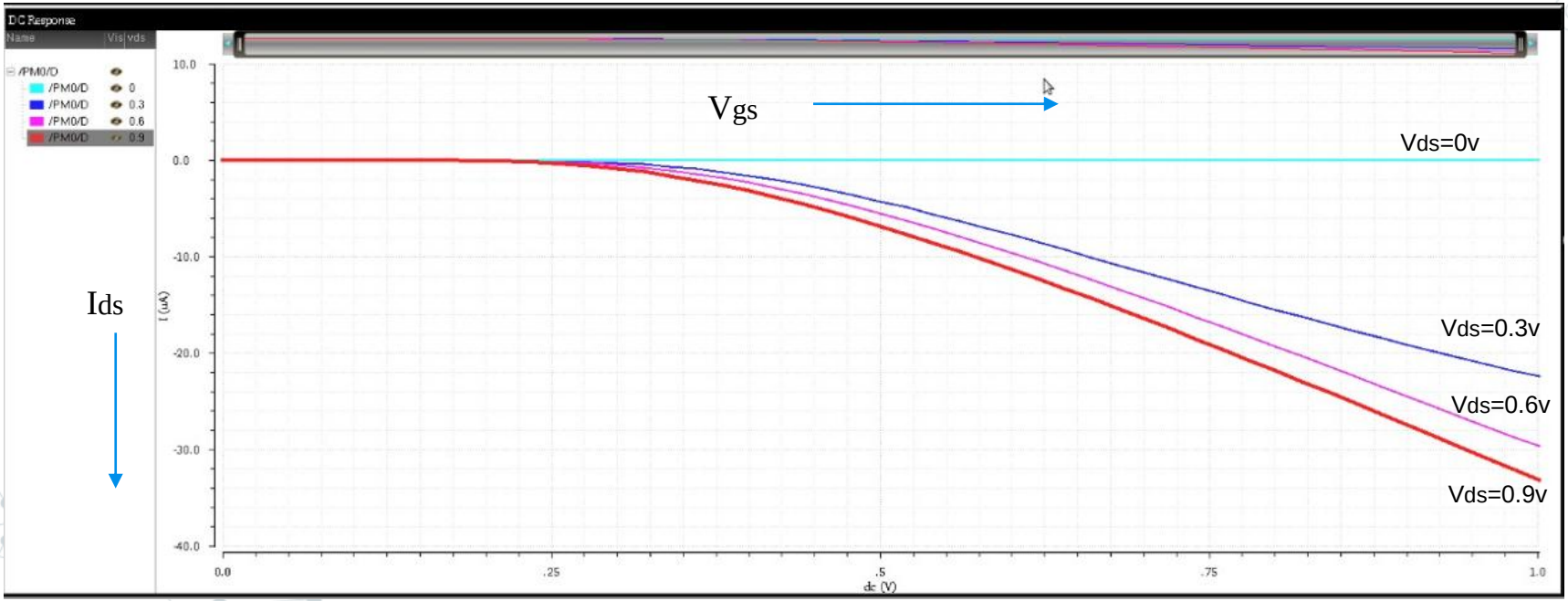
Preliminary Results

PMOS – Vds vs Ids



Preliminary Results

PMOS – Vgs vs Ids

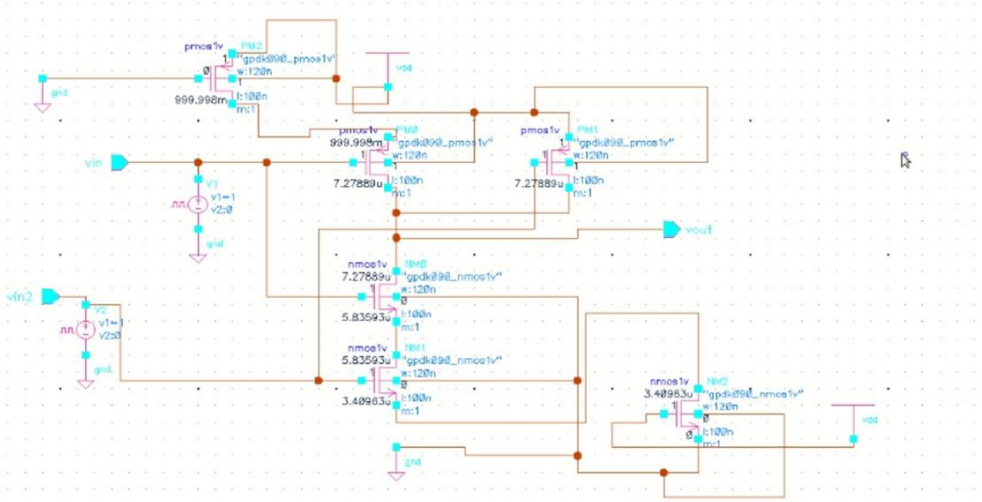


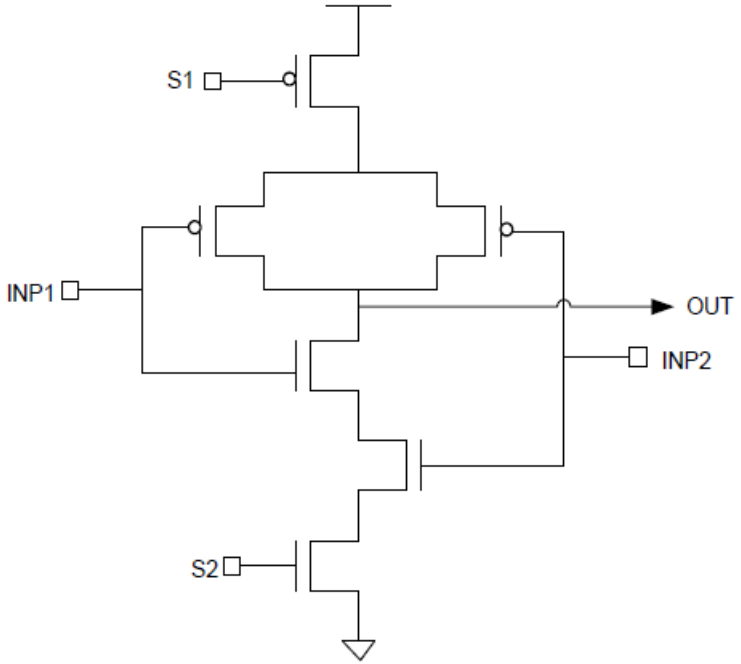
Leakage Power Reduction

- Leakage power consumption is the power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor.
- Short circuit power consumption occurs during switching of both NMOS and PMOS transistors in the circuit and they conduct simultaneously for a short amount of time.

Leakage Power Reduction

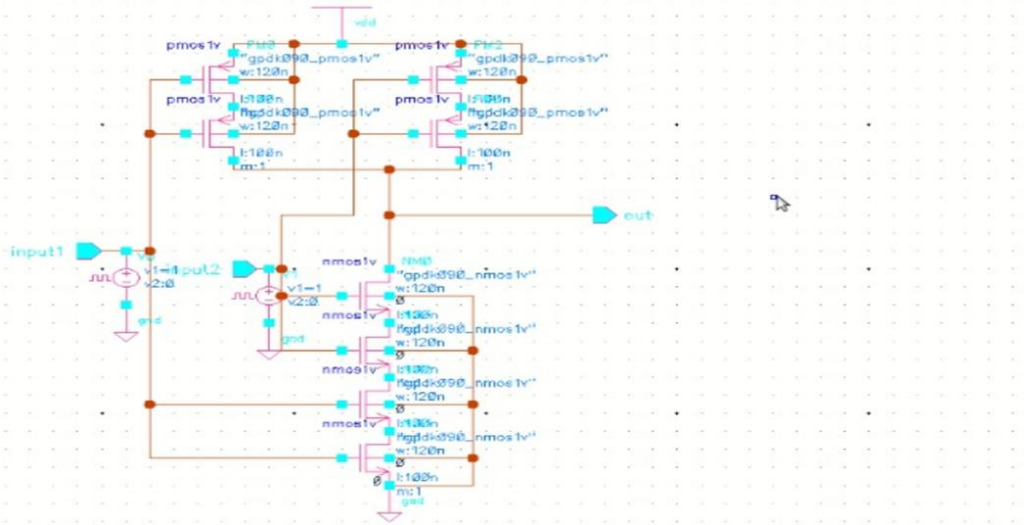
Sleep Approach NAND gate – 26.55 nw

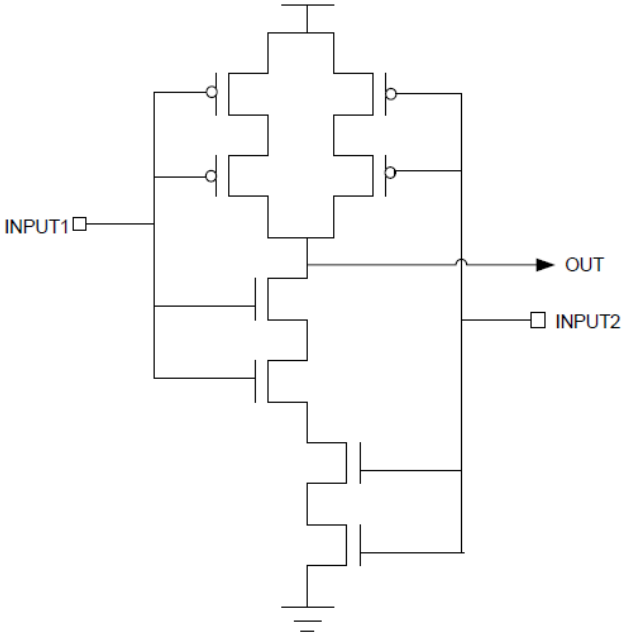




Leakage Power Reduction

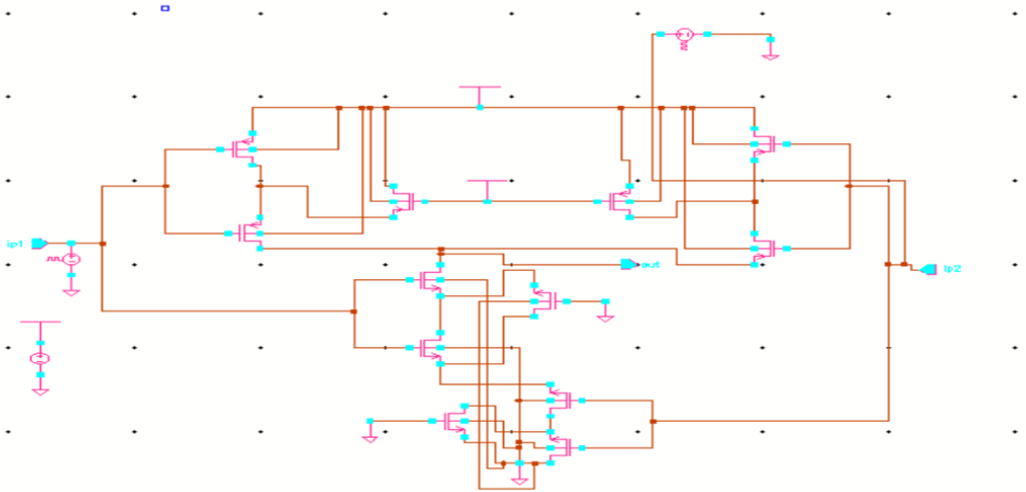
Stack Approach based 2 input NAND gate – 19.47 nw

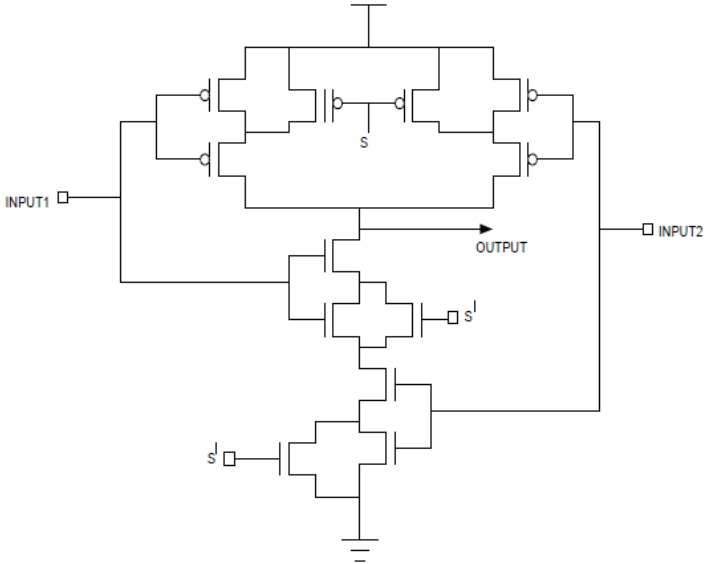




Leakage Power Reduction

Sleepy Stack Approach based 2 input NAND gate – 24.62 nw





Leakage Power Reduction

90 nm	Power (nW)
Sleep Approach NAND gate	26.55 nW
Stack Approach based 2 input NAND gate	19.47 nW
Sleepy Stack Approach based 2 input NAND gate	24.62 nW

Sensitivity of CMOS delay to device parameters

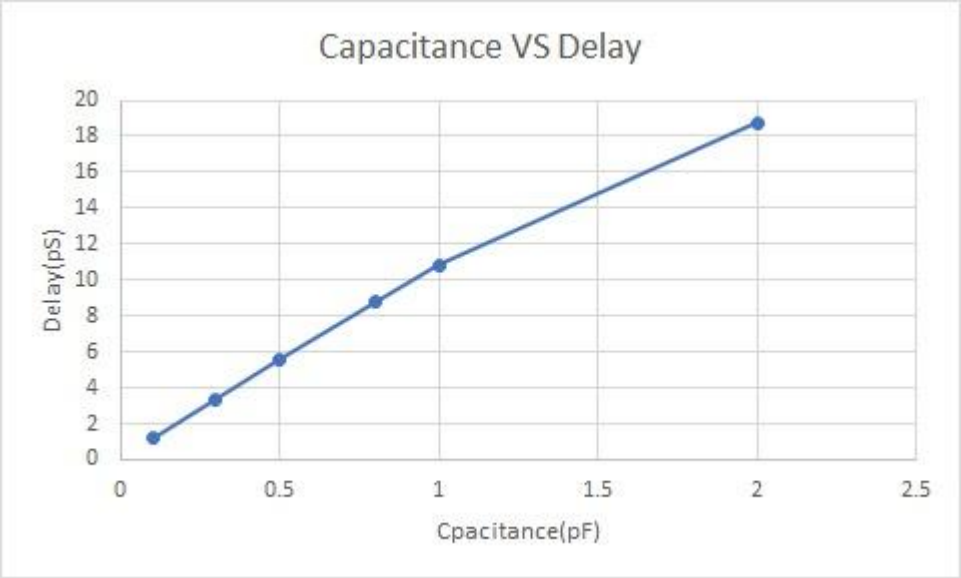
Key Factors affecting device parameters :

1) **Capacitance**

The total delay of a circuit is influenced by the time it takes to charge or discharge the load capacitance (CL) through the driving transistor. The delay can be separated into **rise time** (charging) and fall time (discharging).

Capacitance	0.1pF	0.3pF	0.5pF	0.8pF	1pF	2pF
Delay	1.182ns	3.378ns	5.568ns	8.77ns	10.838ns	18.75ns

Sensitivity of CMOS delay to device parameters



CONCLUSION : An increase in load capacitance increases the delay in a CMOS inverter, as it takes more time to charge and discharge the capacitance. Larger load capacitance results in slower switching and higher propagation delay.

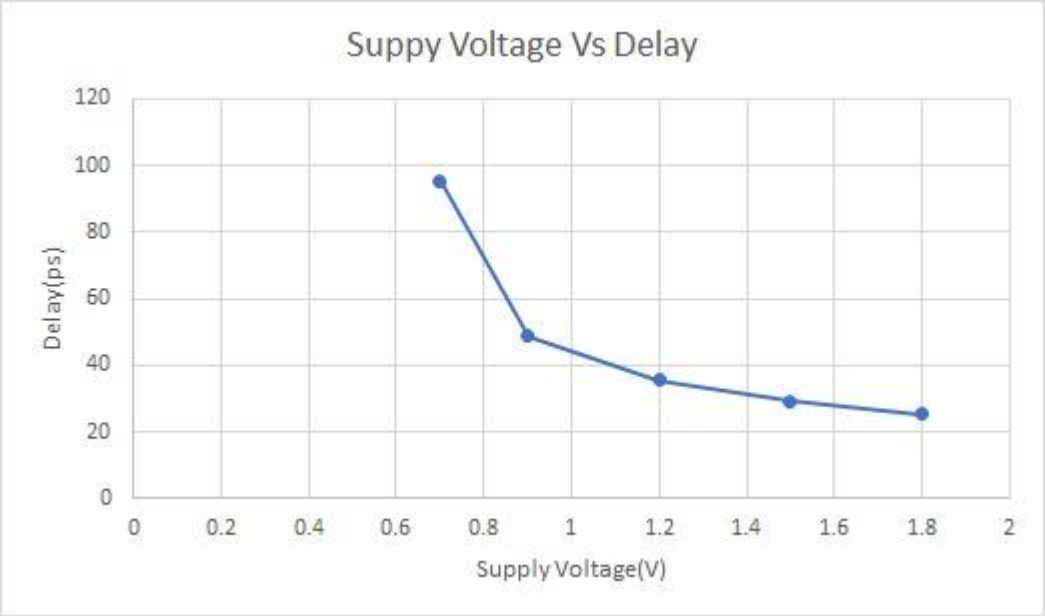
Sensitivity of CMOS delay to device parameters

2) **Power Supply Voltage**

The power supply voltage is the external voltage provided to a circuit or device to power its operation.

Power Supply Voltage	0.45V	0.7V	0.9V	1.2V	1.5V	1.8V
Delay	25.17ns	0.0953ns	0.0488ns	0.0356ns	0.0292ns	0.025ns

Sensitivity of CMOS delay to device parameters



CONCLUSION: An increase in delay occurs when the supply voltage (VDD) is reduced, as the transistors switch slower, resulting in longer rise and fall times. This increases the overall propagation delay of the CMOS inverter.

Sensitivity of CMOS delay to device parameters

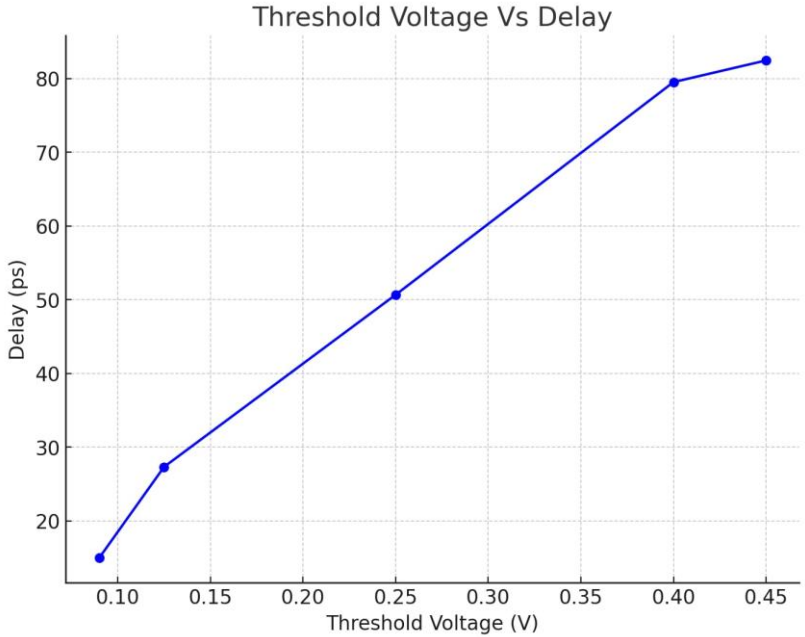
3) **Threshold Voltage**

The **threshold voltage (VT)** is the minimum voltage required at the gate of a transistor (e.g., MOSFET) to create a conducting path between the source and drain terminals. Beyond this voltage, the transistor switches from the OFF state to the ON state.

Threshold Voltage	0.45V	0.40V	0.25V	0.125V	0.09V
Delay	82.46ps	79.52ps	50.67ps	27.33ps	14.99ps

$$t_{pd} = (C_L V_{dd})/ I_{ds}$$

Sensitivity of CMOS delay to device parameters



CONCLUSION : A decrease in threshold voltage lowers the required voltage for the transistor to turn on, increases the current that can flow through it, and reduces the time needed to charge discharge the capacitances associated with switching. As a result, delay decreases.

Sensitivity of CMOS delay to device parameters

4) **Channel Width**

The channel width refers to the width of the conductive channel in a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) that connects the source and drain terminals. This channel allows the flow of charge carriers (electrons or holes) when the transistor is turned on.

a) Width of pmos =120nm (fixed)

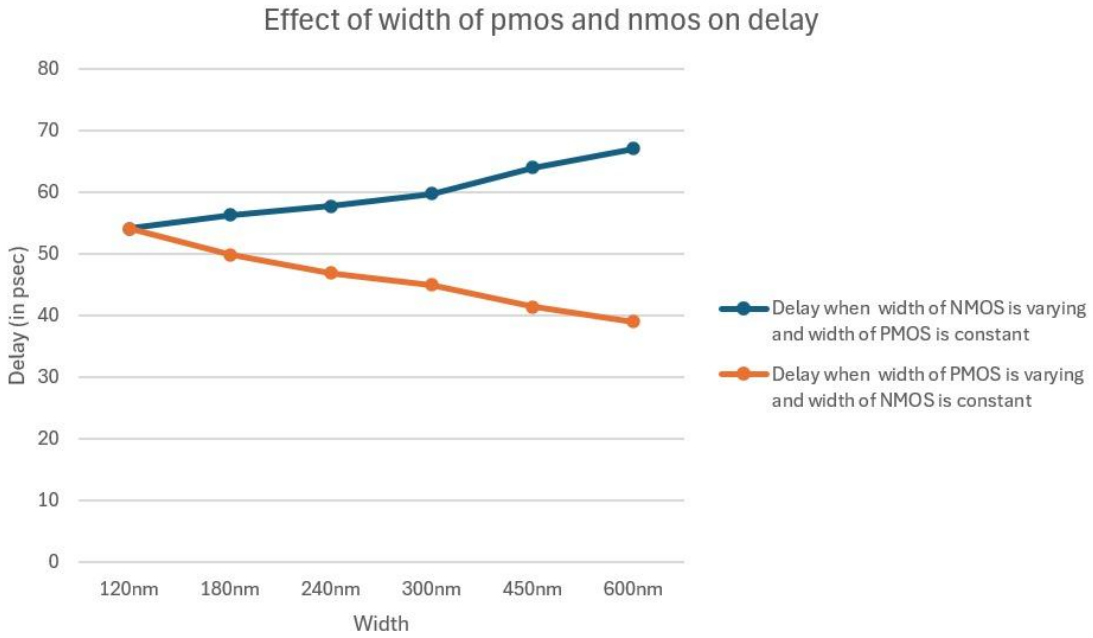
Width of nmos	120nm	180nm	240nm	300nm	450nm	600nm
Delay	54.01ps	56.24ps	57.73ps	59.74ps	63.98ps	67.045ps

Sensitivity of CMOS delay to device parameters

b) Width of nmos =120nm (fixed)

Width of pmos	120nm	180nm	240nm	300nm	450nm	600nm
Delay	54.01ps	49.8ps	46.84ps	44.905ps	41.345ps	38.955ps

Sensitivity of CMOS delay to device parameters



CONCLUSION : Increasing NMOS width increases delay due to secondary effects like leakage current, short-channel effects, or insufficient improvement in current drive . Increasing PMOS width decreases delay as it compensates for the PMOS's lower mobility, improving current drive and speeding up switching.

Sensitivity of CMOS delay to device parameters

5) **Channel length**

The channel length (L) in a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) refers to the distance between the source and drain terminals, where the current flows through the channel created in the semiconductor material between these two terminals.

a) Length of pmos =100nm (fixed)

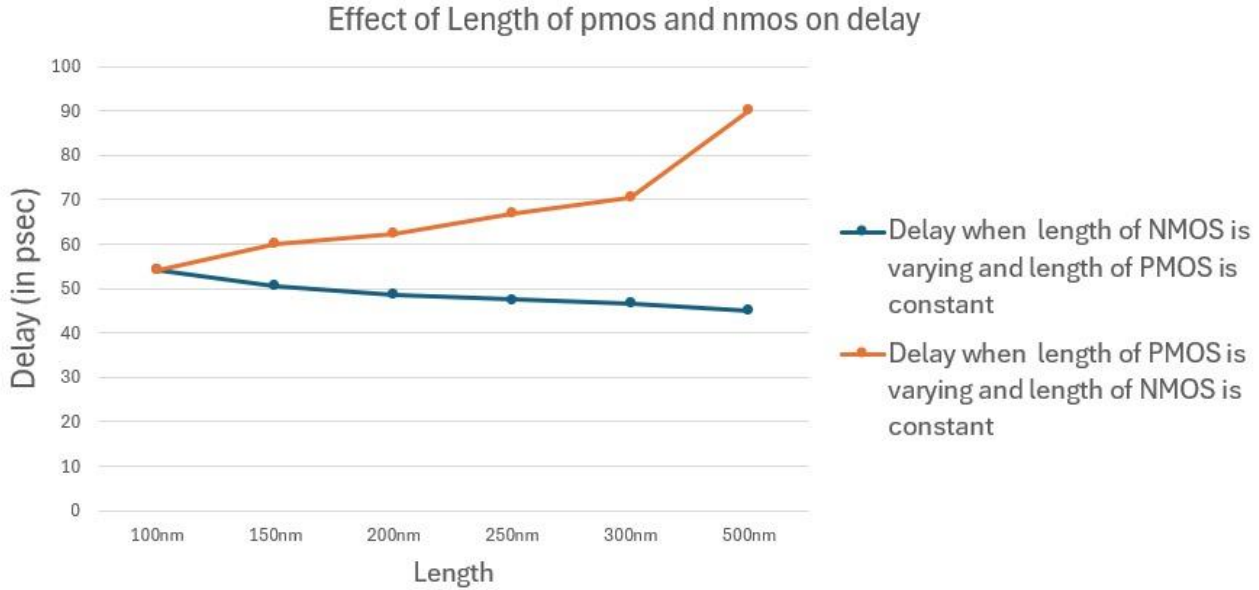
Length of nmos	100nm	150nm	200nm	250nm	300nm	500nm
Delay	54.01ps	50.62ps	48.62ps	47.4ps	46.53ps	44.92ps

Sensitivity of CMOS delay to device parameters

b) Length of nmos =100nm (fixed)

Length of pmos	100nm	150nm	200nm	250nm	300nm	500nm
Delay	54.015ps	59.925ps	62.345ps	66.69ps	70.47ps	90.195ps

Sensitivity of CMOS delay to device parameters



CONCLUSION: the lower mobility of holes in PMOS transistors explains why delay increases significantly as the PMOS length increases, while NMOS devices exhibit a relatively stable delay.

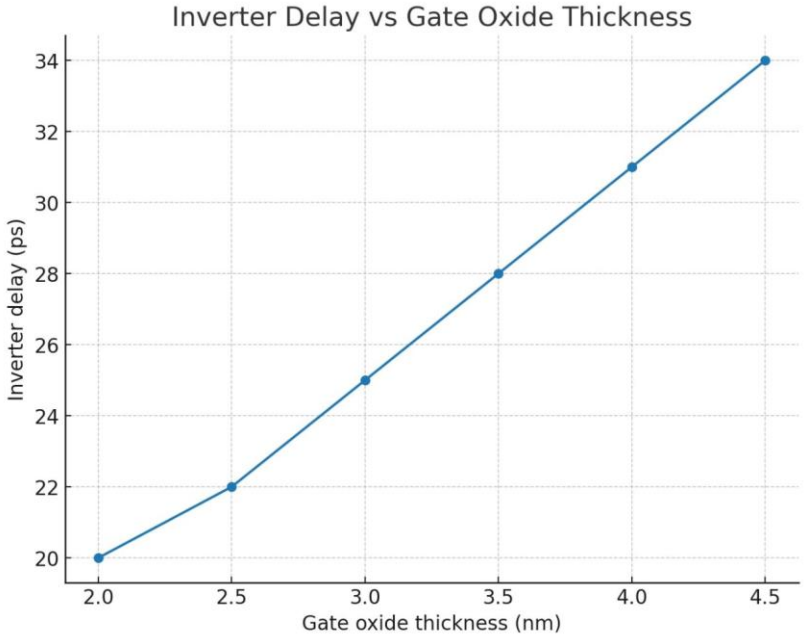
Sensitivity of CMOS delay to device parameters

6) **Gate oxide Thickness**

Gate oxide thickness refers to the thickness of the insulating layer of oxide that separates the gate electrode from the semiconductor channel in a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). This layer plays a critical role in the performance of the transistor, as it controls the flow of current between the source and drain terminals by influencing the gate's ability to control the channel.

Gate oxide	2.0nm	2.5nm	3.0nm	3.5nm	4.0nm	4.5nm
Delay	20.34ps	22.89ps	25.54ps	28.23ps	31.83ps	34.61ps

Sensitivity of CMOS delay to device parameters



CONCLUSION : Thinner oxide leads to a higher gate capacitance. Higher gate capacitance increases the charging/discharging time, resulting in greater propagation delay, reducing overall circuit speed and performance.

Conclusion

- The objectives of performing a detailed analysis of CMOS performance factors and investigating delay sensitivity using simulations in Cadence Virtuoso have been successfully met.

Future Work

- Sensitivity of delay parameter with respect to NAND and NOR gates.
- In similar manner as delay, analyzing the sensitivity of CMOS performance factors to power.

References

[1]Taur, Y., & Ning, T. H. (2023). Fundamentals of modern VLSI devices (3rd ed.). Cambridge University Press.

[2] Talwar, S., Mohapatra, B., & Ansari, M. R. (2020, May 23). Performance Analysis of CMOS Technology. 2nd International Conference on Communication & Information Processing (ICCIP) 2020. SSRN. https://papers.ssrn.com/sol3/papers.cfm?abstract_id=3647984

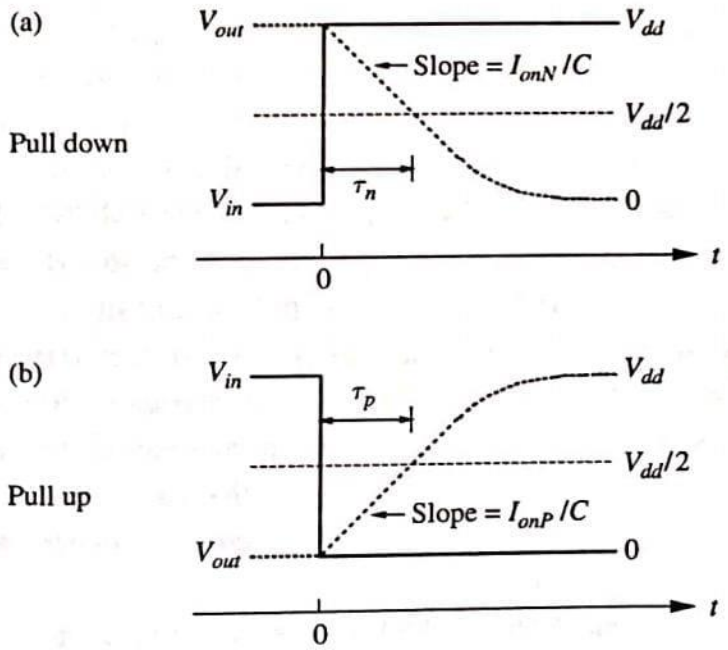
[3] Zitong Han 2021. The power-delay product and its implication to CMOS Inverter. J. Phys.: Conf. Ser. 1754 012131 https://iopscience.iop.org/article/10.1088/1742-6596/1754/1/012131/pdf

[4]International Journal of Computer Applications (0975 – 8887) Volume 134 – No.8, January 2016 28 Comparison of Leakage Power Reduction Techniques in 65nm Technologies

THANK YOU

Additional Study Done

- **Switching Characteristics**



Waveforms of the output node voltage (dotted) of a CMOS inverter. (a) Pull-down transition after an abrupt rise of input voltage (solid). (b) Pull-up transition after an abrupt fall of input voltage (solid).

1. **Overview of CMOS Inverter Switching**: Describes the basic switching characteristics of a CMOS inverter, especially when the gate voltage undergoes an abrupt or infinitely sharp transition.

2. **Switching Transition**

Example: In an inverter, when Vin transitions from 0 to Vdd
Before the transition, the nMOSFET is off, and the pMOSFET is on.
After the transition, the nMOSFET is on, and the pMOSFET is off.

3. **Pull-Down Switching Characteristics**: The switching behaviour is defined by the differential equation:
(C_+C+)dVout/dt=−IN(Vin=Vdd)

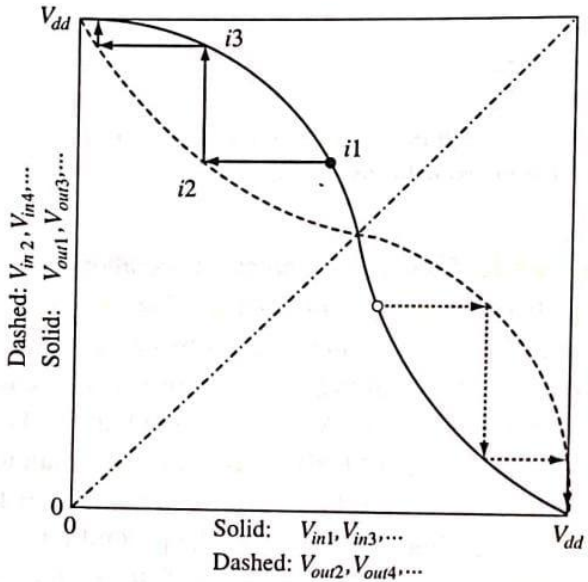
4. **Definition of nMOSFET Pull-Down Delay (τn)**:Defined as the time it takes for the output node voltage to reach Vdd/2.

5. **Definition of pMOSFET Pull-Up Delay (τp)**:Defined as the time for the output voltage to rise.

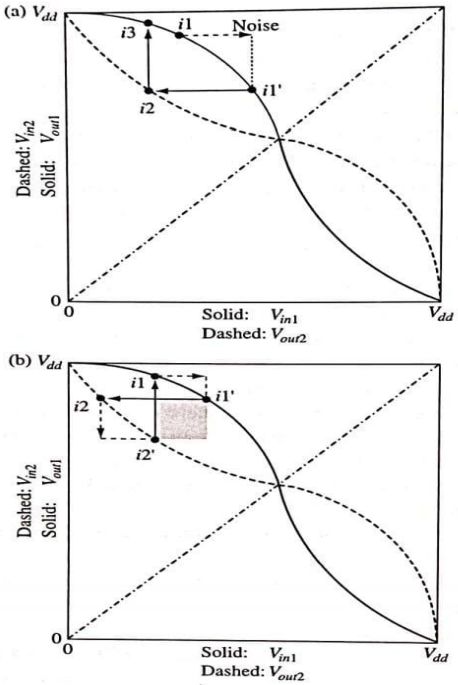
Additional Study Done

- **Noise Margin**

Noise margin is the tolerance level for unwanted voltage (noise) that can be present on an input signal without causing errors in the output.

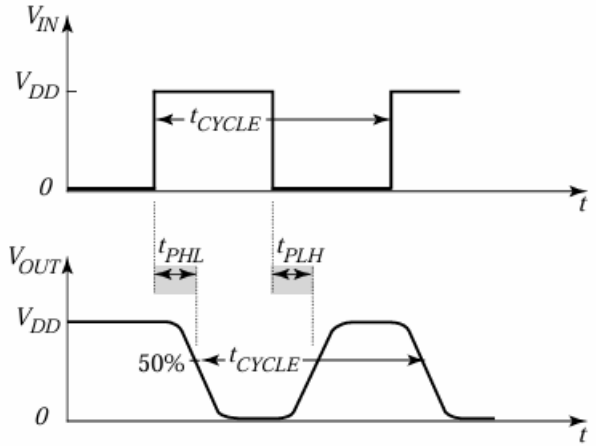


Noise margin for a given transfer curve is measured by the size of the maximum square that can fit between itself and its complementary curve.



Additional Study Done

- **Propagation delay of CMOS inverter**



Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed. Typical propagation delays: < 100 ps.

Average propagation delay: tp = $(T_{PHL}+T_{LHP})/2$.

Where, T_{PHL}= propagation delay high to low

and T_{PLH}= propagation delay low to high

Propagation delay and Power tradeoff:

V_{DD} increases⇒ tp decreases

– **Reason:** V_{DD} increases as a result, the overdrive voltage V_{GS}-V_{TH} is also increased which increases the current I_D

– **Trade-off:** VDD ↑⇒more power consumed.

Additional Study Done

- **Parasitic Elements**

Parasitic elements in CMOS (Complementary Metal-Oxide-Semiconductor) circuits refer to unintended components, such as capacitances, resistances, and sometimes inductances, that arise from the physical layout and materials used in semiconductor devices. These elements can affect the performance, power consumption, and reliability of CMOS circuits, especially as devices are scaled down in size. Common parasitic elements in CMOS **:**

1) Source-Drain Resistance

2) Gate Resistance

3) Junction Capacitance

4) Overlap Capacitance

5) Interconnect R and C