FINAL PROJECT – Operational Amplifier Design

EL-GY 6403

Fundamentals of Analogue CMOS Design

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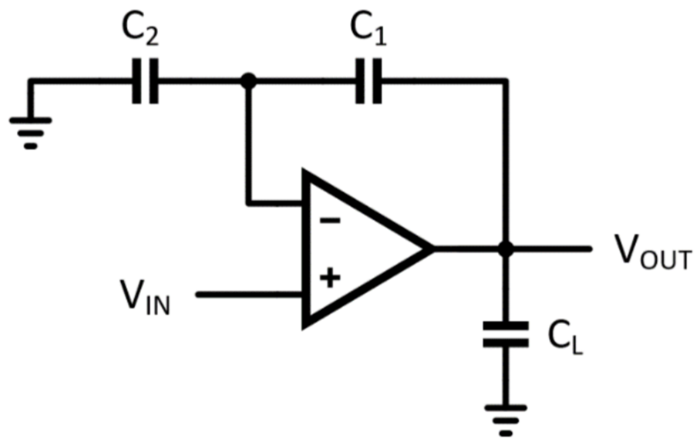
Operational Amplifier :



Specifications :

w(-3dB) = 2*pi* 15 * 10^6 rad/s
Slew Rate = 30 V/ µs
Phase Margin ≥ 70◦
All Capacitances = 2pF (C1, C2, CL)

Different Methods to design Op-Amp:

Several methods currently exist to design the operational amplifier. Some of the methods we considered are mentioned below:

1) Folded cascode:

Although the folded cascode provides high gain, high input impedence, high stability, high slew rate and good bandwidth, it has a limited Vcm. The problem arises with the number of transistors required for designing, hence increasing the over all number of poles (poles at folding node) and higher power consumption.

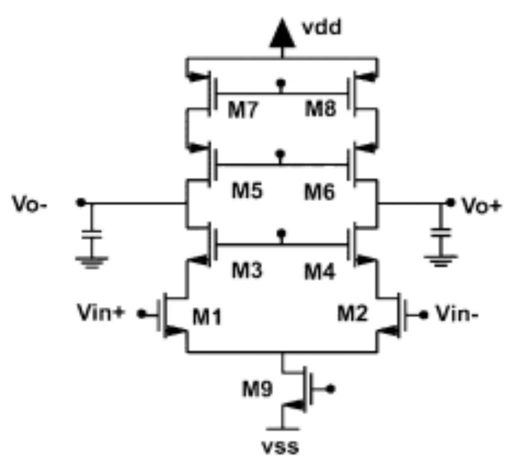


Fig 1. Folded Cascode Operational Amplifier [1]

2) Telescopic :

Although the tradeoff between gain, power dissipation, speed, noise and frequency capability is good for these circuits, the output swing is limited and shorting input and output is difficult.

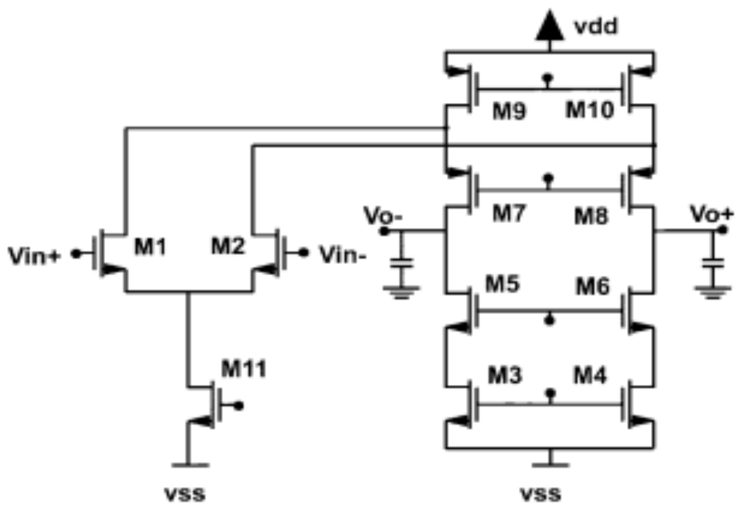


Fig 2. Telescopic Operational Amplifier [1]

3) Two Stage OTA

The two stage OTA provides us with a large gain, more swing and good bandwidth, although the power consumption is high.

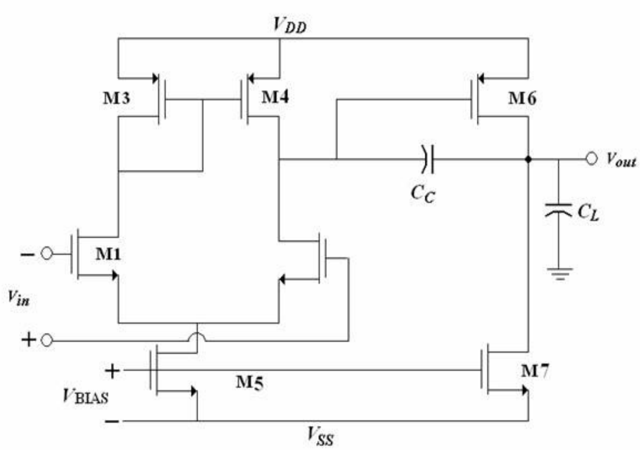


Fig 3. Two Stage OTA

Several variations and modifications have been performed over these models to obtain more efficient, constraint abiding operational amplifiers. Some examples are mentioned below.

Existing Solutions :

1) Gain enhanced differential amplifier using positive feedback [2]:

The cross-coupled MOSFETs provide the positive feedback to the output nodes with a negative transconductance. This reduces the positive output resistance of both PMOS and NMOS loads of diff-pair circuit. Hence, the cross-coupled MOSFET increases the amplifier gain.

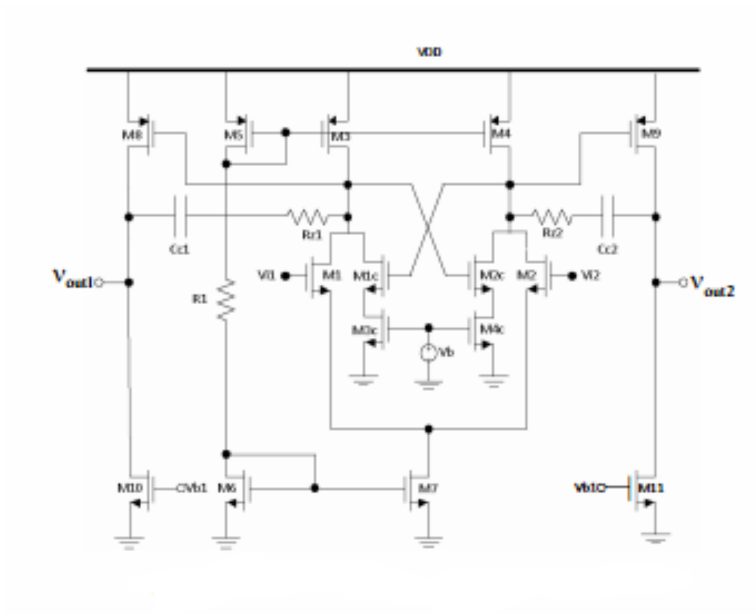


Fig 4. Gain enhanced diff amplifier with positive feedback connected to common source stage [2].

Modifying the differential amplifier by adding positive feedback in stage 1 has the following effects [2]:

Circuit characteristics	Standard CMOS diff-pair	Known Published Diff-amp with positive feedback
Supply voltage	1.0 V	1.0 V
Power dissipation	17.6 μW	17.4 μW
DC gain	30dB	50.8dB
Phase margin	108°	107°
Unity gain freq.	23.3GHz	20.7GHz
Noise (at 10K)	14 μV /Hz$^{1/2}$	92 μV /Hz$^{1/2}$

Table (1).

2) A Folded Cascode Op-Amp with Dynamic Switching Bias Circuit [3]:

A folded-cascode OP Amp with a dynamic switching bias circuit enables low power consumption, a relatively wide dynamic range and high gain in low power supply voltage. Through simulations, it was shown that the OP Amp is able to operate at a 10 MHz dynamic switching rate and a dissipated power of 71 % of that observed in continuous operation. Also, the open loop gain and output dynamic range was found to be wider than that of a telescopic Operational Amplifier. The output inaccuracy for a switched capacitor amplifier with a gain of below 2 is below 1.5 %, which is practicable. This inaccuracy was caused by the static nonlinearity of the OP Amp, determined on its limited open loop gain [3].

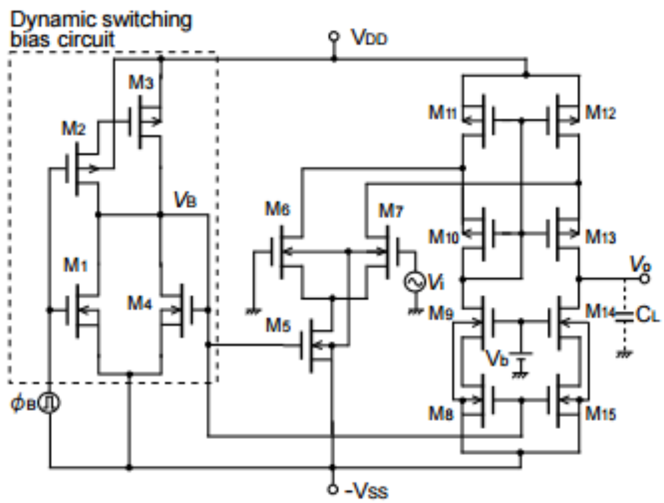


Fig 5. Folded Cascode with Dynamic Bias Circuit Switch [3]

3) A novel feed-forward compensation technique for single-stage fully-differential CMOS folded cascode rail-to-rail amplifier [4]

The rail-to-rail amplification has a passive and active mixed feedforward compensation technique. The compensated OTA provided over 60 dB DC-gain with rail-to-rail output voltage swing as well as wide input common-mode range. This ensures optimum step response (fast and accurate settling without ringing) for the feedback amplifier in switched-capacitor signal processing applications. More about this method can be read from [4]

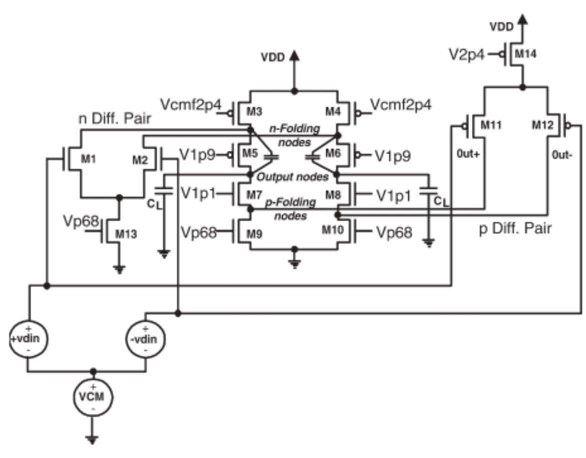


Fig 6. Rail-to-Rail OTA structure

Why Two Stage OTA :

We are using Two Stage Operational Transconductance Amplifier, as it has several advantages over folded cascode which are :

- Large Gain
- Improved Bandwidth
- Improved Swing

Architecture :

OTA consist of two stages, first stage is differential amplifier and second stage is common source amplifier. We have considered the second stage to be a PMOS common-source with a NMOS current load. The reason we chose PMOS common source is that it has better swing voltage as compared to the NMOS common source.

Since it is a two-stage OTA, it is a dipole system. But two poles introduce a very low Phase Margin (we require Phase Margin or PM to be > 70). Hence we manipulate the pole-position of the dominant pole by adding a capacitor Cc and resistor R0 at the output of the first stage, shifting pole P1's position on the Bode Plot to the left. Hence, using the phase plots of pole P2 and Gain-Bandwidth product (GBW), we obtain a reasonable Phase Margin (PM).

Designed the circuit with hand calculations first, by considering that all the transistors are in saturation.

Values considered for hand calculations are as follows :

Gain Bandwidth Product = 15 * 10^6
ICMR(+) = 1.8V
ICMR(-) = 0.6V
Vdd = 2.5V
Length (L) = 500nm
Slew Rate = 30v/us
CL = 2 pF
C1 =C2 = 2 pF
ω−3dB = 2π×15.106 rad/s
un*Cox = 230 u
up*Cox = 30 u

Values obtained after hand calculations :

Cc = 0.9F
ID1 = 15uA
ID2 = 15uA
ID3 = 155uA
ID4 = 15uA
ID5 = 15uA
ID6 = 30uA
ID7 = 30uA
ID8 = 153.55uA
gm1 = 84.82uA/V
gm4 = 82.70 u
Open Loop Gain = gm1.(r04 || r01).gm8(r08 || ro3)
W/L values for all the transistors are given in Table (2).

Comparison between hand calculated values and simulated values :

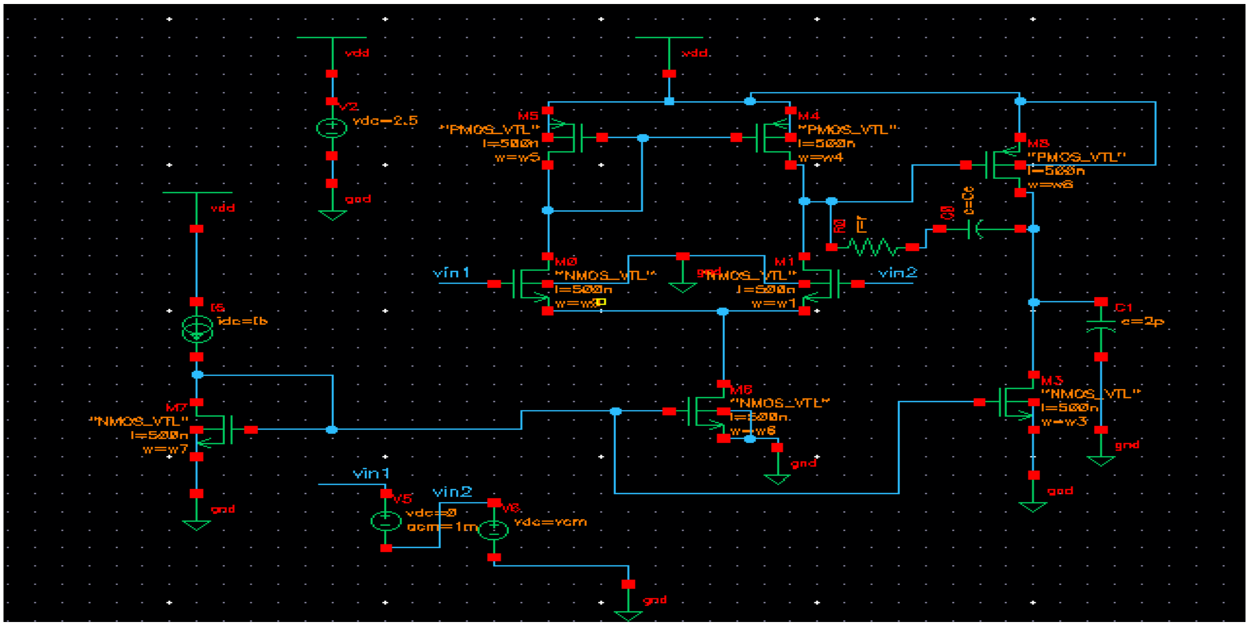
Parameters	Hand calculated	Simulated
(W/L)0	30um	24um
(W/L)1	30um	24um
(W/L)3	38.9um	88um
(W/L)4	3.8um	2um
(W/L)5	3.8um	2um
(W/L)6	7.7um	10um
(W/L)7	7.7um	10um
(W/L)8	38.9um	40um
Slew Rate	30v/us	35.43v/us

Table 2.

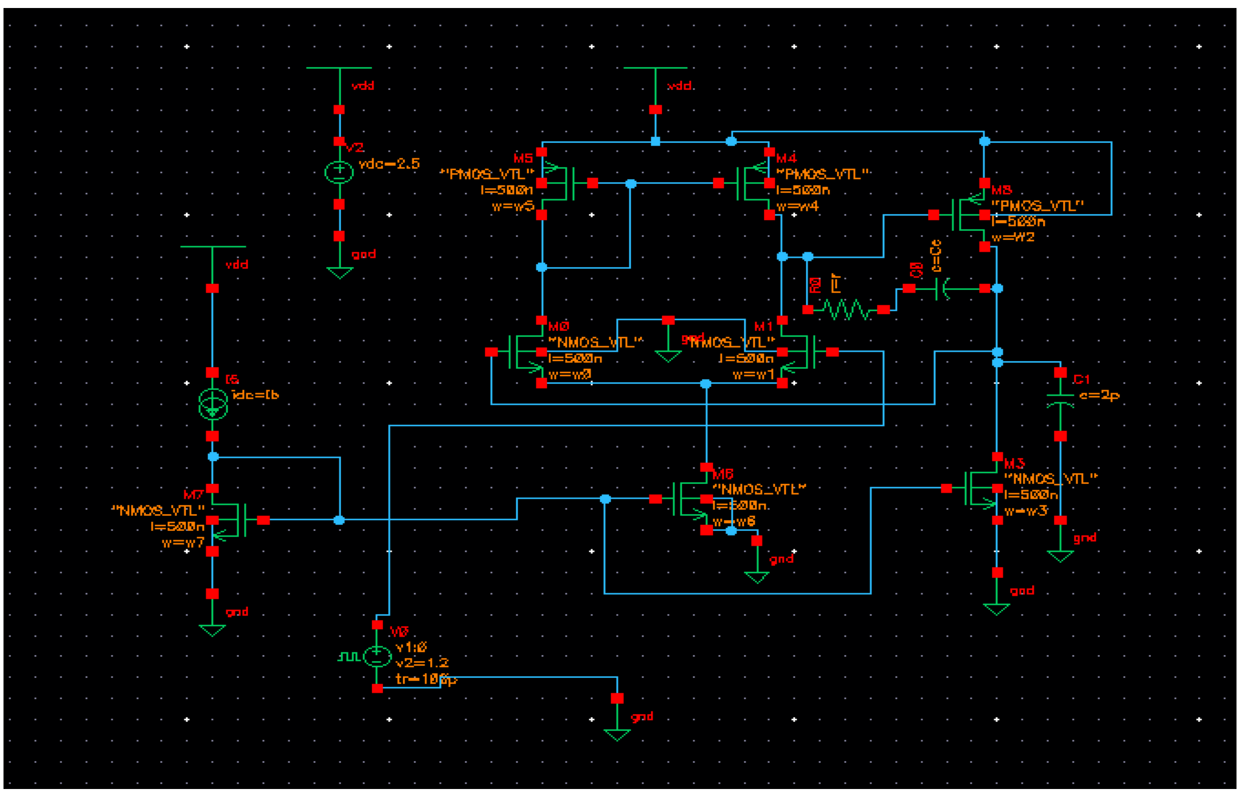
Simulated the schematic of OTA using cadence and obtained the following results :

Open Loop Gain : 66.92dB
3dB Open loop Gain : 63.92dB
Close loop gain : 1.96dB

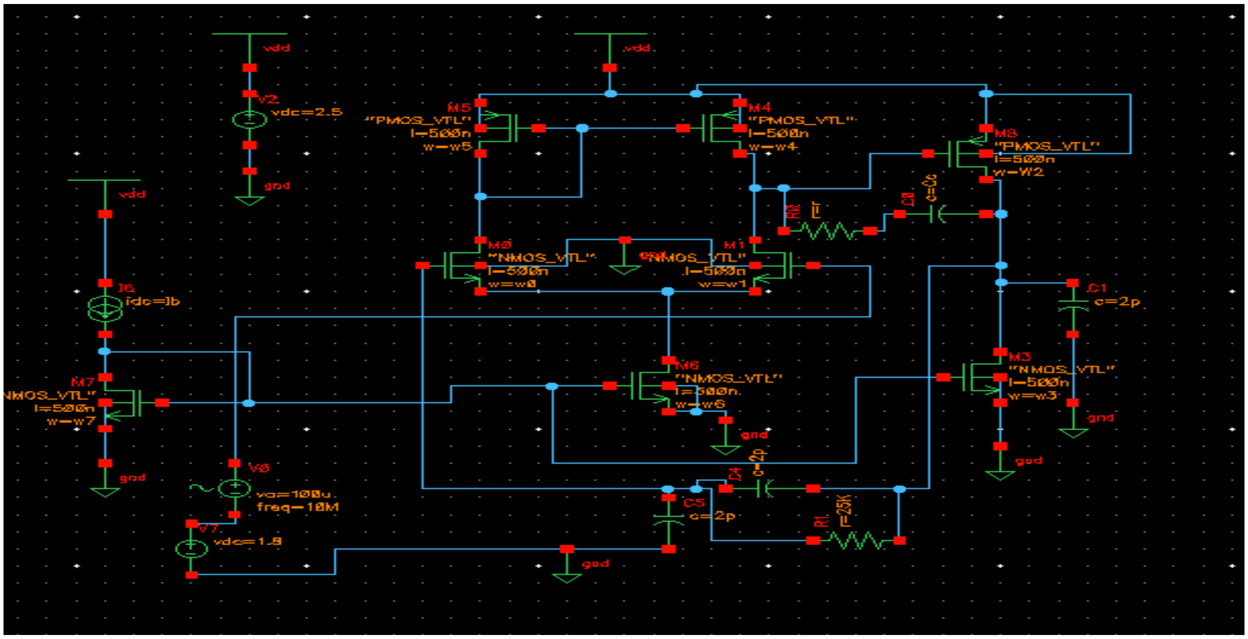
1. **Open Loop Schematic :**



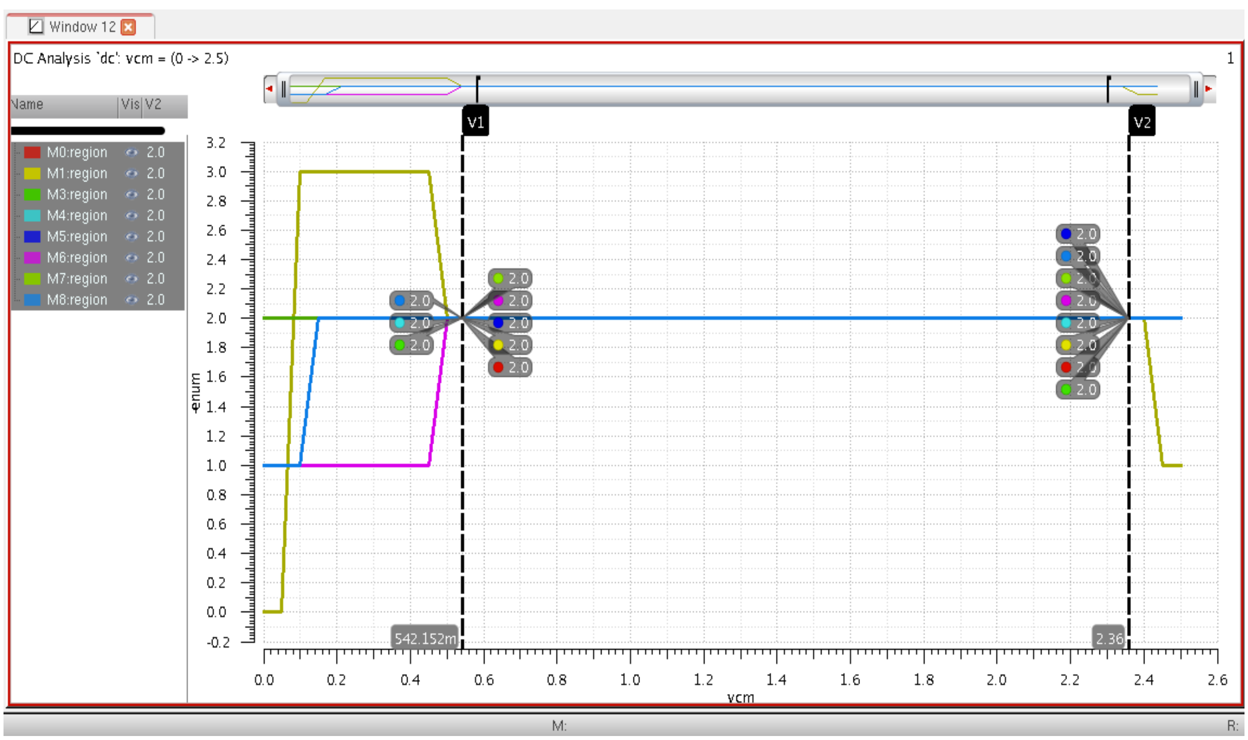
2. **Close Loop Schematic:**



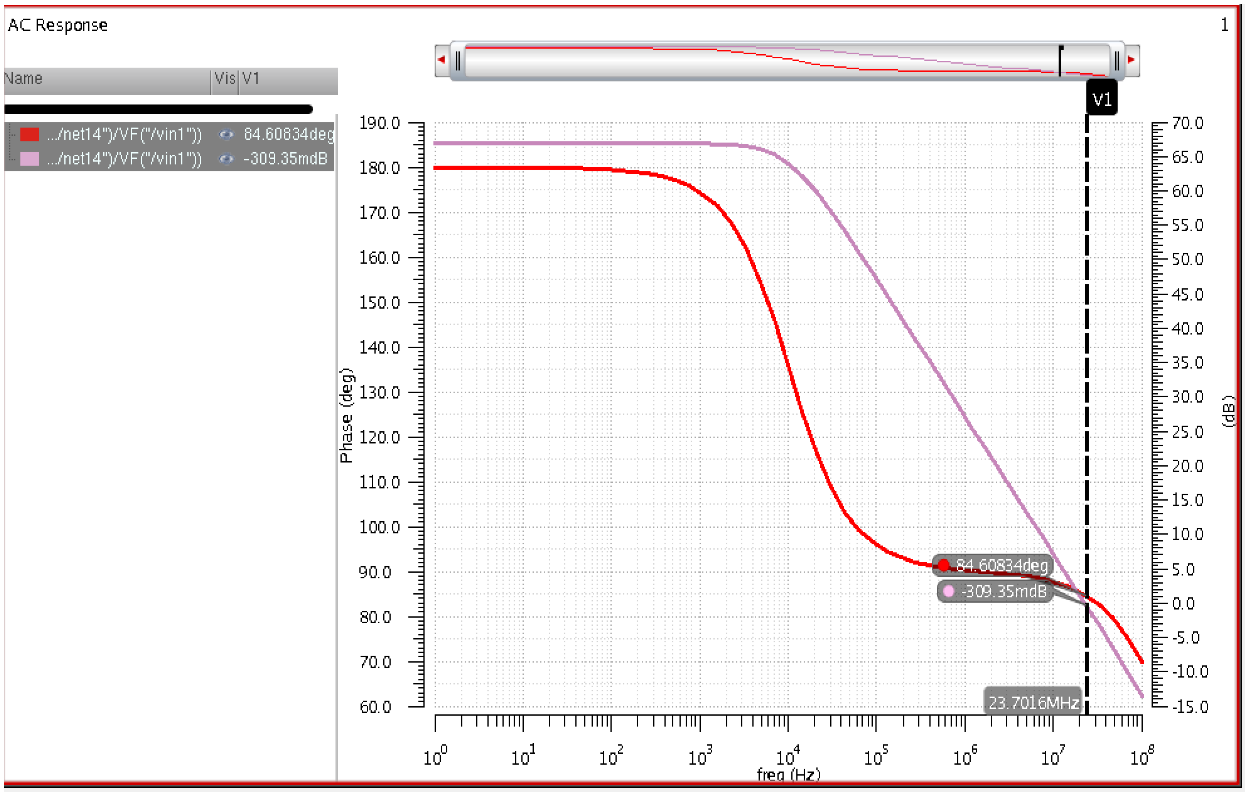
3. Slew Rate Schematic:



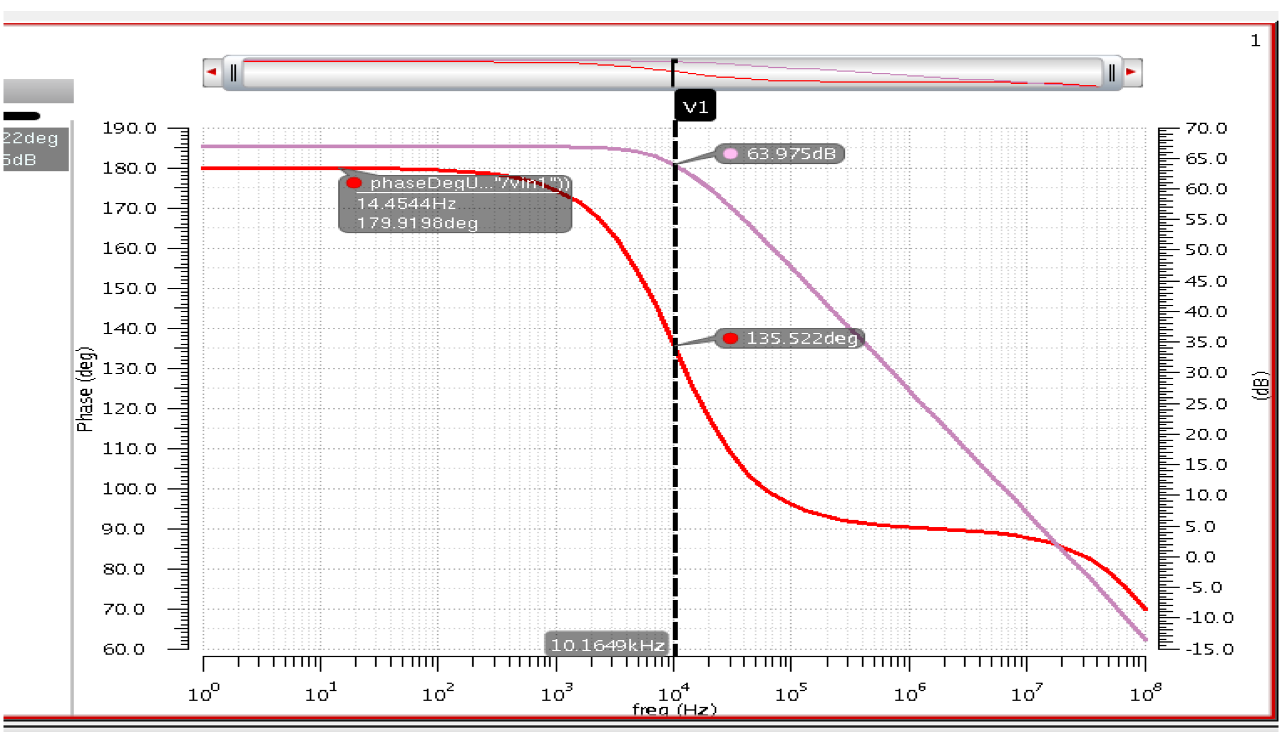
4. MOSFET Regions in saturation :



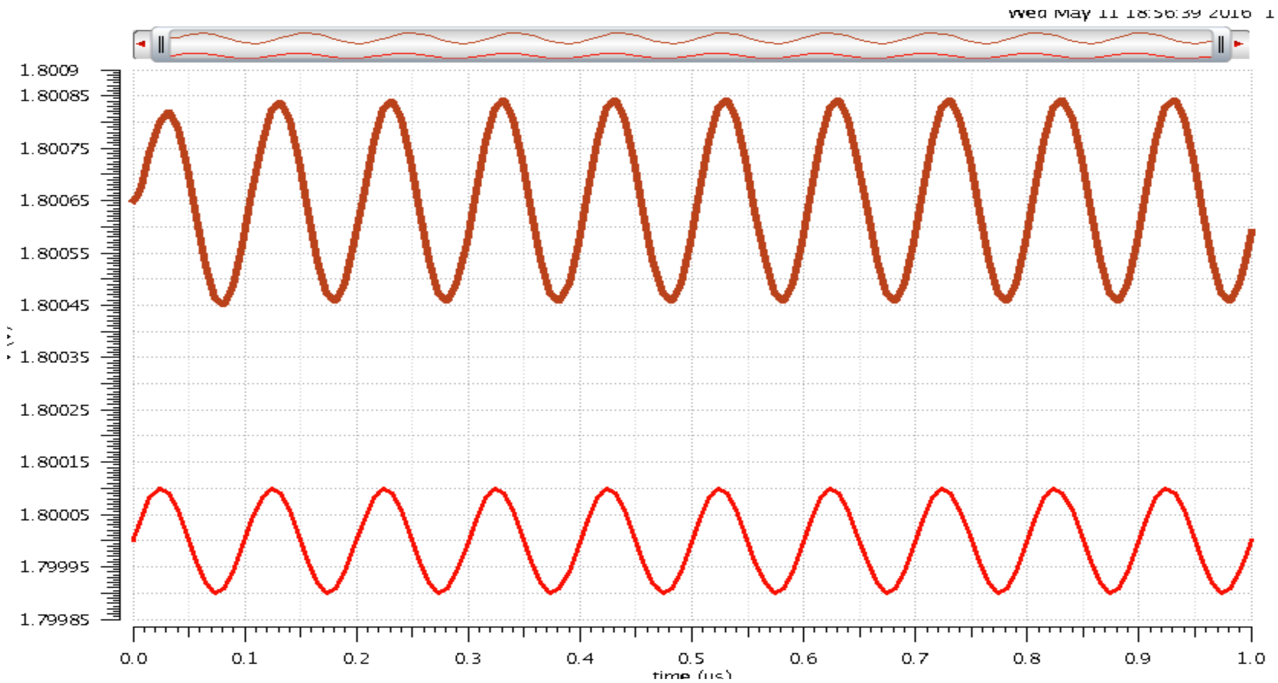
5. Gain and Phase Margin :



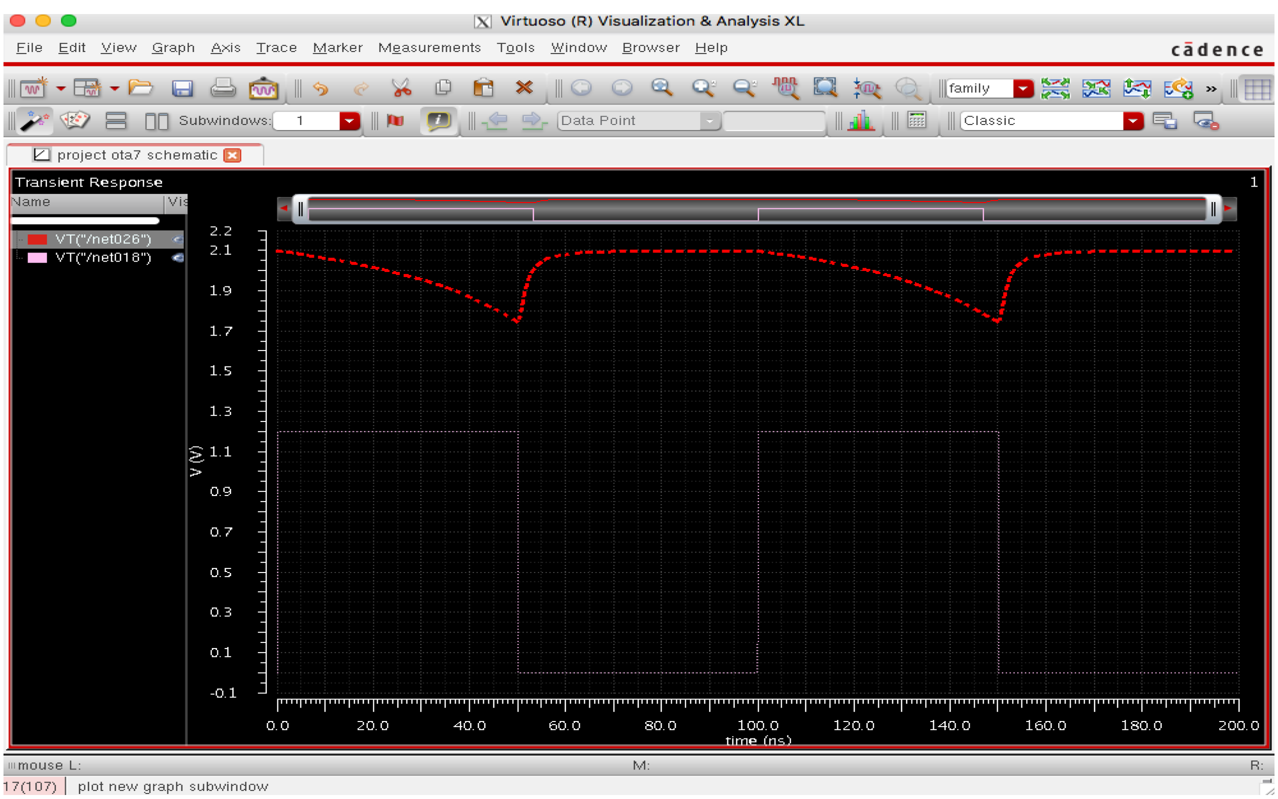
6. Gain and Phase Margin (3dB) :

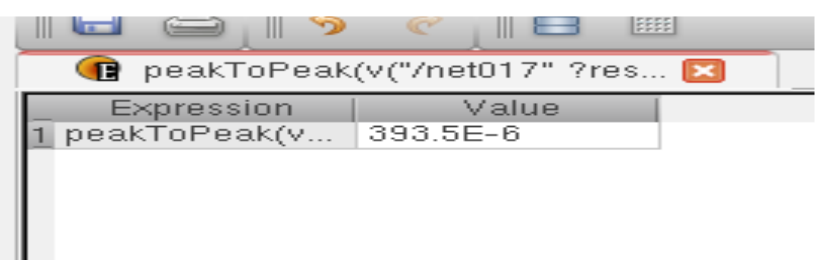


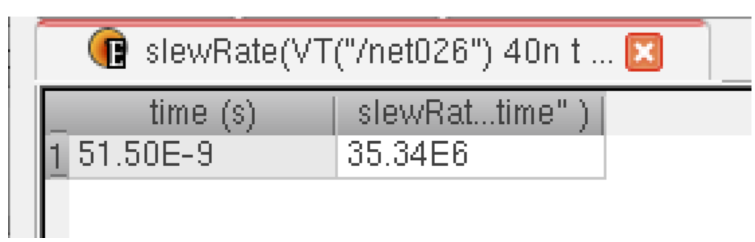
7. Voltage Swing (AC Closed-loop output) :



8. Slew Rate Plot and Value :





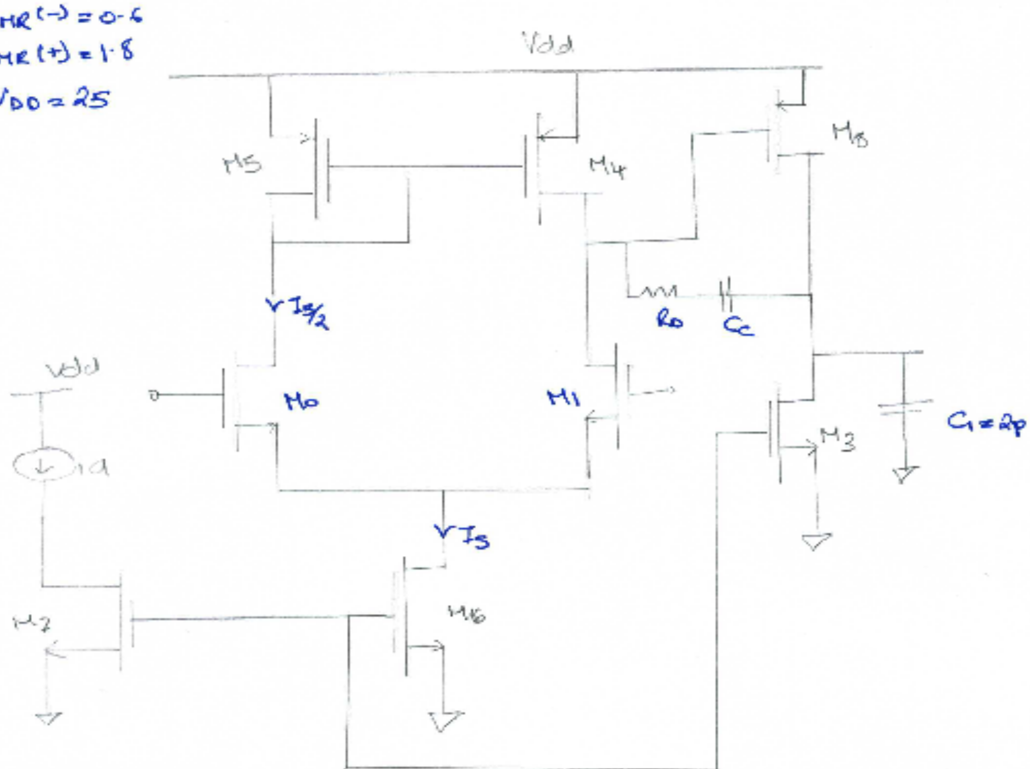


Hand Calculations :

$OCMR^{(-)} = 0.6$

$ICMR(+) = 1.8$

$V_{DD} = 2.5$



$C_L = 2pF$, $C_1 = C_2 = 2pF$

$\omega_{3dB} = 2\pi \times 15 \times 10^6$ rad/s

DC gain = +65

$S.R = 30V/\mu s$

$PM > 70°$

$L = 500\,nm$

$V_{thn} = 0.3220\,V$

$V_{thp} = 0.302\,V$

$\mu_p C_{ox} = 29.8 \approx 30$

$\mu_n C_{ox} = 228.7\mu$

$\approx 230\mu$

$$PM = 84.29 - \tan^{-1}(GBW/P_2)$$

$$70 = 84.29 - \tan^{-1}(GBW/P_2)$$

$$\frac{GBW}{P_2} = 0.25$$

$$P_2 > 3.92\,GBW$$

$$\frac{g_{m8}}{C_L} > 3.92\frac{g_{m1}}{C_c}$$

$$\frac{\cancel{g_{m8}}}{C_L} \geq 3.92\frac{\cancel{g_{m8}}}{10C_c}$$

$$C_c = 0.392\,C_L$$

$$C_c \geq 0.784pF$$

$$C_c = 0.9pF$$

$SR = \frac{I_6}{C_c}$ $\quad I_6 = 30\,\mu A$

For M_1 & M_2 / M_0 & M_1

$$g_{m1} = GBW \times C_c \times 2\pi = 15 \times 10^6 \times 0.9 \times 10^{-12} \times 2\pi$$
$$= 8.4 \times 10^{-5} = 84.82\,\mu$$

$$W/L_1 = \frac{g_{m1}}{\mu_n C_{ox} \times 2 I_D} = \underline{\underline{52}} \simeq 40$$
(by simulation)

$$(W/L)_{3,4} = \frac{2 I_{D3}\, 10^{-6}}{\mu_p C_{ox}[V_{DD} - ICMR^+ - V_{t3}max + V_{t1}min]^2}$$

$(W/L)_{3,4} = 38$

$$V_{ov6} = ICMR - \sqrt{\frac{2 I_{D1}}{\beta_1}} - V_{t1}$$
$$= 197\,mV$$

$$I_{D6} = \frac{\mu_n C_{ox}}{2} (W/L)_6 (V_{ov6})^2$$

$$(W/L)_6 = \frac{2 I_{D6}}{\mu_n C_{ox}(V_{ov})^2} = 7.7$$

for M_7

$$\frac{I_3}{I_6} = \frac{(W/L)_3}{(W/L)_6}$$

$$(W/L)_3 = (W/L)_6 \frac{I_3}{I_6}$$
$$= \frac{155}{30} \times 7.7$$
$$\boxed{(W/L)_3 = 39.78}$$

Open loop gain:

$$A_{DC} = \frac{g_{m1} R_1\, g_{m2} R_2}{g_{m0} R_1\, g_{m2} R_2}$$

$R_1 = r_{o4} \| r_{o1}$ $\quad R_2 = r_{o8} \| r_{o3}$

$$P_2 = \frac{g_{m2} C_c}{g\, C_2 \bar{C}}$$

Open loop Gain

$$A_{DC} = g_{m1} (r_{o4} \| r_{o1})\, g_{m8} (r_{o8} \| r_{o3})$$

$$P_2 = \frac{g_{m2}}{C_2} = \frac{g_{m8}}{C_2}$$

$$P_1 = \frac{1}{g_{m8}\,(r_{o8} \| r_{o3})(r_{o4} \| r_{o1})\,C_c} \qquad Z = \frac{g_{m8}}{C_c}$$

$$GBP = \text{DC gain} \times P_1$$

$$= \frac{g_{m1}\,\cancel{g_{m8}}\,\cancel{R_1}\cancel{R_2} \times 1}{\cancel{g_{m8}}\,\cancel{R_1}\cancel{R_2}\,C_c} = \frac{g_{m1}}{C_c}$$

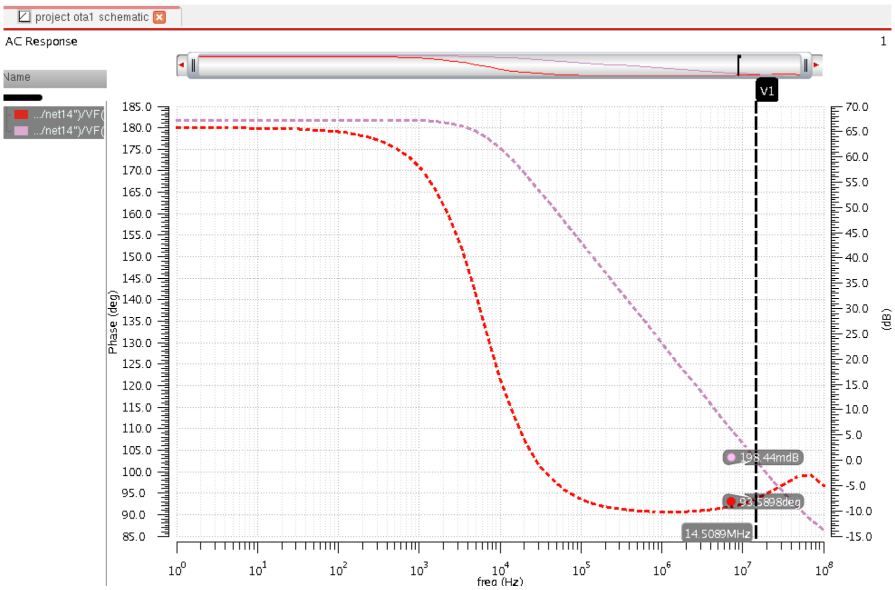
$$Z \geq 10\,GBP$$

$$\angle = -\tan^{-1}\left(\omega/Z\right) - \tan^{-1}\left(\omega/P_1\right) - \tan^{-1}\left(\omega/P_2\right)$$

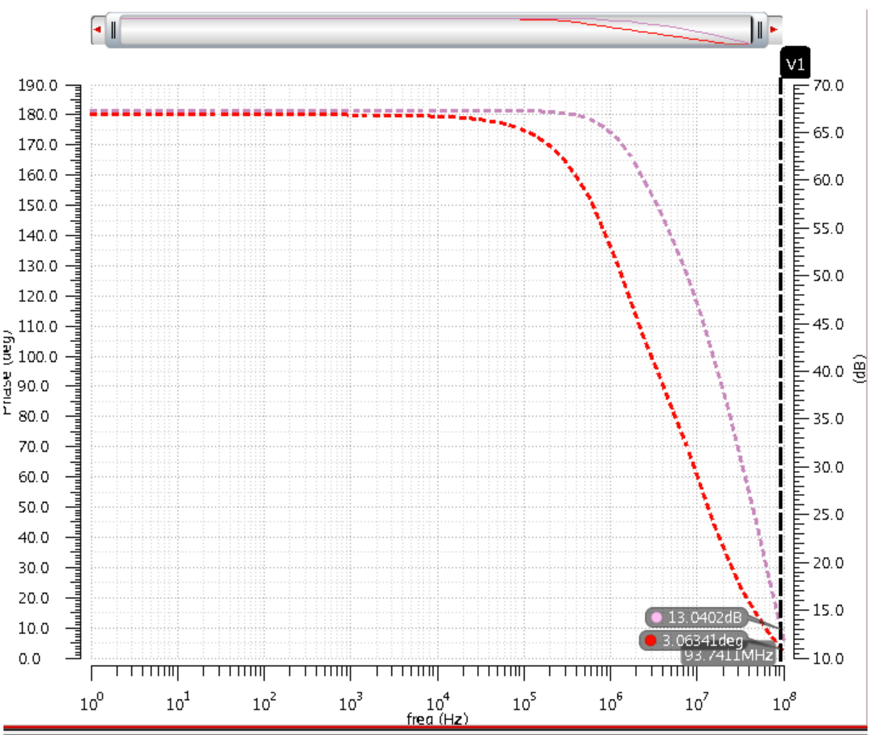
$$= -\tan^{-1}\left(1/10\right) - \tan^{-1}\left(\frac{g_{m7}}{C_c P_1}\right)$$

Proof of Theory:

Based on the formula used for the hand calculations and simulations, our Phase Margin would increase and Slew Rate would decrease if we increase Cc or Resistance from stage 1 output to stage 2 input. In Example 1, Cc5 is the plot whene we take Cc as 5pF. Phase Margin goes very high



In Example 2, CC001 has Cc as 0.01pF and Phase Margin goes down to 13.



Conclusion:

We are able to design the Two Stage Operational Transconductance Amplifier in a manner that satisfies the constraints. While the closed-loop gain we achieved by simulations was 1.95 (expected to be 2), most conditions were met during simulations. Further investigations need to be performed to find the reason for the low Close Loop gain. Finally, our choice was determined by the following comparison between the different Operational Amplifier Design Methods [5]:

Topology	Gain	Output Swing	Speed	Power
Two-stage	High	Highest	Low	Medium
Telescopic	Medium	Medium	Highest	Low
Folded cascade	Medium	Medium	High	Highest

Table 3. [5]

References:

[1] A High-Swing CMOS Telescopic Operational Amplifier Kush Gulati and Hae-Seung Lee, Fellow, IEEE, IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998

[2] Operational Amplifier Design with Gain-Enhancement Differential Amplifier Phuoc T. Tran University of Idaho Herbert L. Hess University of Idaho Kenneth V. Noren University of Idaho, IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society,September 2012

[3] A Folded-Cascode OP Amp with a Dynamic Switching Bias Circuit, Hiroo Wakaumi Division of Electronics and Information Engineering, Monozukuri Engineering Department Tokyo Metropolitan College of Industrial Technology Tokyo, Japan, Circuits and Systems (APCCAS), 2014 IEEE Asia Pacific Conference on 17-20 Nov. 2014, pg 53 – 56

[4] A novel feed-forward compensation technique for single-stage fully-differential CMOS folded cascode rail-to-rail amplifier, S. M. Rezaul Hasan · Nazmul Ula. Electrical Engineering (2006) 88: 509–517, 20 December 2005

[5] Design and Analysis of a Two-Stage OTA for Sensor Interface Circuit, Siti Nur Syuhadah Baharudin, Asral Bahari Jambek and Rizalafande Che Ismail, School of Microelectronic Engineering, Universiti Malaysia Perlis, Malaysia, 2014 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE) , April 7 - 8, 2014, Penang, Malaysia