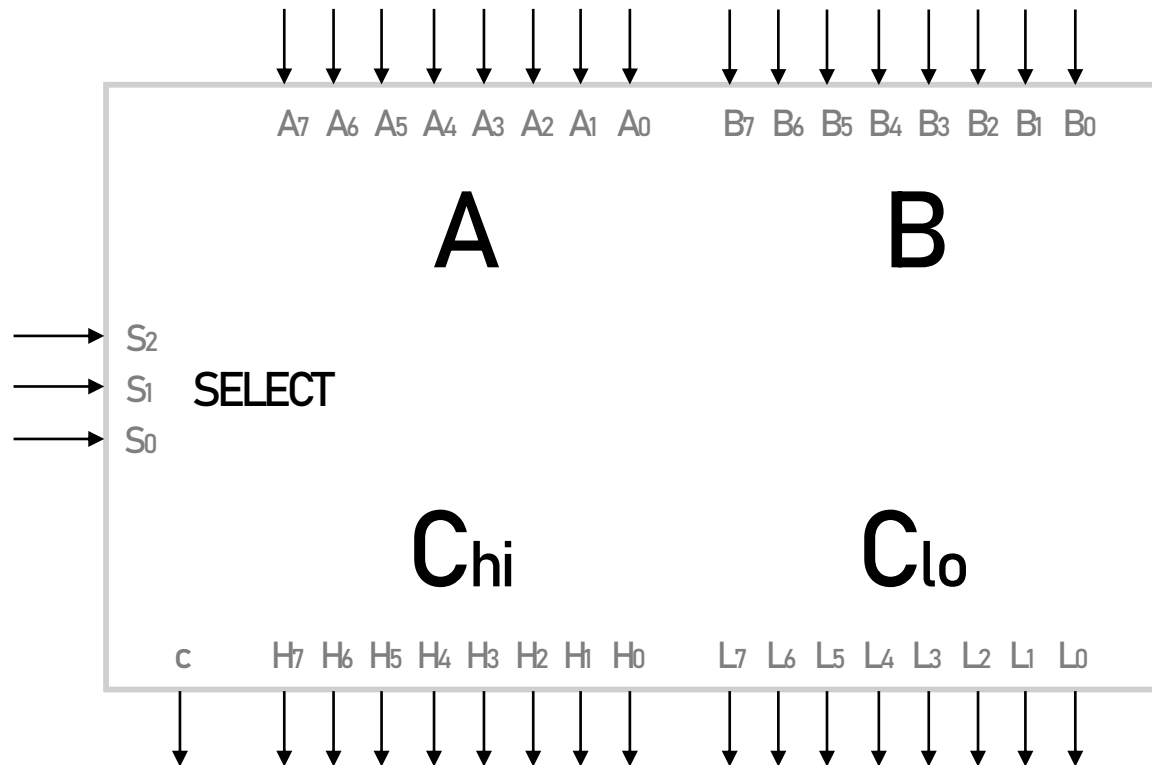
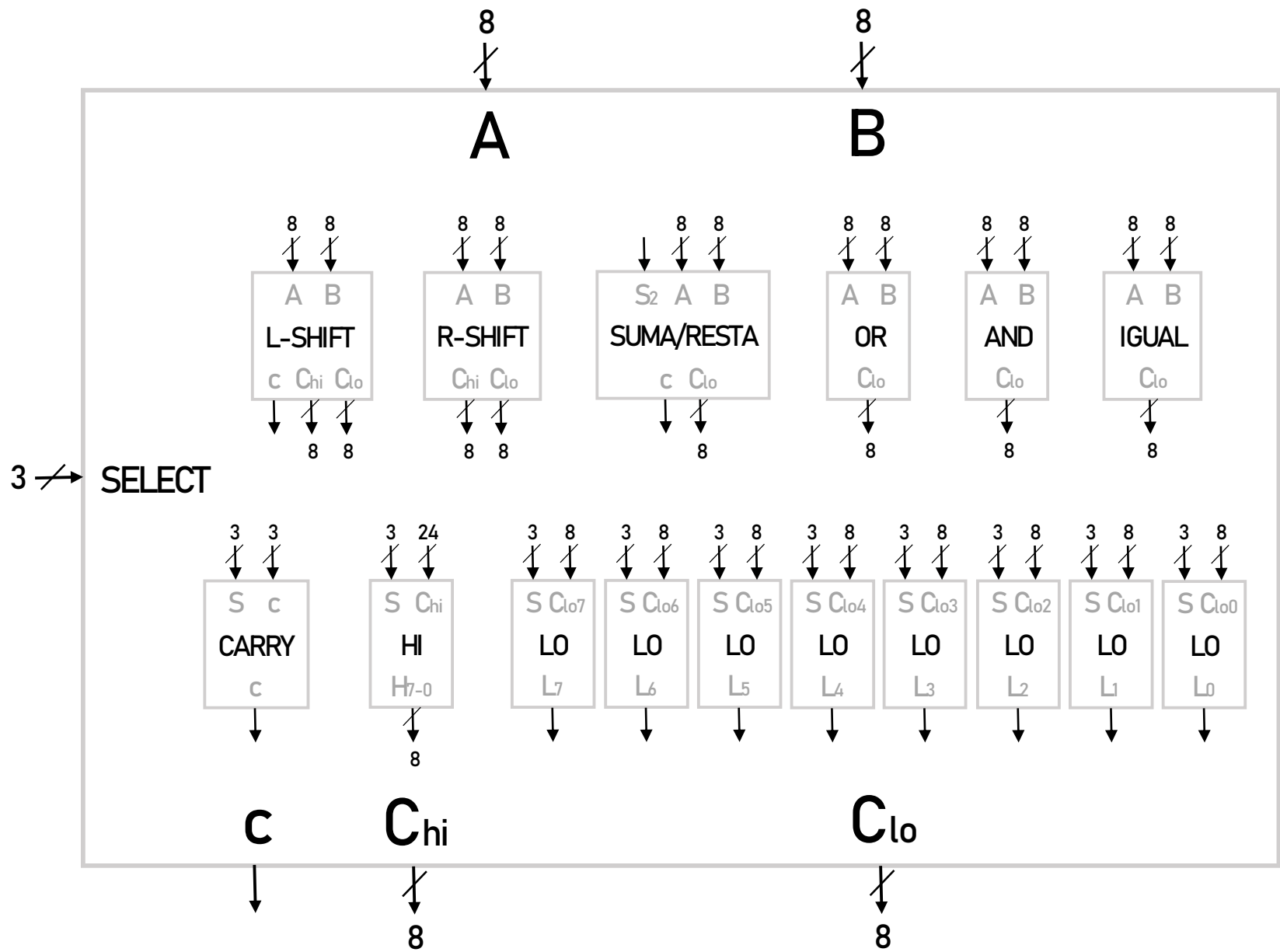
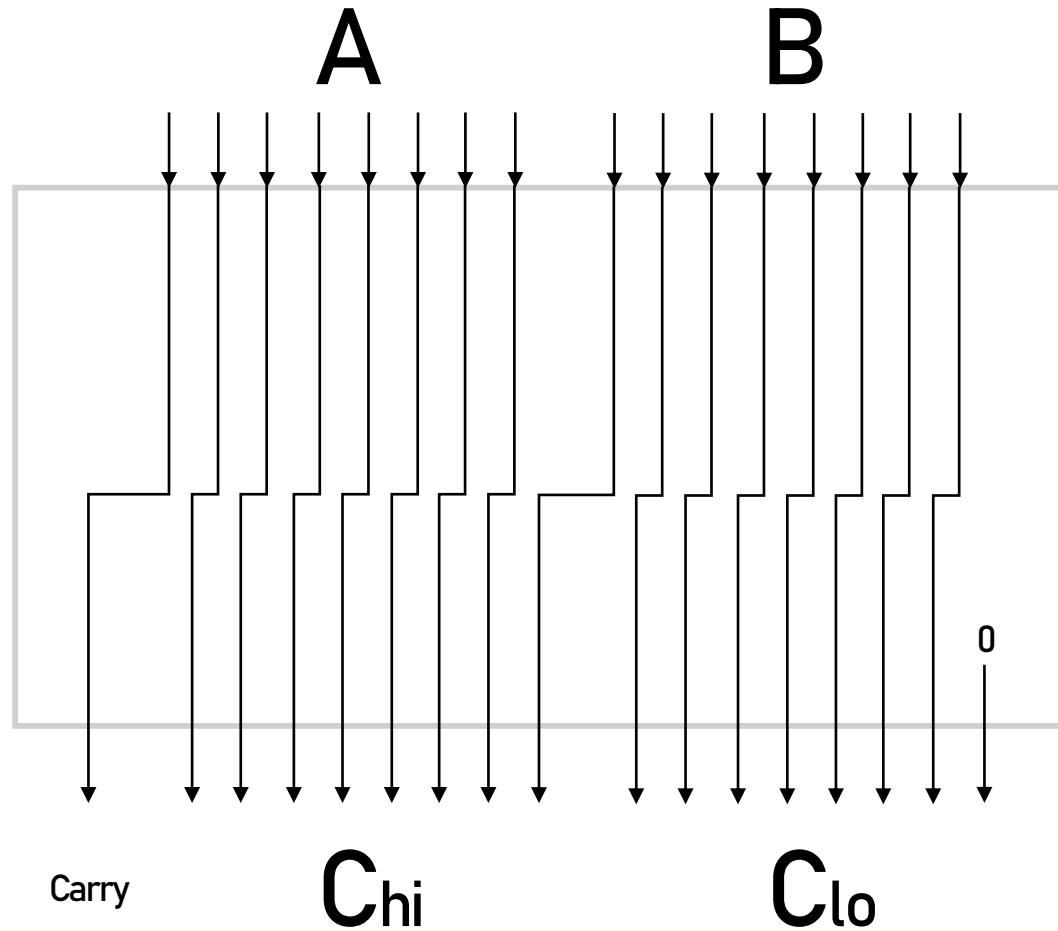


# DISEÑO CPU

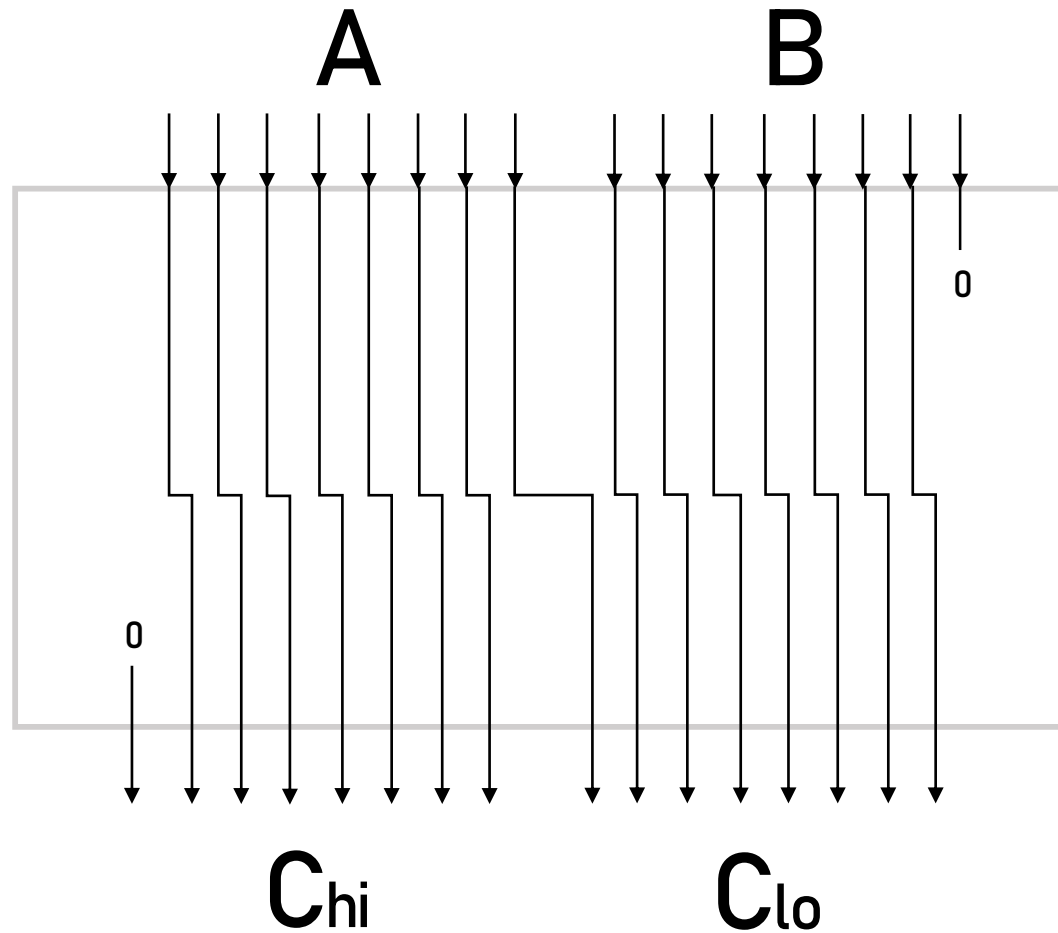




# L-SHIFT



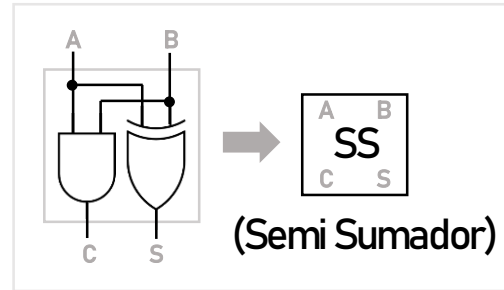
# R-SHIFT



The diagram shows a logic circuit for a Semi Sumador. It has two inputs, A and B. Input A is connected to the top input of an AND gate and the bottom input of an XOR gate. Input B is connected to the top input of an XOR gate and the bottom input of an AND gate. The output of the AND gate is labeled C (Carry). The output of the XOR gate is labeled S (Sum). An arrow points from the circuit to a truth table.

A	B	SS	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

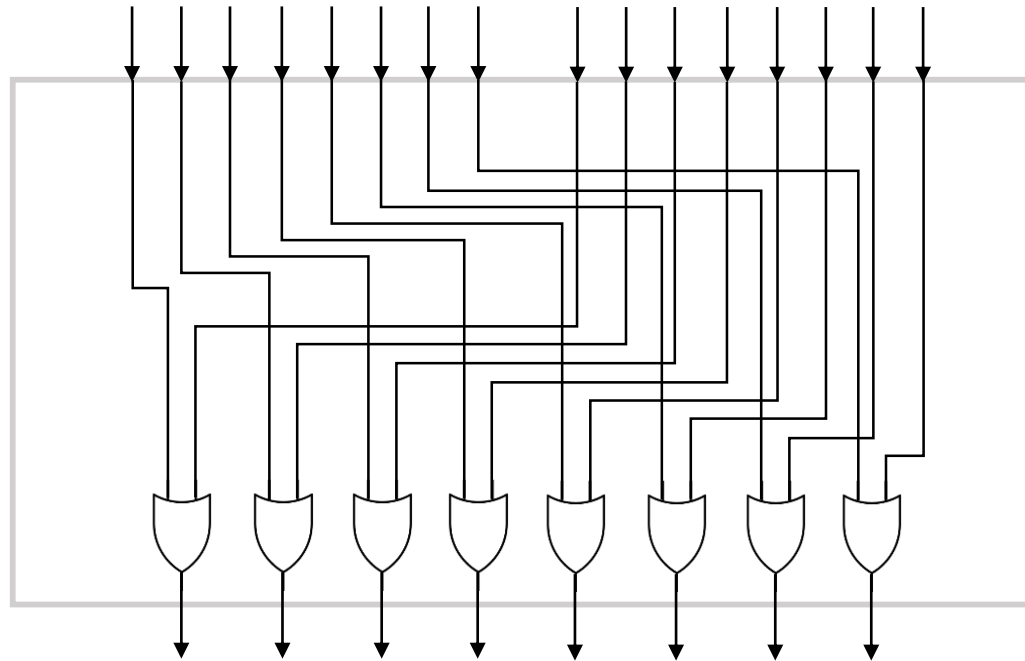
(Semi Sumador)



OR

A

B

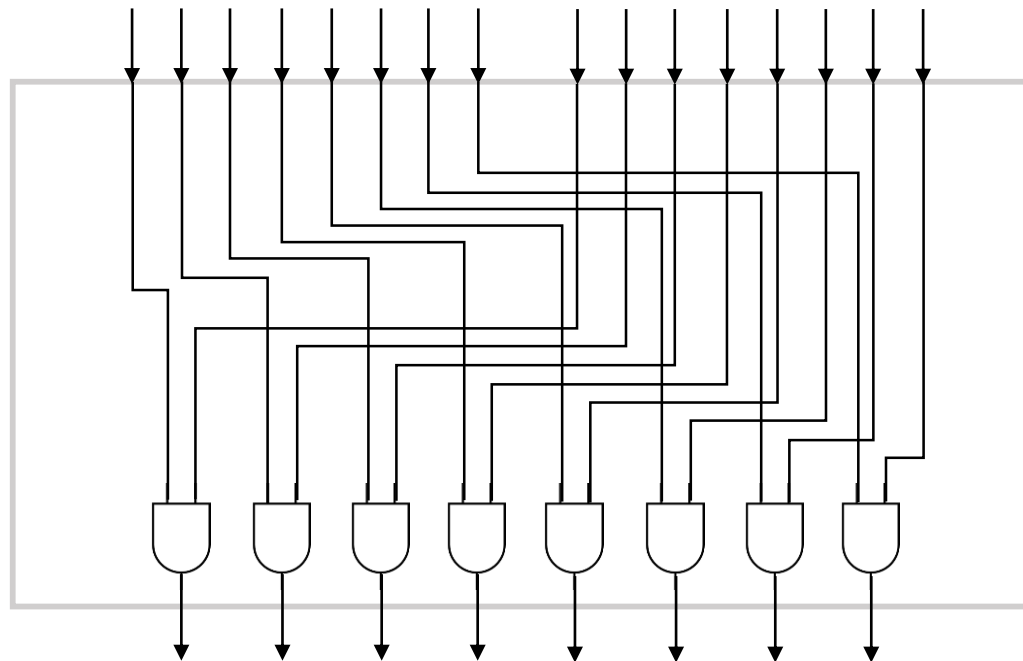


C<sub>lo</sub>

# AND

## A

## B

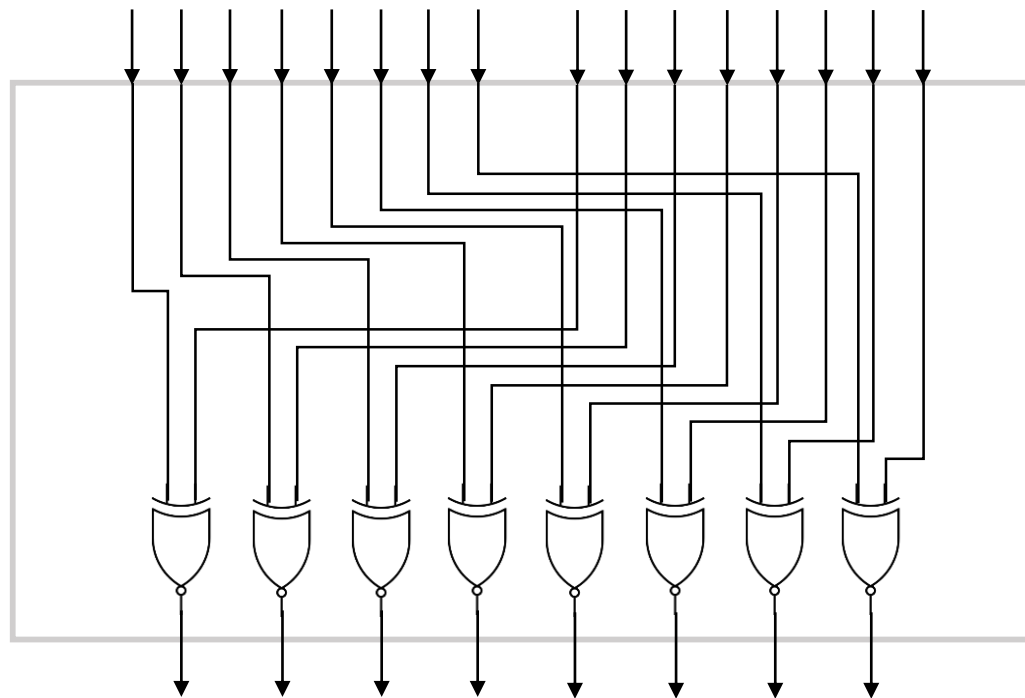


## C<sub>lo</sub>

# IGUAL

## A

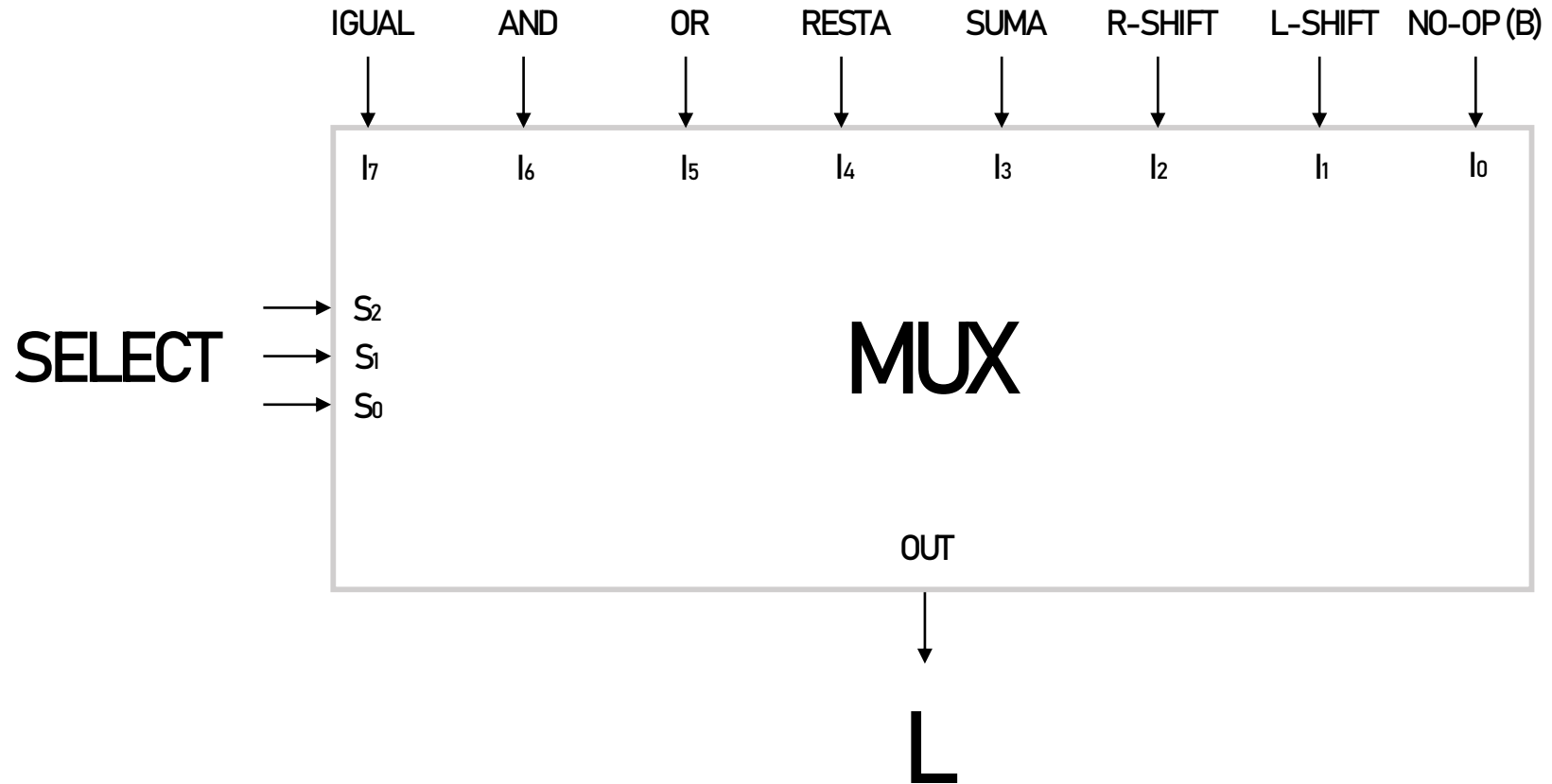
## B

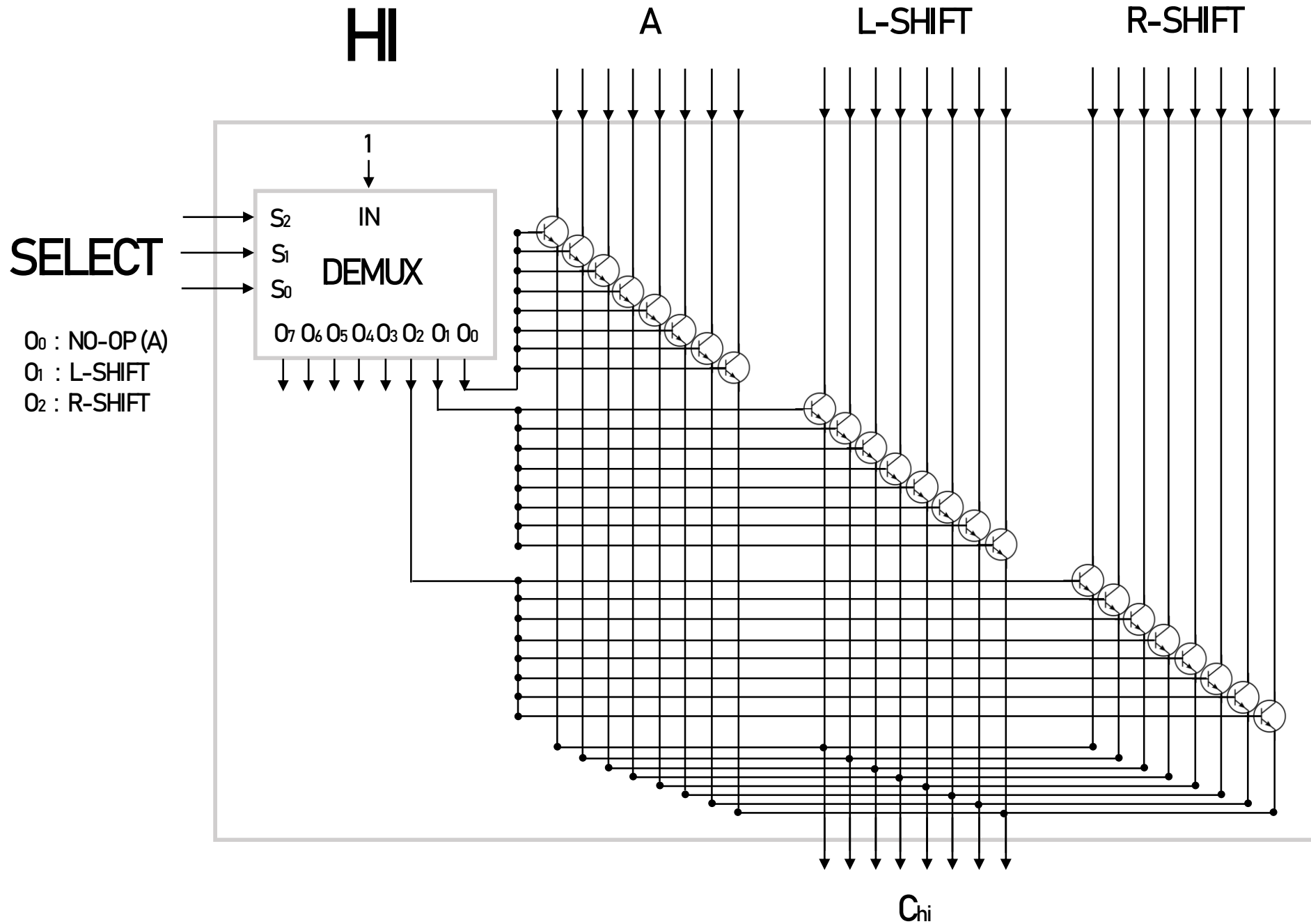


## C<sub>lo</sub>



# L0





CARRY

