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Carné:19659
Sección 21

Electrónica digital
Laboratorio 4

EJERCICIO 1

Tabla No. 1

A	B	C	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

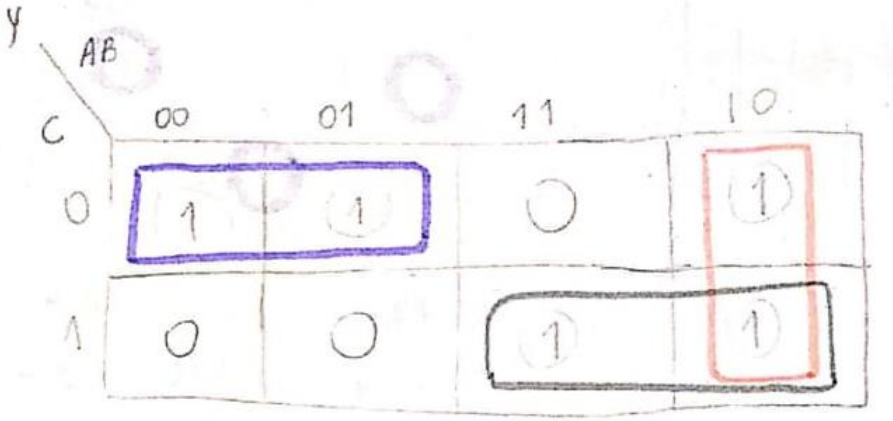


Tabla No 2

A	B	C	y
0	0	0	1
0	0	1	x
0	1	0	0
0	1	1	0
1	0	0	x
1	0	1	1
1	1	0	0
1	1	1	0

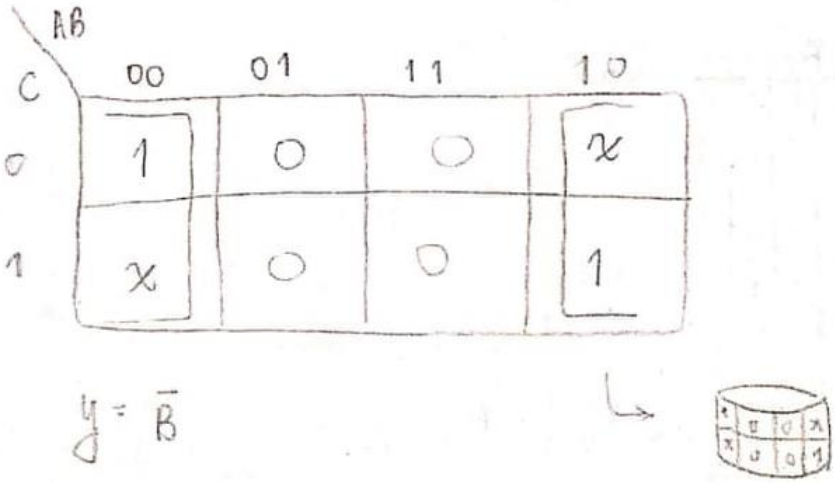


Tabla 3

A	B	C	D	y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

CD \ AB	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

$y = A'B'C'D' + ABC'D' + A'BC'D + AB'C'D + A'B'CD + ABCD + A'BCD' + AB'CD'$

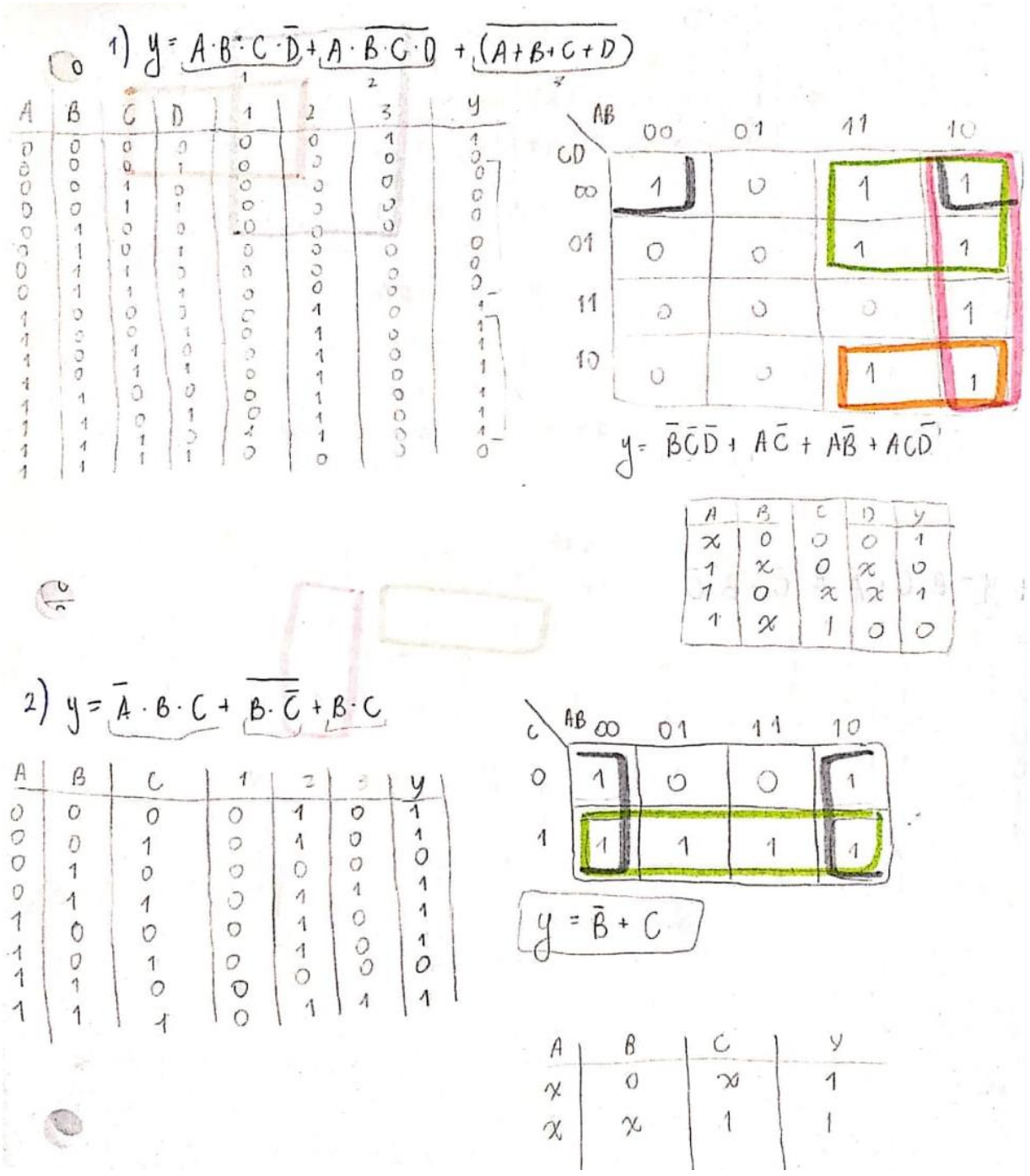
Tabla No. 4

A	B	C	D	y
0	0	0	0	x
0	0	0	1	x
0	0	1	0	0
0	0	1	1	0
0	1	0	0	x
0	1	0	1	x
0	1	1	0	1
0	1	1	1	0
1	0	0	0	x
1	0	0	1	x
1	0	1	0	1
1	0	1	1	x
1	1	0	0	1
1	1	0	1	1
1	1	1	0	x
1	1	1	1	1

CD \ AB	00	01	11	10
00	x	0	1	1
01	x	x	1	0
11	0	x	1	1
10	x	0	x	x

$y = A\bar{C}\bar{D} + BD + AC$

EJERCICIO 2



3. $y = \overline{(A + B + \bar{C}\ D) + A \cdot D + B)}$

A	B	C	D	1	2	y
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	0	0
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	1	1

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	0	1	1	1
10	0	1	1	0

$y = B + AD$

A	B	C	D	y
x	1	x	x	1
1	x	x	1	1

4. $y = B \cdot C + \bar{A} \cdot \bar{B} \cdot \bar{C} + B \cdot \bar{C}$

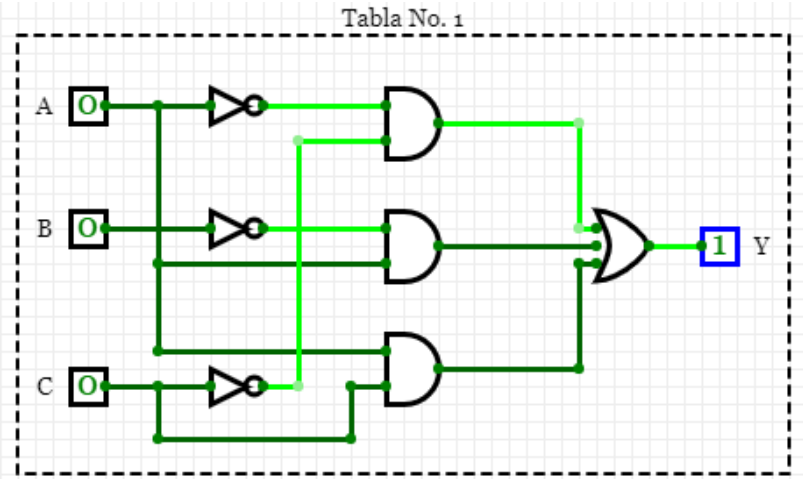
A	B	C	1	2	3	y
0	0	0	0	1	0	1
0	0	1	0	0	0	0
0	1	0	0	0	1	1
0	1	1	0	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	0	1	1
1	1	1	1	0	0	1

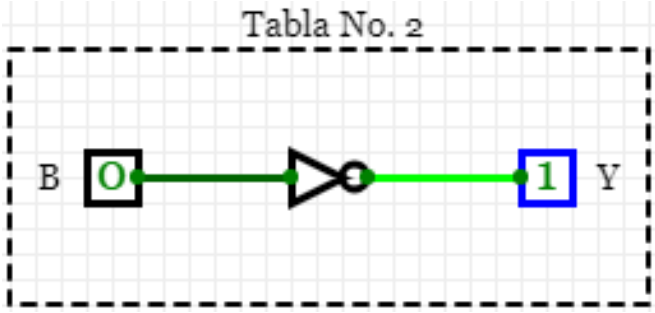
CD \ AB	00	01	11	10
0	1	1	1	0
1	0	0	1	0

$y = \bar{A}\bar{C} + AB$

A	B	C	y
0	x	0	1
1	1	x	1

EJERCICIO 3 y 4





Código TABLA_1 y TABLA_2

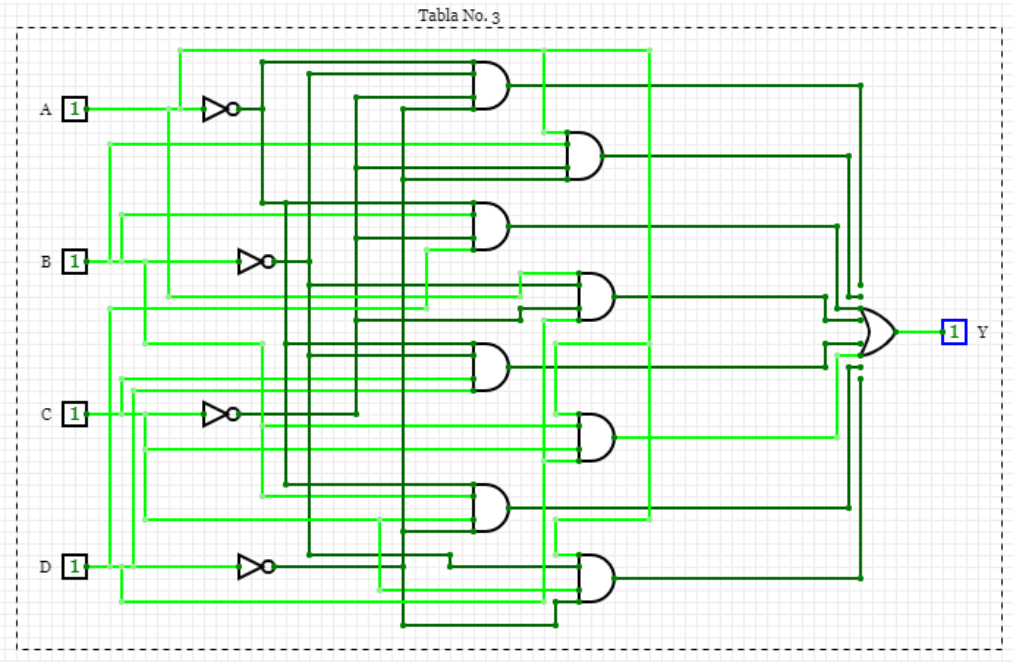
A	B	C	Y	Y1
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	0

Settings | Lab_4.v | 01_TABLA_POS.v | Telemetry Consent

```
// Ecuación a implementar y = (A' * C') + (A * C) + (A * B')

module TABLA_1(input wire A, B, C, output wire Y); // Generar y nombr


wire u1, u2, u3, u4, u5, u6; // Nombres de los cables

// Declaración de las compuertas
not(u1, A);
not(u2, B);
not(u3, C);
and(u4, u1,u3);
and(u5, A,C);
and(u6, A,u2);
or(Y, u4,u5,u6);

endmodule


// Ecuación a implementar Y1 = B'

module TABLA_2(input wire A, B, C, output wire Y1);  // Nombres de lo

// Declaración de las compuertas
not(Y1, B);

endmodule
```

Lab_4_tb.v

```
//------------------------------Valerie Valdez-----------------

module testbench();

// TABLA_1 Y TABLA_2
reg s1, s2, s3;
wire led1, led2;

TABLA_1 G1(s1,s2,s3, led1);
TABLA_2 G2(s1,s2,s3, led2);

initial begin
  $display("A B C | Y Y1");
  $display("------|---");
  $monitor("%b %b %b | %b %b", s1,s2,s3, led1, led2);

      s1 = 0; s2 = 0; s3 = 0;
      #1 s1 = 0; s2 = 0; s3 = 1;
      #1 s1 = 0; s2 = 1; s3 = 0;
      #1 s1 = 0; s2 = 1; s3 = 1;
      #1 s1 = 1; s2 = 0; s3 = 0;
      #1 s1 = 1; s2 = 0; s3 = 1;
      #1 s1 = 1; s2 = 1; s3 = 0;
      #1 s1 = 1; s2 = 1; s3 = 1;

end
```

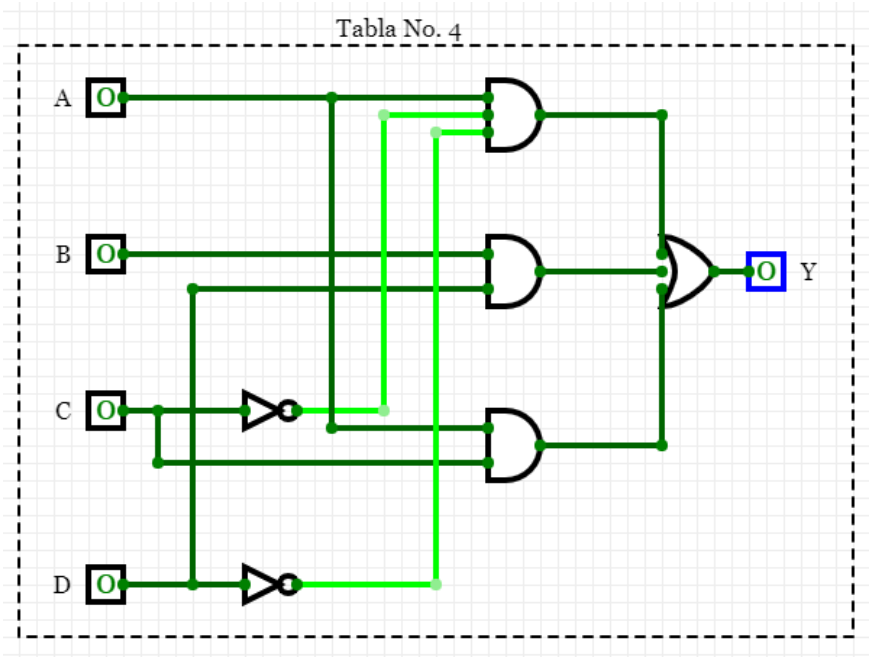


A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

```
37
38  module TABLA_3(input wire A, B, C, D, output wire Y);
39
40  assign Y = (~A & ~B & ~C & ~D) | (A & B & ~C & ~D) | (~A & B & ~C & D) | (A & ~B & ~C & D) | (~A & ~B & C & D) | (A & B & C & D) | (~A & B & C & ~D) | (A & ~B & C & ~D);
41
42  endmodule
43
```

Lab_4_tb.v

```
28
29  // TABLA_3
30  reg t1, t2, t3, t4;
31  wire led3;
32
33  TABLA_3 G3 (t1,t2,t3,t4, led3);
34
35  initial begin
36    #8
37    $display("\n");
38    $display("A B C D | Y ");
39    $display("--------|---");
40    $monitor("%b %b %b %b | %b", t1,t2,t3,t4, led3);
41
42        t1 = 0; t2 = 0; t3 = 0; t4 = 0;
43        #1 t1 = 0; t2 = 0; t3 = 0; t4 = 1;
44        #1 t1 = 0; t2 = 0; t3 = 1; t4 = 0;
45        #1 t1 = 0; t2 = 0; t3 = 1; t4 = 1;
46        #1 t1 = 0; t2 = 1; t3 = 0; t4 = 0;
47        #1 t1 = 0; t2 = 1; t3 = 0; t4 = 1;
48        #1 t1 = 0; t2 = 1; t3 = 1; t4 = 0;
49        #1 t1 = 0; t2 = 1; t3 = 1; t4 = 1;
50        #1 t1 = 1; t2 = 0; t3 = 0; t4 = 0;
51        #1 t1 = 1; t2 = 0; t3 = 0; t4 = 1;
52        #1 t1 = 1; t2 = 0; t3 = 1; t4 = 0;
53        #1 t1 = 1; t2 = 0; t3 = 1; t4 = 1;
54        #1 t1 = 1; t2 = 1; t3 = 0; t4 = 0;
55        #1 t1 = 1; t2 = 1; t3 = 0; t4 = 1;
56        #1 t1 = 1; t2 = 1; t3 = 1; t4 = 0;
57        #1 t1 = 1; t2 = 1; t3 = 1; t4 = 1;
58
```



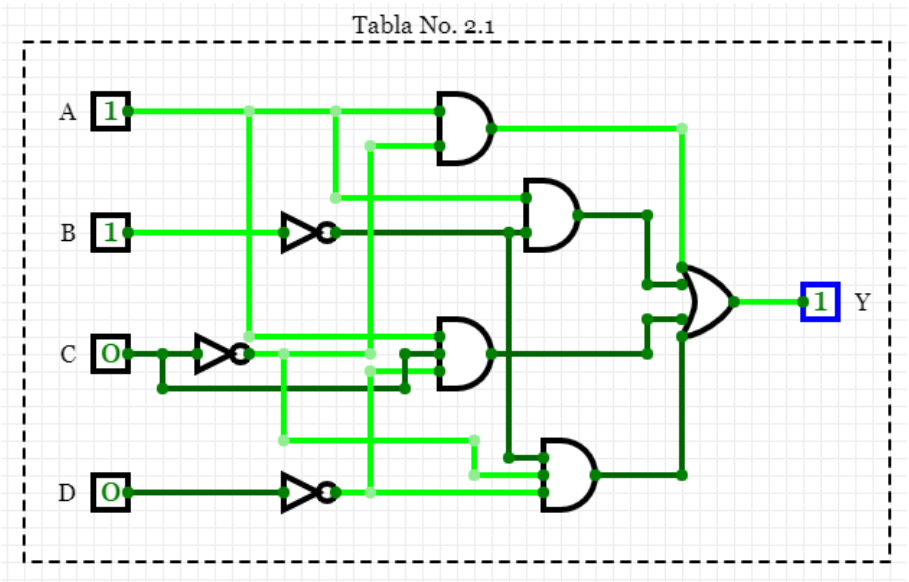
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Settings | Lab_4.v | 01_TABLA_POS.v | Telemetry Cons...

```
43
44
45  //Ecuación a implementar Y = AC'D' + BD + AC
46
47  module TABLA_4(input wire A, B, C, D, output wire Y);
48
49  wire w1, w2, w3, w4, w5;
50
51  not(w1, C);
52  not(w2, D);
53  and(w3, A,w1,w2);
54  and(w4, B,D);
55  and(w5, A,C);
56  or(Y, w3,w4,w5);
57
58  endmodule
59
60
61  // Ecuación a implementar Y = B'C'D' + AC' + AB' + ACD'
62  module TABLA_5(input wire A, B, C, D, output wire Y1);
63
64  wire r1, r2, r3, r4, r5, r6, r7;
65
66  not(r1, B);
67  not(r2, C);
68  not(r3, D);
69  and(r4, r1,r2,r3);
70  and(r5, A,r2);
71  and(r6, A,r1);
72  and(r7, A,C,r3);
73  or(Y1, r4,r5,r6,r7);
74
75  endmodule
76
```

Lab_4_tb.v

```
59  end
60
61  // TABLA_4 y TABLA_5
62  reg q1, q2, q3, q4;
63  wire led4, led5;
64
65  TABLA_4 G4 (q1,q2,q3,q4, led4);
66  TABLA_5 G5 (q1,q2,q3,q4, led5);
67
68  initial begin
69    #24
70    $display("\n");
71    $display("A B C D | Y Y1");
72    $display("--------|-----");
73    $monitor("%b %b %b %b | %b %b", q1,q2,q3,q4, led4, led5);
74
75        q1 = 0; q2 = 0; q3 = 0; q4 = 0;
76        #1 q1 = 0; q2 = 0; q3 = 0; q4 = 1;
77        #1 q1 = 0; q2 = 0; q3 = 1; q4 = 0;
78        #1 q1 = 0; q2 = 0; q3 = 1; q4 = 1;
79        #1 q1 = 0; q2 = 1; q3 = 0; q4 = 0;
80        #1 q1 = 0; q2 = 1; q3 = 0; q4 = 1;
81        #1 q1 = 0; q2 = 1; q3 = 1; q4 = 0;
82        #1 q1 = 0; q2 = 1; q3 = 1; q4 = 1;
83        #1 q1 = 1; q2 = 0; q3 = 0; q4 = 0;
84        #1 q1 = 1; q2 = 0; q3 = 0; q4 = 1;
85        #1 q1 = 1; q2 = 0; q3 = 1; q4 = 0;
86        #1 q1 = 1; q2 = 0; q3 = 1; q4 = 1;
87        #1 q1 = 1; q2 = 1; q3 = 0; q4 = 0;
88        #1 q1 = 1; q2 = 1; q3 = 0; q4 = 1;
89        #1 q1 = 1; q2 = 1; q3 = 1; q4 = 0;
90        #1 q1 = 1; q2 = 1; q3 = 1; q4 = 1;
91
92  end
```




```
A B C D | Y Y1
--------|-----
0 0 0 0 | 0 1
0 0 0 1 | 0 0
0 0 1 0 | 0 0
0 0 1 1 | 0 0
0 1 0 0 | 0 0
0 1 0 1 | 1 0
0 1 1 0 | 0 0
0 1 1 1 | 1 0
1 0 0 0 | 1 1
1 0 0 1 | 0 1
1 0 1 0 | 1 1
1 0 1 1 | 1 1
1 1 0 0 | 1 1
1 1 0 1 | 1 1
1 1 1 0 | 1 1
1 1 1 1 | 1 0
```

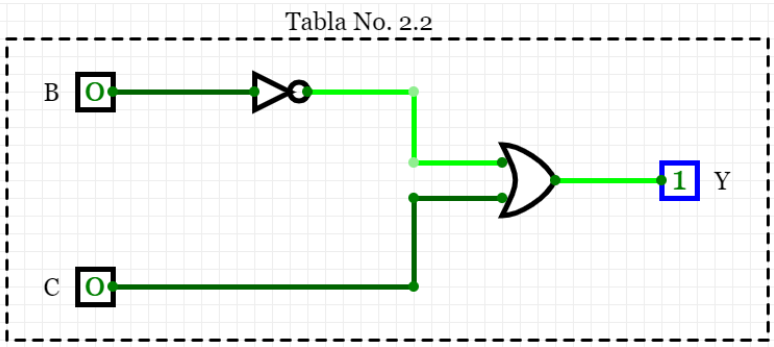
Settings | Lab_4.v | 01_TABLA_POS.v | Telemetry Cons...

```
43
44
45  //Ecuación a implementar Y = AC'D' + BD + AC
46
47  module TABLA_4(input wire A, B, C, D, output wire Y);
48
49  wire w1, w2, w3, w4, w5;
50
51  not(w1, C);
52  not(w2, D);
53  and(w3, A,w1,w2);
54  and(w4, B,D);
55  and(w5, A,C);
56  or(Y, w3,w4,w5);
57
58  endmodule
59
60
61  // Ecuación a implementar Y = B'C'D' + AC' + AB' + ACD'
62  module TABLA_5(input wire A, B, C, D, output wire Y1);
63
64  wire r1, r2, r3, r4, r5, r6, r7;
65
66  not(r1, B);
67  not(r2, C);
68  not(r3, D);
69  and(r4, r1,r2,r3);
70  and(r5, A,r2);
71  and(r6, A,r1);
72  and(r7, A,C,r3);
73  or(Y1, r4,r5,r6,r7);
74
75  endmodule
76
```

Lab_4_tb.v

```
59  end
60
61  // TABLA_4 y TABLA_5
62  reg q1, q2, q3, q4;
63  wire led4, led5;
64
65  TABLA_4 G4 (q1,q2,q3,q4, led4);
66  TABLA_5 G5 (q1,q2,q3,q4, led5);
67
68  initial begin
69    #24
70    $display("\n");
71    $display("A B C D | Y Y1");
72    $display("--------|-----");
73    $monitor("%b %b %b %b | %b %b", q1,q2,q3,q4, led4, led5);
74
75        q1 = 0; q2 = 0; q3 = 0; q4 = 0;
76        #1 q1 = 0; q2 = 0; q3 = 0; q4 = 1;
77        #1 q1 = 0; q2 = 0; q3 = 1; q4 = 0;
78        #1 q1 = 0; q2 = 0; q3 = 1; q4 = 1;
79        #1 q1 = 0; q2 = 1; q3 = 0; q4 = 0;
80        #1 q1 = 0; q2 = 1; q3 = 0; q4 = 1;
81        #1 q1 = 0; q2 = 1; q3 = 1; q4 = 0;
82        #1 q1 = 0; q2 = 1; q3 = 1; q4 = 1;
83        #1 q1 = 1; q2 = 0; q3 = 0; q4 = 0;
84        #1 q1 = 1; q2 = 0; q3 = 0; q4 = 1;
85        #1 q1 = 1; q2 = 0; q3 = 1; q4 = 0;
86        #1 q1 = 1; q2 = 0; q3 = 1; q4 = 1;
87        #1 q1 = 1; q2 = 1; q3 = 0; q4 = 0;
88        #1 q1 = 1; q2 = 1; q3 = 0; q4 = 1;
89        #1 q1 = 1; q2 = 1; q3 = 1; q4 = 0;
90        #1 q1 = 1; q2 = 1; q3 = 1; q4 = 1;
91
92  end
```

Tabla No. 2.2

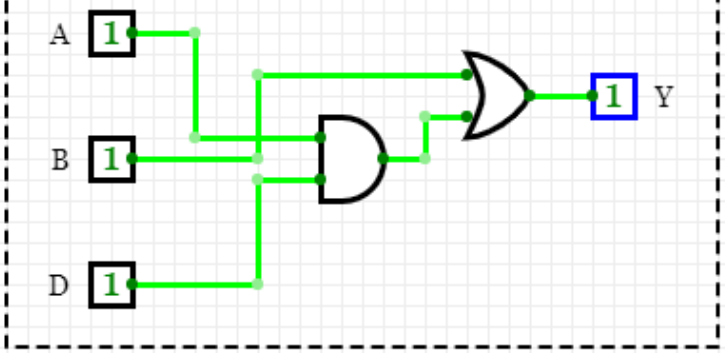


A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0

```
not(r2, C);
not(r3, D);
and(r4, r1,r2,r3);
and(r5, A,r2);
and(r6, A,r1);
and(r7, A,C,r3);
or(Y1, r4,r5,r6,r7);

endmodule


// Ecuación a implementar Y = B' + C
module TABLA_6(input wire A, B, C, output wire Y);

assign Y = (~B) | (C);

endmodule


// Ecuación a implementar Y = B + AD

module TABLA_7(input wire A, B, C, D, output wire Y);

assign Y = (B) | (A & D);
```

```
// TABLA_6
reg F1, F2, F3;
wire led6;

TABLA_6 G6(F1,F2,F3, led6);

initial begin
  #40
  $display("\n");
  $display("A B C | Y ");
  $display("------|---");
  $monitor("%b %b %b | %b", F1,F2,F3, led6);

  F1 = 0; F2 = 0; F3 = 0;
  #1 F1 = 0; F2 = 0; F3 = 1;
  #1 F1 = 0; F2 = 1; F3 = 0;
  #1 F1 = 0; F2 = 1; F3 = 1;
  #1 F1 = 1; F2 = 0; F3 = 0;
  #1 F1 = 1; F2 = 0; F3 = 1;
  #1 F1 = 1; F2 = 1; F3 = 0;
  #1 F1 = 1; F2 = 1; F3 = 1;

end
```

Tabla No. 2.3

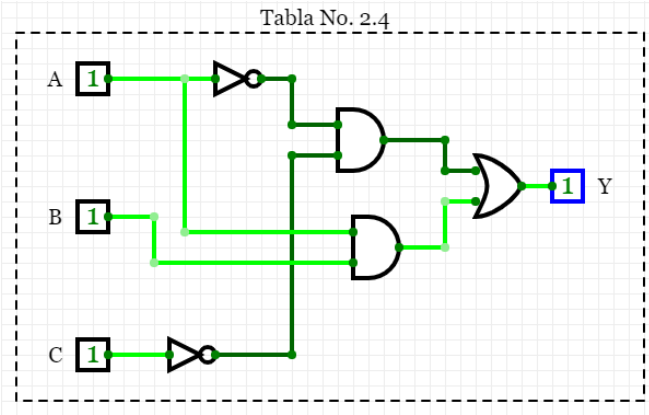


A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

```
// Ecuación a implementar Y = B + AD

module TABLA_7(input wire A, B, C, D, output wire Y);

assign Y = (B) | (A & D);

endmodule
```

```
// TABLA_7
reg d1, d2, d3, d4;
wire led7;

TABLA_7 G7(d1,d2,d3,d4, led7);

initial begin
  #47
  $display("\n");
  $display("A B C D | Y");
  $display("--------|----");
  $monitor("%b %b %b %b | %b", d1,d2,d3,d4, led7);

      d1 = 0; d2 = 0; d3 = 0; d4 = 0;
      #1 d1 = 0; d2 = 0; d3 = 0; d4 = 1;
      #1 d1 = 0; d2 = 0; d3 = 1; d4 = 0;
      #1 d1 = 0; d2 = 0; d3 = 1; d4 = 1;
      #1 d1 = 0; d2 = 1; d3 = 0; d4 = 0;
      #1 d1 = 0; d2 = 1; d3 = 0; d4 = 1;
      #1 d1 = 0; d2 = 1; d3 = 1; d4 = 0;
      #1 d1 = 0; d2 = 1; d3 = 1; d4 = 1;
      #1 d1 = 1; d2 = 0; d3 = 0; d4 = 0;
      #1 d1 = 1; d2 = 0; d3 = 0; d4 = 1;
      #1 d1 = 1; d2 = 0; d3 = 1; d4 = 0;
      #1 d1 = 1; d2 = 0; d3 = 1; d4 = 1;
      #1 d1 = 1; d2 = 1; d3 = 0; d4 = 0;
      #1 d1 = 1; d2 = 1; d3 = 0; d4 = 1;
      #1 d1 = 1; d2 = 1; d3 = 1; d4 = 0;
      #1 d1 = 1; d2 = 1; d3 = 1; d4 = 1;

end
```

Tabla No. 2.4

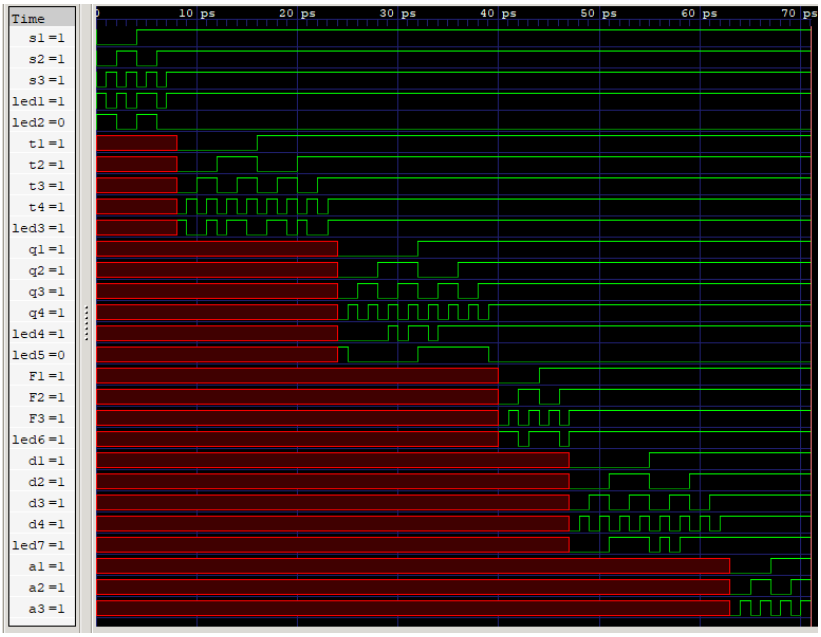


A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

```
// Ecuación a implementar Y = A'C' + AB
module TABLA_8(input wire A, B, C, output wire Y);

assign Y = (~A & ~C) | (A & B);

endmodule
```

```
//TABLA_8
reg a1, a2, a3;
wire led8;

TABLA_8 G8(a1,a2,a3, led8);

initial begin
  #63
  $display("\n");
  $display("A B C | Y");
  $display("------|----");
  $monitor("%b %b %b | %b", a1,a2,a3, led8);

  a1 = 0; a2 = 0; a3 = 0;
  #1 a1 = 0; a2 = 0; a3 = 1;
  #1 a1 = 0; a2 = 1; a3 = 0;
  #1 a1 = 0; a2 = 1; a3 = 1;
  #1 a1 = 1; a2 = 0; a3 = 0;
  #1 a1 = 1; a2 = 0; a3 = 1;
  #1 a1 = 1; a2 = 1; a3 = 0;
  #1 a1 = 1; a2 = 1; a3 = 1;

end

endmodule
```

DIAGRAMA DE TIMING



EJERCICIO 5

Problema 5

A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

donde A = Armado
B = sensor Mov
C = sensor VIP

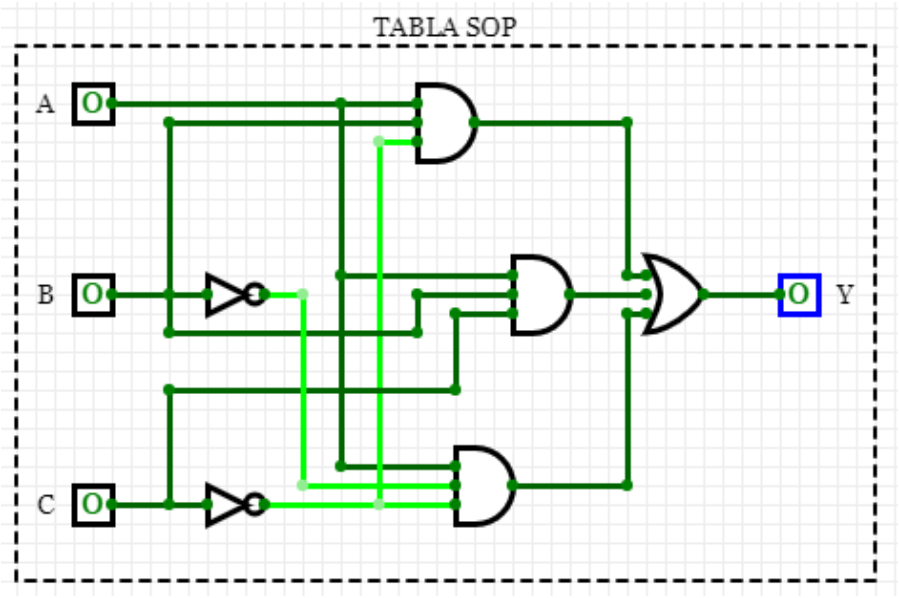
SOP
$y = (A \cdot B' \cdot C') + (A \cdot B \cdot C') + (A \cdot B \cdot C)$

POS
$y = (A + B + C) \cdot (A + B + C') \cdot (A + B' + C) \cdot (A + B' + C') \cdot (A' + B + C')$

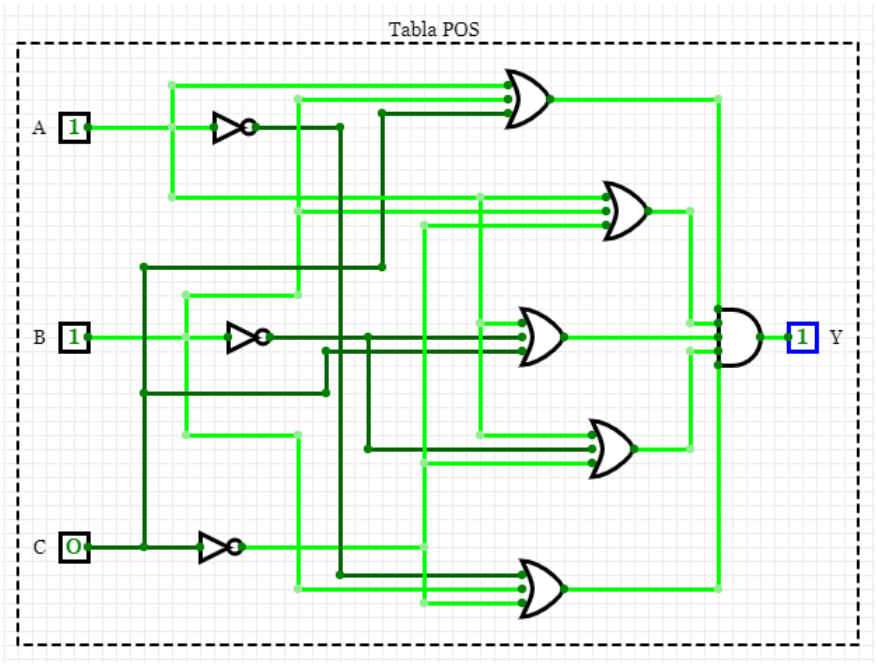
C \ AB	00	01	11	10
0	0	0	1	1
1	0	0	1	0

$y = A \cdot C' + AB$

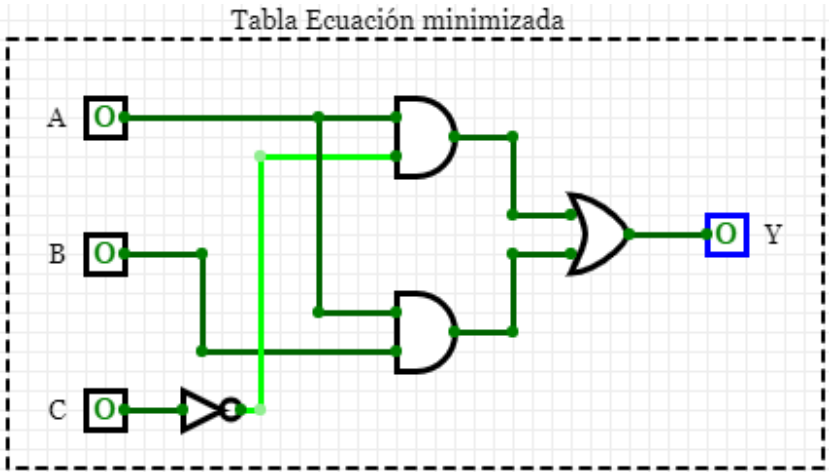
A	B	C	y
1	X	0	1
1	1	0	1




```
TABLA SOP


A B C | Y
------|---
VCD info: du
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1


A B C | Y
------|---
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
```

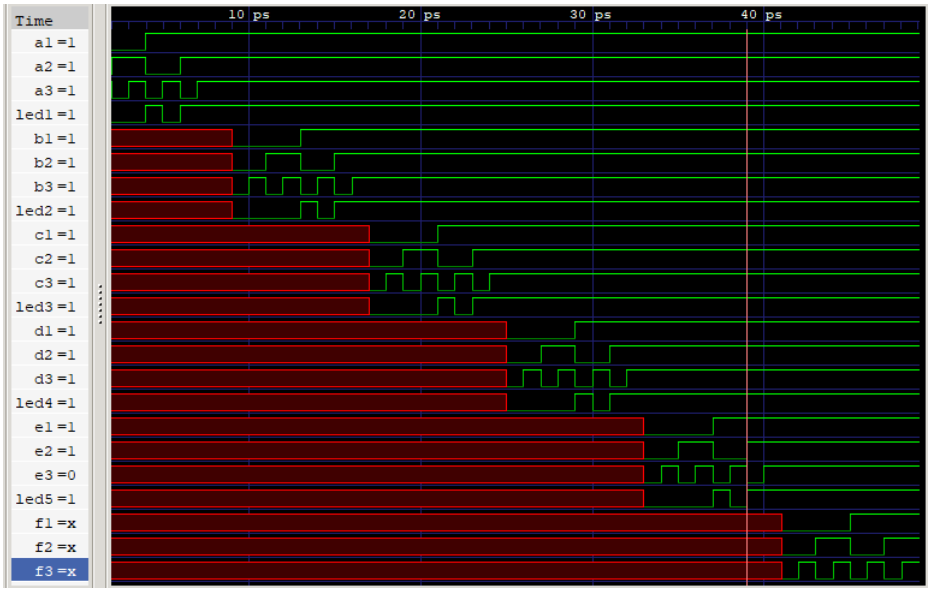



```
TABLA POS


A B C | Y
------|---
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1


A B C | Y
------|---
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
```



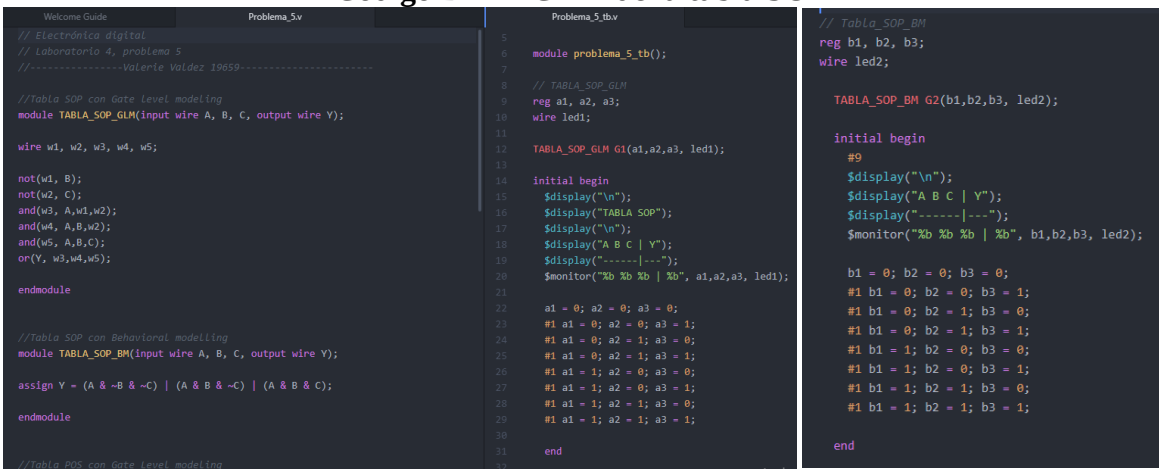

```
Tabla: ecuacion minimizada


A B C | Y
------|---
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1


A B C | Y
------|---
0 0 0 | 0
0 0 1 | 0
0 1 0 | 0
0 1 1 | 0
1 0 0 | 1
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
```

Diagrama de Timing



Códigos

Código BM Y GLM de la tabla SOP



```
// Electrónica digital
// Laboratorio 4, problema 5
//----------------Valerie Valdez 19659----------------------

//Tabla SOP con Gate level modeling
module TABLA_SOP_GLM(input wire A, B, C, output wire Y);

wire w1, w2, w3, w4, w5;

not(w1, B);
not(w2, C);
and(w3, A,w1,w2);
and(w4, A,B,w2);
and(w5, A,B,C);
or(Y, w3,w4,w5);

endmodule


//Tabla SOP con Behavioral modelling
module TABLA_SOP_BM(input wire A, B, C, output wire Y);

assign Y = (A & ~B & ~C) | (A & B & ~C) | (A & B & C);

endmodule
```

```
module problema_5_tb();

// TABLA_SOP_GLM
reg a1, a2, a3;
wire led1;

TABLA_SOP_GLM G1(a1,a2,a3, led1);

initial begin
  $display("\n");
  $display("TABLA SOP");
  $display("\n");
  $display("A B C | Y");
  $display("------|---");
  $monitor("%b %b %b | %b", a1,a2,a3, led1);

  a1 = 0; a2 = 0; a3 = 0;
  #1 a1 = 0; a2 = 0; a3 = 1;
  #1 a1 = 0; a2 = 1; a3 = 0;
  #1 a1 = 0; a2 = 1; a3 = 1;
  #1 a1 = 1; a2 = 0; a3 = 0;
  #1 a1 = 1; a2 = 0; a3 = 1;
  #1 a1 = 1; a2 = 1; a3 = 0;
  #1 a1 = 1; a2 = 1; a3 = 1;

  end
```

```
// Tabla_SOP_BM
reg b1, b2, b3;
wire led2;

  TABLA_SOP_BM G2(b1,b2,b3, led2);

  initial begin
    #9
    $display("\n");
    $display("A B C | Y");
    $display("------|---");
    $monitor("%b %b %b | %b", b1,b2,b3, led2);

    b1 = 0; b2 = 0; b3 = 0;
    #1 b1 = 0; b2 = 0; b3 = 1;
    #1 b1 = 0; b2 = 1; b3 = 0;
    #1 b1 = 0; b2 = 1; b3 = 1;
    #1 b1 = 1; b2 = 0; b3 = 0;
    #1 b1 = 1; b2 = 0; b3 = 1;
    #1 b1 = 1; b2 = 1; b3 = 0;
    #1 b1 = 1; b2 = 1; b3 = 1;

  end
```

Código BM y GLM de la tabla POS

```
endmodule


//Tabla SOP con Behavioral modelling
module TABLA_SOP_BM(input wire A, B, C, output wire Y);

assign Y = (A & ~B & ~C) | (A & B & ~C) | (A & B & C);

endmodule


//Tabla POS con Gate Level modeling
module TABLA_POS_GLM(input wire A,B,C, output wire Y);

wire q1, q2, q3, q4, q5, q6, q7, q8;

not(q1, A);
not(q2, B);
not(q3, C);
or(q4, A,B,C);
or(q5, A,B,q3);
or(q6, A,q2,C);
or(q7, A,q2,q3);
or(q8, q1,B,q3);
and(Y, q4,q5,q6,q7,q8);

endmodule
```

```
//Tabla Pos con Gate Level modeling
reg c1, c2, c3;
wire led3;

  TABLA_POS_GLM G3(c1,c2,c3, led3);

  initial begin
    #17
    $display("\n");
    $display("TABLA POS");
    $display("\n");
    $display("A B C | Y");
    $display("------|---");
    $monitor("%b %b %b | %b", c1,c2,c3, led3);

    c1 = 0; c2 = 0; c3 = 0;
    #1 c1 = 0; c2 = 0; c3 = 1;
    #1 c1 = 0; c2 = 1; c3 = 0;
    #1 c1 = 0; c2 = 1; c3 = 1;
    #1 c1 = 1; c2 = 0; c3 = 0;
    #1 c1 = 1; c2 = 0; c3 = 1;
    #1 c1 = 1; c2 = 1; c3 = 0;
    #1 c1 = 1; c2 = 1; c3 = 1;

  end
```

```
//Tabla Pos con Behavioral Modelling
reg d1, d2, d3;
wire led4;

  TABLA_POS_BM G4(d1,d2,d3, led4);

  initial begin
    #25
    $display("\n");
    $display("A B C | Y");
    $display("------|---");
    $monitor("%b %b %b | %b", d1,d2,d3, led4);

    d1 = 0; d2 = 0; d3 = 0;
    #1 d1 = 0; d2 = 0; d3 = 1;
    #1 d1 = 0; d2 = 1; d3 = 0;
    #1 d1 = 0; d2 = 1; d3 = 1;
    #1 d1 = 1; d2 = 0; d3 = 0;
    #1 d1 = 1; d2 = 0; d3 = 1;
    #1 d1 = 1; d2 = 1; d3 = 0;
    #1 d1 = 1; d2 = 1; d3 = 1;

    end
```

Códigos BM y GLM de la tabla con ecuación minimizada

```
//Tabla POS con Behavioral Modelling
module TABLA_POS_BM(input wire A,B,C, output wire Y);

assign Y = (A | B | C) & (A | B | ~C) & (A | ~B | C) & (A | ~B | ~C) & (~A | B

endmodule


// Tabla ecuación minimizada con Gate Level Modeling
module TABLA_MIN_GLM(input wire A,B,C, output wire Y);

wire s1, s2, s3;

not(s1, C);
and(s2, A,s1);
and(s3, A,B);
or(Y, s2,s3);

endmodule


// Tabla ecuación minimizada con Behavioral Modeling
module TABLA_MIN_BM(input wire A,B,C, output wire Y);

assign Y = (A & ~C) | (A & B);

endmodule
```

```
// Tabla ecuación minimizada con Gate Level modelin
reg e1, e2, e3;
wire led5;

  TABLA_MIN_GLM G5(e1,e2,e3, led5);

  initial begin
    #33
    $display("\n");
    $display("Tabla: ecuacion minimizada");
    $display("\n");
    $display("A B C | Y");
    $display("------|---");
    $monitor("%b %b %b | %b", e1,e2,e3, led5);

    e1 = 0; e2 = 0; e3 = 0;
    #1 e1 = 0; e2 = 0; e3 = 1;
    #1 e1 = 0; e2 = 1; e3 = 0;
    #1 e1 = 0; e2 = 1; e3 = 1;
    #1 e1 = 1; e2 = 0; e3 = 0;
    #1 e1 = 1; e2 = 0; e3 = 1;
    #1 e1 = 1; e2 = 1; e3 = 0;
    #1 e1 = 1; e2 = 1; e3 = 1;

    end
```

```
// Tabla ecuación minimizada con Behavioral Modelin
reg f1, f2, f3;
wire led6;

  TABLA_MIN_BM G6(f1,f2,f3, led6);

  initial begin
    #41
    $display("\n");
    $display("A B C | Y");
    $display("------|---");
    $monitor("%b %b %b | %b", f1,f2,f3, led6);

    f1 = 0; f2 = 0; f3 = 0;
    #1 f1 = 0; f2 = 0; f3 = 1;
    #1 f1 = 0; f2 = 1; f3 = 0;
    #1 f1 = 0; f2 = 1; f3 = 1;
    #1 f1 = 1; f2 = 0; f3 = 0;
    #1 f1 = 1; f2 = 0; f3 = 1;
    #1 f1 = 1; f2 = 1; f3 = 0;
    #1 f1 = 1; f2 = 1; f3 = 1;

    end

    initial
      #49 $finish;

      initial begin
        $dumpfile("Problema_5_tb.vcd");
        $dumpvars(0, problema_5_tb);
        end

endmodule
```