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Universidad del Valle de Guatemala

Carné: 19659
Sección: 21

Electrónica digital
Laboratorio #4

Primera parte

Ejercicio 01

	A	B	C	y
	0	0	0	1
*	0	0	1	0
	0	1	0	1
*	0	1	1	0
	1	0	0	1
	1	0	1	1
*	1	1	0	0
	1	1	1	1

SOP

$y = A' \cdot B' \cdot C' + A'BC' + AB'C' + AB'C + ABC$

POS

$y = (A + B + C') \cdot (A + B' + C') \cdot (A' + B' + C)$

	A	B	C	y
*	0	0	0	0
	0	0	1	1
*	0	1	0	0
*	0	1	1	0
*	1	0	0	0
*	1	0	1	0
	1	1	0	1
	1	1	1	1

SOP

$y = (A' \cdot B' \cdot C) + (A \cdot B \cdot C') + (ABC)$

POS

$y = (A + B + C) \cdot (A + B' + C) \cdot (A + B' + C') \cdot (A' + B + C) \cdot (A' + B' + C')$

A	B	C	D	y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
*0	1	0	0	0
*0	1	0	1	0
*0	1	1	0	0
*0	1	1	1	0
1	0	0	0	1
*1	0	0	1	0
1	0	1	0	1
*1	0	1	1	0
*1	1	0	0	0
*1	1	0	1	0
1	1	1	0	1
*1	1	1	1	0

SOP

$y = (A' \cdot B' \cdot C' \cdot D') + (A' B' C' \cdot D) + (A' \cdot B' C\ D') + (A' \cdot B' \cdot C \cdot D) +$
$(A \cdot B' \cdot C' \cdot D') + (A \cdot B' \cdot C \cdot D') + (A \cdot B \cdot C \cdot D')$

POS

$y = (A+B'+C+D) \cdot (A+B'+C+D') \cdot (A+B'+C'+D) \cdot (A+B'+C'+D')$
$(A'+B+C+D') \cdot (A'+B+C'+D') \cdot (A'+B'+C+D) \cdot (A'+B'+C+D') \cdot (A'+B'+C'+D)$

A	B	C	D	y
0	0	0	0	1
*0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
*0	1	0	0	0
*0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
*1	0	0	1	0
1	0	1	0	1
*1	0	1	1	0
*1	1	0	0	0
*1	1	0	1	0
*1	1	1	0	0
*1	1	1	1	0

SOP

$y = (A' \cdot B' \cdot C' \cdot D') + (A' \cdot B' \cdot C \cdot D') + (A' \cdot B' \cdot C \cdot D) +$
$(A' \cdot B \cdot C \cdot D') + (A' \cdot B \cdot C \cdot D) + (A \cdot B' \cdot C' \cdot D')$
$(A \cdot B' \cdot C \cdot D')$

POS

$y = (A+B+C+D') \cdot (A+B'+C+D) \cdot (A \cdot B' \cdot C \cdot D')$
$(A'+B+C+D') \cdot (A'+B+C'+D') \cdot (A'+B'+C+D')$
$(A'+B'+C+D') \cdot (A'+B'+C'+D) \cdot (A'+B'+C'+D')$

Segunda parte

Tabla No. 3, SOP

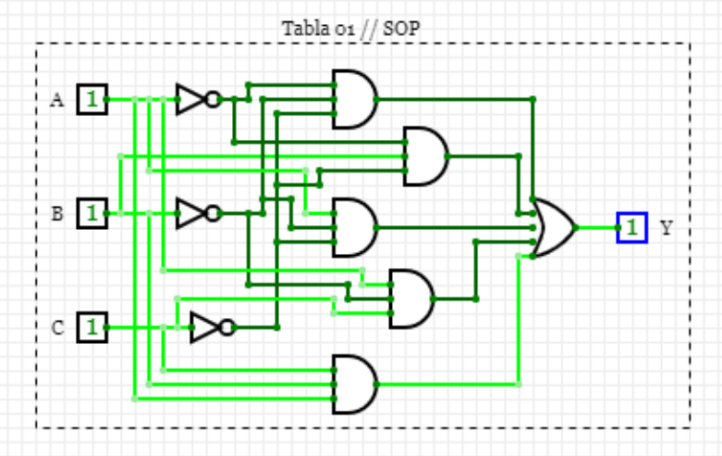


Tabla No. 2, SOP

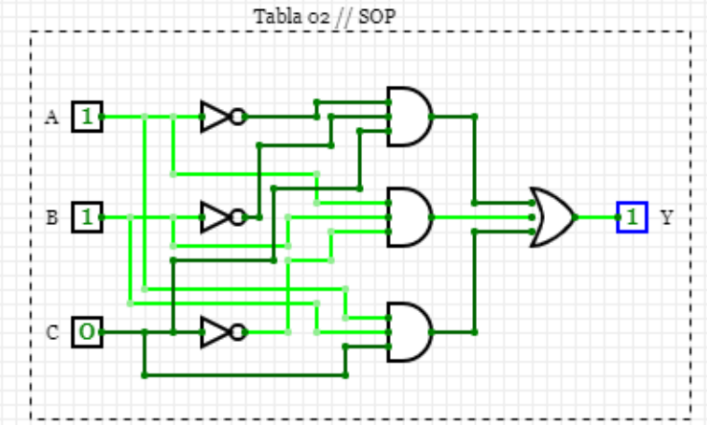


Tabla No. 3, POS

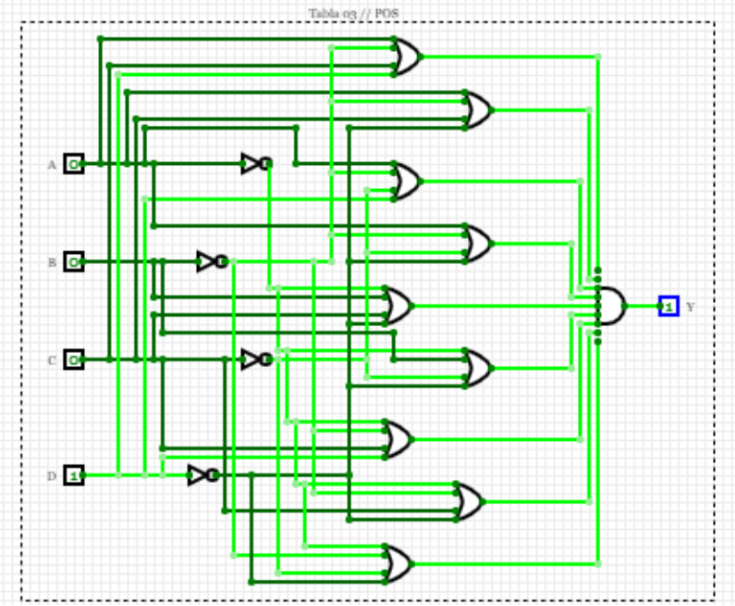
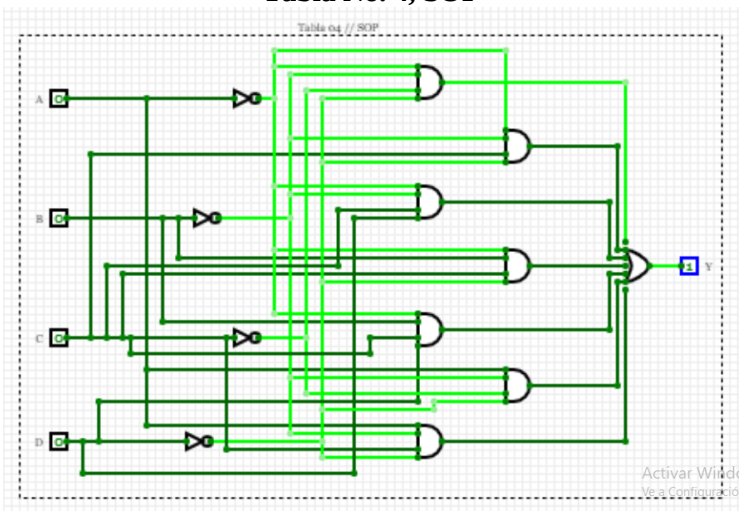


Tabla No. 4, SOP



Tercera parte

01 Tabla POS

```
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C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\01_TABLA_
POS>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 01_TABLA_POS_tb.out -D VCD_OUTPUT=01_TABLA_POS_tb C:/Users/personal/.apio\package
s\toolchain-yosys\share\yosys/ice40/cells_sim.v 01_TABLA_POS.v 01_TABLA_POS_tb.v
vvp 01_TABLA_POS_tb.out
A B C | Y
----------
VCD info: dumpfile 01_TABLA_POS_tb.vcd opened for output.
0 0 0 | 1
0 0 1 | 0
0 1 0 | 1
0 1 1 | 0
1 0 0 | 1
1 0 1 | 1
1 1 0 | 0
1 1 1 | 1
gtkwave 01_TABLA_POS_tb.vcd 01_TABLA_POS_tb.gtkw
```

01 Tabla SOP

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\01_
TABLA_SOP>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 01_TABLA_SOP_tb.out -D VCD_OUTPUT=01_TABLA_SOP_tb C:/Users/personal/.apio\p
ackages\toolchain-yosys\share\yosys/ice40/cells_sim.v 01_TABLA_SOP.v 01_TABLA_SOP_tb.v
vvp 01_TABLA_SOP_tb.out
A B C | Y
----------
VCD info: dumpfile 01_TABLA_SOP_tb.vcd opened for output.
0 0 0 | 1
0 0 1 | 0
0 1 0 | 1
0 1 1 | 0
1 0 0 | 1
1 0 1 | 1
1 1 0 | 0
1 1 1 | 1
gtkwave 01_TABLA_SOP_tb.vcd 01_TABLA_SOP_tb.gtkw
```

02 Tabla POS

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\02_TABLA
_POS>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 02_TABLA_POS_tb.out -D VCD_OUTPUT=02_TABLA_POS_tb C:/Users/personal/.apio\packag
es\toolchain-yosys\share\yosys/ice40/cells_sim.v 02_TABLA_POS.v 02_TABLA_POS_tb.v
vvp 02_TABLA_POS_tb.out
A B C | Y
----------
VCD info: dumpfile 02_TABLA_POS_tb.vcd opened for output.
0 0 0 | 0
0 0 1 | 1
0 1 0 | 0
0 1 1 | 0
1 0 0 | 0
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
gtkwave 02_TABLA_POS_tb.vcd 02_TABLA_POS_tb.gtkw
```

02 Tabla SOP

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\02_TABLA
_SOP>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 02_TABLA_SOP_tb.out -D VCD_OUTPUT=02_TABLA_SOP_tb C:/Users/personal/.apio\packag
es\toolchain-yosys\share\yosys/ice40/cells_sim.v 02_TABLA_SOP.v 02_TABLA_SOP_tb.v
vvp 02_TABLA_SOP_tb.out
A B C | Y
----------
VCD info: dumpfile 02_TABLA_SOP_tb.vcd opened for output.
0 0 0 | 0
0 0 1 | 1
0 1 0 | 0
0 1 1 | 0
1 0 0 | 0
1 0 1 | 0
1 1 0 | 1
1 1 1 | 1
gtkwave 02_TABLA_SOP_tb.vcd 02_TABLA_SOP_tb.gtkw
```

03 Tabla POS

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\03_TABLA_POS>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 03_TABLA_POS_tb.out -D VCD_OUTPUT=03_TABLA_POS_tb C:/Users/personal/.apio\packages\toolchain-yosys\share\yos
ys/ice40/cells_sim.v 03_TABLA_POS.v 03_TABLA_POS_tb.v
vvp 03_TABLA_POS_tb.out
A B C D | Y
----------
VCD info: dumpfile 03_TABLA_POS_tb.vcd opened for output.
0 0 0 0 | 1
0 0 0 1 | 1
0 0 1 0 | 1
0 0 1 1 | 1
0 1 0 0 | 0
0 1 0 1 | 0
0 1 1 0 | 0
0 1 1 1 | 0
1 0 0 0 | 1
1 0 0 1 | 0
1 0 1 0 | 1
1 0 1 1 | 0
1 1 0 0 | 0
1 1 0 1 | 0
1 1 1 0 | 1
1 1 1 1 | 0
gtkwave 03_TABLA_POS_tb.vcd 03_TABLA_POS_tb.gtkw
```

03 Tabla SOP

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\03_TABLA_SOP>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 03_TABLA_SOP_tb.out -D VCD_OUTPUT=03_TABLA_SOP_tb C:/Users/personal/.apio\packages\toolchain-y
osys\share\yosys/ice40/cells_sim.v 03_TABLA_SOP.v 03_TABLA_SOP_tb.v
vvp 03_TABLA_SOP_tb.out
A B C D | Y
----------
VCD info: dumpfile 03_TABLA_SOP_tb.vcd opened for output.
0 0 0 0 | 1
0 0 0 1 | 1
0 0 1 0 | 1
0 0 1 1 | 1
0 1 0 0 | 0
0 1 0 1 | 0
0 1 1 0 | 0
0 1 1 1 | 0
1 0 0 0 | 1
1 0 0 1 | 0
1 0 1 0 | 1
1 0 1 1 | 0
1 1 0 0 | 0
1 1 0 1 | 0
1 1 1 0 | 1
1 1 1 1 | 0
gtkwave 03_TABLA_SOP_tb.vcd 03_TABLA_SOP_tb.gtkw
```

04 Tabla POS

```
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C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\04_TABLA_POS>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 04_TABLA_POS_tb.out -D VCD_OUTPUT=04_TABLA_POS_tb C:/Users/personal/.apio\packages\toolchain-yosys
\share\yosys/ice40/cells_sim.v 04_TABLA_POS.v 04_TABLA_POS_tb.v
vvp 04_TABLA_POS_tb.out
A B C D | Y
----------
VCD info: dumpfile 04_TABLA_POS_tb.vcd opened for output.
0 0 0 0 | 1
0 0 0 1 | 0
0 0 1 0 | 1
0 0 1 1 | 1
0 1 0 0 | 0
0 1 0 1 | 0
0 1 1 0 | 1
0 1 1 1 | 1
1 0 0 0 | 1
1 0 0 1 | 0
1 0 1 0 | 1
1 0 1 1 | 0
1 1 0 0 | 0
1 1 0 1 | 0
1 1 1 0 | 0
1 1 1 1 | 0
gtkwave 04_TABLA_POS_tb.vcd 04_TABLA_POS_tb.gtkw
```

04 Tabla SOP

```
C:\Users\personal\Documents\Valerie Valdez\Electronica digital\Github\Lab_digital_3\04_TABLA_SOP>apio sim

---> WARNING: no PCF file found (.pcf)

iverilog -o 04_TABLA_SOP_tb.out -D VCD_OUTPUT=04_TABLA_SOP_tb C:/Users/personal/.apio\packages\toolchain-yosy
s\share\yosys/ice40/cells_sim.v 04_TABLA_SOP.v 04_TABLA_SOP_tb.v
vvp 04_TABLA_SOP_tb.out
A B C D | Y
----------
VCD info: dumpfile 04_TABLA_SOP_tb.vcd opened for output.
0 0 0 0 | 1
0 0 0 1 | 0
0 0 1 0 | 1
0 0 1 1 | 1
0 1 0 0 | 0
0 1 0 1 | 0
0 1 1 0 | 1
0 1 1 1 | 1
1 0 0 0 | 1
1 0 0 1 | 0
1 0 1 0 | 1
1 0 1 1 | 0
1 1 0 0 | 0
1 1 0 1 | 0
1 1 1 0 | 0
1 1 1 1 | 0
gtkwave 04_TABLA_SOP_tb.vcd 04_TABLA_SOP_tb.gtkw
```

Link: https://github.com/valeelorraine/Lab_digital_3

Cuarta parte