keypad_controler Project Status			
Project File:	Keyboard_controller.xise	**Parser Errors:**	No Errors
Module Name:	keypad_controler	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-4ft256	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	24 Warnings (24 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	179	3,840	4%	
Number used as Flip Flops	175			
Number used as Latches	4			
Number of 4 input LUTs	159	3,840	4%	
Number of occupied Slices	158	1,920	8%	
Number of Slices containing only related logic	158	158	100%	
Number of Slices containing unrelated logic	0	158	0%	
Total Number of 4 input LUTs	266	3,840	6%	
Number used as logic	159			
Number used as a route-thru	107			
Number of bonded IOBs	21	173	12%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.65			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	ven. 8. mars 17:45:08 2019	0	4 Warnings (4 new)	5 Infos (5 new)
Translation Report	Current	ven. 8. mars 17:45:25 2019	0	0	0
Map Report	Current	ven. 8. mars 17:45:30 2019	0	5 Warnings (5 new)	2 Infos (2 new)
Place and Route Report	Current	ven. 8. mars 17:45:37 2019	0	10 Warnings (10 new)	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	ven. 8. mars 17:45:40 2019	0	0	6 Infos (6 new)
Bitgen Report	Current	ven. 8. mars 17:45:45 2019	0	5 Warnings (5 new)	1 Info (1 new)

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	ven. 8. mars 17:43:26 2019
WebTalk Report	Current	ven. 8. mars 17:45:45 2019
WebTalk Log File	Current	ven. 8. mars 17:45:49 2019

Date Generated: 03/16/2019 - 16:43:59