```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.11 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.11 secs

--> Reading design: tx_uart.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "tx_uart.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "tx_uart"
Output Format                      : NGC
Target Device                      : xc3s200-4-ft256

---- Source Options
Top Module Name                    : tx_uart
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
```

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ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Compilation                             *
=========================================================================
Compiling vhdl file "F:/Mes Documents/GitHub/-ESE-VHDL-UART/UART/tx_uart.vhd" in Library
work.
Entity <tx_uart> compiled.
Entity <tx_uart> (Architecture <behavioral>) compiled.

=========================================================================
*                       Design Hierarchy Analysis                       *
=========================================================================
Analyzing hierarchy for entity <tx_uart> in library <work> (architecture <behavioral>).


=========================================================================
*                             HDL Analysis                              *
=========================================================================
Analyzing Entity <tx_uart> in library <work> (Architecture <behavioral>).
WARNING:Xst:819 - "F:/Mes Documents/GitHub/-ESE-VHDL-UART/UART/tx_uart.vhd" line 69: One
```

```
or more signals are missing in the process sensitivity list. To enable synthesis of
FPGA/CPLD hardware, XST will assume that all necessary signals are present in the
sensitivity list. Please note that the result of the synthesis may differ from the initial
design specification. The missing signals are:
   <tx_start>
Entity <tx_uart> analyzed. Unit <tx_uart> generated.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <tx_uart>.
    Related source file is "F:/Mes Documents/GitHub/-ESE-VHDL-UART/UART/tx_uart.vhd".
    Found finite state machine <FSM_0> for signal <current_state>.
    -----------------------------------------------------------------------
    | States             | 4                                              |
    | Transitions        | 12                                             |
    | Inputs             | 4                                              |
    | Outputs            | 4                                              |
    | Clock              | clk                       (rising_edge)        |
    | Reset              | rst                       (positive)           |
    | Reset type         | asynchronous                                   |
    | Reset State        | idle                                           |
    | Power Up State     | idle                                           |
    | Encoding           | automatic                                      |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
    Found 4-bit register for signal <n_reg>.
    Found 4-bit adder for signal <n_reg$addsub0000> created at line 114.
    Found 4-bit adder for signal <s$add0000> created at line 95.
    Found 4-bit register for signal <s_reg>.
    Summary:
        inferred   1 Finite State Machine(s).
        inferred   8 D-type flip-flop(s).
        inferred   2 Adder/Subtractor(s).
Unit <tx_uart> synthesized.


=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 2
 4-bit adder                                          : 2
# Registers                                            : 2
 4-bit register                                       : 2

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================

Analyzing FSM <FSM_0> for best encoding.
Optimizing FSM <current_state/FSM> on signal <current_state[1:2]> with gray encoding.
-------------------
 State | Encoding
-------------------
```

```
 idle  | 00
 start | 01
 data  | 11
 stop  | 10
-------------------

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# FSMs                                                 : 1
# Adders/Subtractors                                   : 2
 4-bit adder                                          : 2
# Registers                                            : 8
 Flip-Flops                                           : 8

=========================================================================

=========================================================================
*                            Low Level Synthesis                        *
=========================================================================

Optimizing unit <tx_uart> ...
WARNING:Xst:1293 - FF/Latch <n_reg_3> has a constant value of 0 in block <tx_uart>. This
FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1293 - FF/Latch <n_reg_3> has a constant value of 0 in block <tx_uart>. This
FF/Latch will be trimmed during the optimization process.

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block tx_uart, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 9
 Flip-Flops                                           : 9

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : tx_uart.ngr
Top Level Output File Name         : tx_uart
Output Format                      : NGC
```

```
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 14

Cell Usage :
# BELS                             : 30
#      LUT2                        : 2
#      LUT2_L                      : 2
#      LUT3                        : 5
#      LUT3_L                      : 1
#      LUT4                        : 15
#      LUT4_L                      : 2
#      MUXF5                       : 3
# FlipFlops/Latches                : 9
#      FDC                         : 9
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 13
#      IBUF                        : 11
#      OBUF                        : 2
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s200ft256-4

 Number of Slices:                       14  out of   1920     0%
 Number of Slice Flip Flops:              9  out of   3840     0%
 Number of 4 input LUTs:                 27  out of   3840     0%
 Number of IOs:                          14
 Number of bonded IOBs:                  14  out of    173     8%
 Number of GCLKs:                         1  out of      8    12%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 9     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
```

```
---------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst                                | IBUF                   | 9     |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 5.546ns (Maximum Frequency: 180.310MHz)
   Minimum input arrival time before clock: 5.831ns
   Maximum output required time after clock: 11.086ns
   Maximum combinational path delay: 10.593ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.546ns (frequency: 180.310MHz)
  Total number of paths / destination ports: 67 / 9
-------------------------------------------------------------------------
Delay:               5.546ns (Levels of Logic = 3)
  Source:            s_reg_2 (FF)
  Destination:       current_state_FSM_FFd2 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: s_reg_2 to current_state_FSM_FFd2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              2   0.720   1.072  s_reg_2 (s_reg_2)
     LUT4:I1->O            6   0.551   1.071  s_reg_mux0000<0>21 (N7)
     LUT3:I2->O            1   0.551   0.827  current_state_FSM_FFd2-In6
(current_state_FSM_FFd2-In6)
     LUT4:I3->O            1   0.551   0.000  current_state_FSM_FFd2-In38
(current_state_FSM_FFd2-In)
     FDC:D                 0.203          current_state_FSM_FFd2
    ----------------------------------------
    Total                  5.546ns (2.576ns logic, 2.970ns route)
                                   (46.4% logic, 53.6% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 10 / 9
-------------------------------------------------------------------------
Offset:              5.831ns (Levels of Logic = 4)
  Source:            s_tick (PAD)
  Destination:       current_state_FSM_FFd2 (FF)
  Destination Clock: clk rising

  Data Path: s_tick to current_state_FSM_FFd2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   0.821   1.256  s_tick_IBUF (s_tick_IBUF)
     LUT4:I0->O            6   0.551   1.071  s_reg_mux0000<0>21 (N7)
```

```
     LUT3:I2->O            1   0.551   0.827  current_state_FSM_FFd2-In6
(current_state_FSM_FFd2-In6)
     LUT4:I3->O            1   0.551   0.000  current_state_FSM_FFd2-In38
(current_state_FSM_FFd2-In)
     FDC:D                     0.203          current_state_FSM_FFd2
    ----------------------------------------
    Total                      5.831ns (2.677ns logic, 3.154ns route)
                                       (45.9% logic, 54.1% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 14 / 2
-------------------------------------------------------------------------
Offset:              11.086ns (Levels of Logic = 4)
  Source:            n_reg_0 (FF)
  Destination:       tx (PAD)
  Source Clock:      clk rising

  Data Path: n_reg_0 to tx
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              9   0.720   1.463  n_reg_0 (n_reg_0)
     LUT4:I0->O            1   0.551   0.000  tx44_F (N21)
     MUXF5:I0->O           1   0.360   0.996  tx44 (tx44)
     LUT4:I1->O            1   0.551   0.801  tx140 (tx_OBUF)
     OBUF:I->O                 5.644          tx_OBUF (tx)
    ----------------------------------------
    Total                     11.086ns (7.826ns logic, 3.260ns route)
                                       (70.6% logic, 29.4% route)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
Delay:               10.593ns (Levels of Logic = 5)
  Source:            din<5> (PAD)
  Destination:       tx (PAD)

  Data Path: din<5> to tx
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   0.821   0.869  din_5_IBUF (din_5_IBUF)
     LUT4:I2->O            1   0.551   0.000  tx44_F (N21)
     MUXF5:I0->O           1   0.360   0.996  tx44 (tx44)
     LUT4:I1->O            1   0.551   0.801  tx140 (tx_OBUF)
     OBUF:I->O                 5.644          tx_OBUF (tx)
    ----------------------------------------
    Total                     10.593ns (7.927ns logic, 2.666ns route)
                                       (74.8% logic, 25.2% route)

=========================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.73 secs

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Total memory usage is 4550260 kilobytes
```

```
Number of errors   :    0 (   0 filtered)
Number of warnings :    3 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```