| rx_uart Project Status (03/20/2019 - 17:25:10) | | | |
|---|---|---|---|
| **Project File:** | UART.xise | **Parser Errors:** | No Errors |
| **Module Name:** | rx_uart | **Implementation State:** | Synthesized |
| **Target Device:** | xc3s200-4ft256 | • **Errors:** | No Errors |
| **Product Version:** | ISE 14.7 | • **Warnings:** | 15 Warnings (15 new) |
| **Design Goal:** | Balanced | • **Routing Results:** | |
| **Design Strategy:** | Xilinx Default (unlocked) | • **Timing Constraints:** | |
| **Environment:** | System Settings | • **Final Timing Score:** | |

| Device Utilization Summary (estimated values) [-] | | | |
|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** |
| Number of Slices | 33 | 1920 | 1% |
| Number of Slice Flip Flops | 23 | 3840 | 0% |
| Number of 4 input LUTs | 60 | 3840 | 1% |
| Number of bonded IOBs | 13 | 173 | 7% |
| Number of GCLKs | 1 | 8 | 12% |

| Detailed Reports [-] | | | | | |
|---|---|---|---|---|---|
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** |
| Synthesis Report | Current | dim. 7. avr. 16:45:22 2019 | 0 | 15 Warnings (15 new) | 5 Infos (5 new) |
| Translation Report | | | | | |
| Map Report | | | | | |
| Place and Route Report | | | | | |
| Power Report | | | | | |
| Post-PAR Static Timing Report | | | | | |
| Bitgen Report | | | | | |

| Secondary Reports [-] | | |
|---|---|---|
| **Report Name** | **Status** | **Generated** |
| ISIM Simulator Log | Current | dim. 7. avr. 16:46:40 2019 |
| WebTalk Report | Out of Date | mer. 27. mars 15:14:19 2019 |
| WebTalk Log File | Out of Date | mer. 27. mars 15:14:24 2019 |

**Date Generated:** 04/07/2019 - 16:53:01