UART Project Status (04/07/2019 - 16:45:24)			
Project File:	UART.xise	**Parser Errors:**	No Errors
Module Name:	UART	**Implementation State:**	Synthesized
Target Device:	xc3s200-4ft256	• **Errors:**	
Product Version:	ISE 14.7	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	14	1920	0%
Number of Slice Flip Flops	9	3840	0%
Number of 4 input LUTs	27	3840	0%
Number of bonded IOBs	14	173	8%
Number of GCLKs	1	8	12%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	dim. 7. avr. 17:02:29 2019			
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	dim. 7. avr. 17:55:09 2019
WebTalk Report	Out of Date	mer. 27. mars 15:14:19 2019
WebTalk Log File	Out of Date	mer. 27. mars 15:14:24 2019

Date Generated: 04/07/2019 - 18:03:21