**APPENDIX ON THE WEBSITE TO WHICH THE PAPER IS REFERRED**

**P1**  Block diagram of a microcomputer system

**P2** Block diagram of memory organization in a computer

**P3** Presentation of the organization of input and output units with connection to the regulated process

**P4** Presentation of the computer interrupt system organization

**P5** The input control delay is given in Figure P5

**P6** The schematic of the servo amplifier

CLOCK

8824

CONTROLER

8828

DISPLAY

D/A

D/A

8255 # 1

8255 # 2

8255 # 3

A, B

C

B

A

A, B

C

CPU

8080

STSTB

01

2,5 ms

MM1

50 ms

MM2

614,4 ms

LENGTH SELECTOOR

I1

I2

I3

STOP

GI

D1

D2

D3

∅1

∅2

WAIT

READY

RESET

SYNC

D0-D7

HLDA

DB/N

WR

INTE

INT.

A0-A15

DECODER

8205

4

A8A9A10

+5V

+12V

–5V

GND

A0A1A11

A0A1A13

A0A1A12

A0-A7

A0-A7

4×811

4×8702

RIN

MEMR

MEMR

MEMW

OD

C5

RAM

256 byte

EPROM

1 k byte

ADRESS BUS

DATA BUS

CONTROL BUS

IO/R

I/OW

I/OW

I/OR

I/OR

I/OW

Appendix P1

A0-A7

A0-A7

D0-D3

D4-D7

DECODER

8205

A8, A9, A10

RAM

811

RAM

811

EPROM

8702

EPROM

8702

A0-A7

A0-A7

CS

CS

CS

CS

A0-A7

A0-A7

EPROM

8702

EPROM

8702

MEMR

MEMW

ADRESS BUS

DATA BUS

APPENDIX P2

CLAMPING THE JAWS

LOWERING THE CUTTING TOOL

LIFTING THE CUTTING TOOL

IMPULSE GENERATOR

LOWER POSITION DETECTOR

UPPER POSITION DETECTOR

REST POSITION DETECTOR

DECEELERATION DETECTOR

STOP

LENGTH SELECTOR

D/A

D/A

TO THE MODEL

TO THE SERVO AMPL.

B

C

A

#1

8255

#2

A, B

C

8255

01

2.5 ms

#3

A, B

C

8255

DISPLAY

MM1

MM2

50 ms

614,4 ms

Appendix P3

DATA BUS

∅2

CLK

Vcc

1k

1k

INTE

INT

INT

INT. REQUESTS

R0

R1

8214

STB

8214

A0–A2

D0–D2

D6–D7

ETLG

D0–D7

GND

GND

ECS

ELR

CLR

DS1

INTA

10k

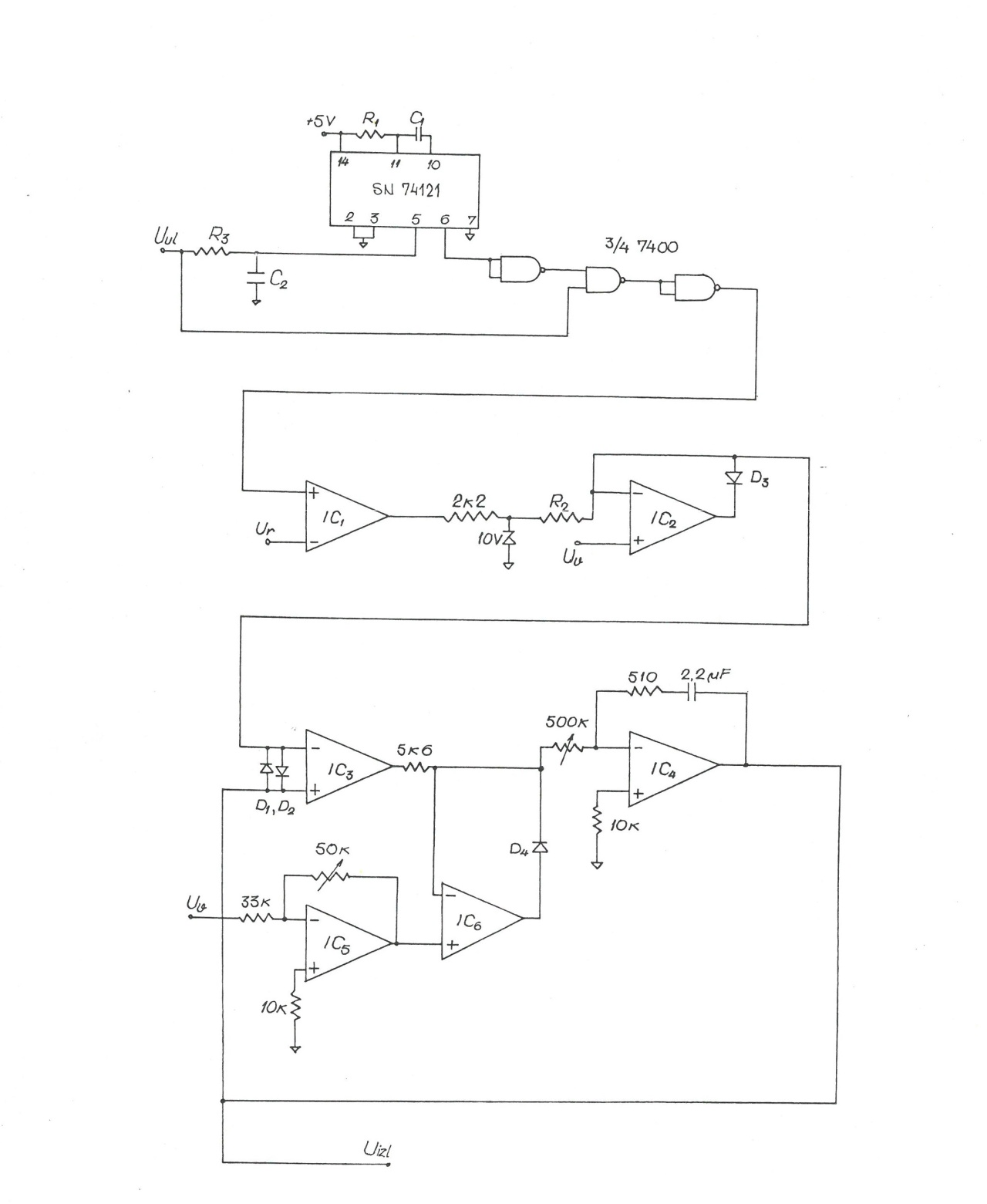
INT

ACCORD.8080

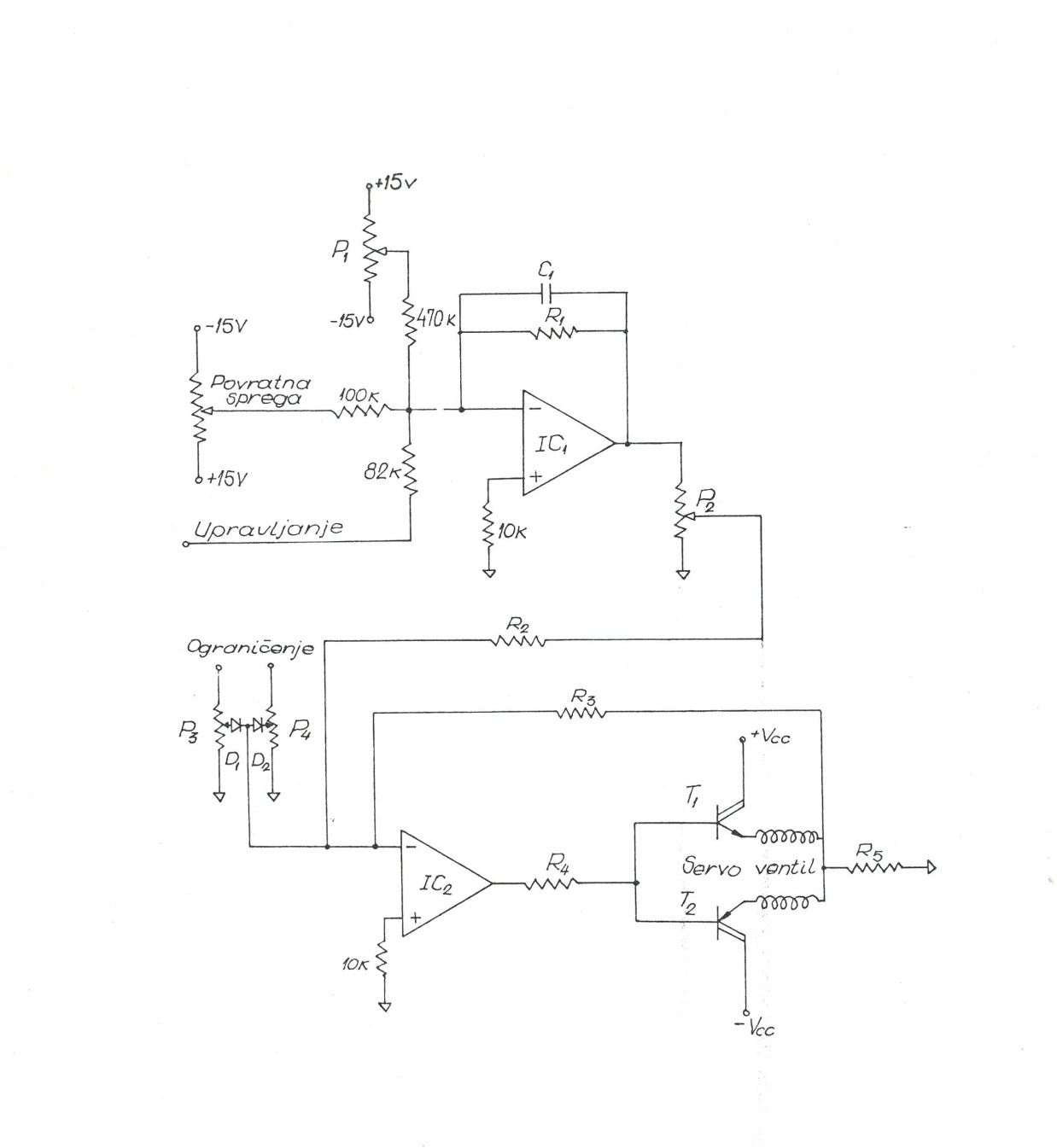
DS2

MD

Apendix P4

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Appendix P5



Appendix P6