

LTC 1060

Universal Dual Filter **Building Block**

FERTURES

- Guaranteed Filter Specification for ±2.37V and
- Operates Up to 30kHz
- Low Power and 88dB Dynamic Range at ±2.5V Supply
- Center Frequency Q Product Up to 1.6MHz
- Guaranteed Offset Voltages
- Guaranteed Clock-to-Center Frequency Accuracy Over emperature:
- 0.8% for LTC1060 0.3% for LTC1060A
- Guaranteed Q Accuracy Over Temperature
- Low Temperature Coefficient of Q and Center
- Low Crosstalk, 70dB
- Clock Inputs TTL and CMOS Compatible

APPLICATIONS

- Single 5V Supply Medium Frequency Filters
- Very High Q and High Dynamic Range Bandpass, Notch Filters
- Tracking Filters
- Telecom Filters

DESCRIPTION

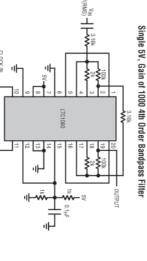
to 4th order full biquadratic functions can be achieved by external clock or by an external clock and resistor ratio. Up lowpass, bandpass, highpass notch and allpass. The can be formed. cascading the two filter blocks. Any of the classical filter center frequency of these functions can be tuned by an can produce various 2nd order filter functions such as capacitor filters. Each filter, together with 2 to 5 resistors, The LTC®1060 consists of two high performance, switched configurations (like Butterworth, Chebyshev, Bessel, Cauer)

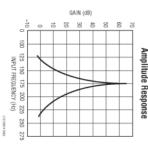
very high Q values can also be obtained ±5V supply, the frequency range extends to 30kHz and and can operate with center frequencies up to 10kHz. With (i.e. single 5V supply), the filter typically consumes 12mW from ±2.37V to ±8V. When used with low supply The LTC1060 operates with either a single or dual supply

center frequency Q product and excellent temperature Because of this, low offsets, high dynamic range, high Technology's enhanced LTCMOS™ silicon gate process. The LTC1060 is manufactured by using Linear

The LTC1060 is pinout compatible with MF10.

TYPICAL APPLICATION





LTC 1060

ABSOLUTE MAXIMUM RATINGS

PACKAGE/ORDER INFORMATION

LTC1060AM/LTC1060M -55° C $\leq T_{A} \leq 125^{\circ}$ C
LTC1060AC/LTC1060C -40° C $\leq T_{A} \leq 85^{\circ}$ C
Operating Temperature Range
Power Dissipation 500mW
Supply Voltage18V
1,000

N/AP/HPA N PACKAGE SW PACKAGE 20-LEAD PDIP 20-LEAD PLASTIC SO WIDE T_{AMAX} = 100°C, θ_{AA} = 100°C/W (N) T_{AMAX} = 150°C, θ_{AA} = 80°C/W (SW) CLKA TO LPA 1 BPA 2 (P/HPA 3 INVA 4 S1A 5 SA/B 6 VA⁺ 7 Vb⁺ 8 LSh 9 220 LP8 19 8P8 18 NVAP/HP8 17 NVB 16 S18 15 AGND 14 VA 19 S0/100/HC 50/100/HOLD ORDER PART LTC1060CSW LTC1060CN LTC1060ACN NUMBER

Storage Temperature Range

... -65°C to 150°C

Lead Temperature (Soldering, 10 sec)...

Consult LTC Marketing for parts specified with wider operating temperature ranges LTC1060CJ

OBSOLETE PACKAGE J PACKAGE 20-LEAD CERDIP T_{JIMAX} = 150°C, θ_{JA} = 70°C/W

LTC1060ACJ LTC1060MJ LTC1060AMJ

ELECTRICAL CHARACTERISTICS The ullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. (Complete Filter) $V_S = \pm 5V$, unless otherwise noted.

1050F						
dB		70				Crosstalk
mA	8 12	3		•		Power Supply Current
MHz		1.5				Max Clock Frequency
mV _(P-P)		10			f _{CLK} ≤ 1MHz	Clock Feedthrough
%		±0.1			Mode 1, $Q = 10$, $f_0 = 5kHz$	BP Gain Accuracy at f ₀
%	2	±0.1			Mode 1, R1 = R2 = 50k	DC Lowpass Gain Accuracy
mV	60	4		•	f _{CLK} = 500kHz, 100:1, S _{A/B} = Low	V ₀₈₃
m/	30	2		•	$f_{GLK} = 250 \text{kHz}, 50.1, S_{A/B} = \text{Low}$	Vosa
m۷	60	4		•	f _{CLK} = 500kHz, 100:1, S _{A/R} = Low	Voso
M۷	30	2		•	$f_{CLK} = 250 \text{kHz}, 50:1, S_{MB} = Low$	Voss
m۷	80	0		•	f _{CLK} = 500kHz, 100:1, S _{A/R} = High	Vosa
m۷	40	ω		•	$f_{CLK} = 250 \text{kHz}, 50:1, S_{\Delta/B} = \text{High}$	Voso
m/	15	2		•		DC Offset V _{OS1}
ppm/°c		20			Mode 1, f _{CLK} < 500kHz, Q = 10	Q Temperature Coefficient
ppm/°c		-10			Mode 1, f _{CLK} < 500kHz	f ₀ Temperature Coefficient
%%	σ 1 (±0.5		• •	Mode 1, 50:1 or 100:1, f ₀ = 5kHz, Q=10	LTC1060
200	ىد	+ O 5		•	Mode 1 50:1 or 100:1 fo = 5kHz 0=10	Q Accuracy
	100 ± 0.8%			•	Mode 1, 100:1, f _{CLK} = 500kHz, Q = 10	LTC1060
	$100 \pm 0.3\%$			•	<u>,</u> ,	LTC1060A
	50 ± 0.3%			• •	Mode 1, 50:1, $f_{CLK} = 250 \text{kHz}$, $G = 10$	LTC1060A
	0000			,		Clock-to-Center Frequency Ratio
도 :		0.1 to 16k			f ₀ • Q ≤ 1.6MHz, Mode 1, Figure 4	(See Applications Information)
Н7		0 1 to 20k	1	\dashv	fo • O < 400kHz Mode 1 Figure 4	Center Frequency Range
STINU	MAX	MIN TYP			CONDITIONS	PARAMETER

ELECTRICAL CHARACTERISTICS The \bullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Complete Filter) $V_S = \pm 2.37V$.

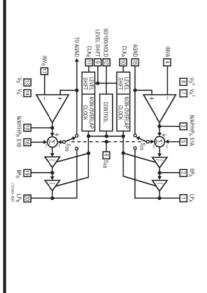
PARAMETER	CONDITIONS		MIN	TYP	MAX	STINU
Center Frequency Range	f ₀ • Q ≤ 100kHz			0.1 to 10k		Hz
Clock-to-Center Frequency Ratio						
LTC1060A	Mode 1, 50:1, f _{CLK} = 250kHz, Q = 10	•			50 ± 0.5%	
LTC1060	Mode 1, 50:1, f _{CLK} = 250kHz, Q = 10			$50 \pm 0.8\%$		
LTC1060A	Mode 1, 100:1, f _{CLK} = 250kHz, Q = 10	•	_	$100 \pm 0.5\%$		
LTC1060	Mode 1, 100:1, f _{GLK} = 250kHz, Q = 10		1	100 ± 0.8%		
Q Accuracy	Model 50:1 or 100:1 f 2 5FHz 0 - 10			3		7/0
LTC1060A LTC1060	Mode1, 50:1 or 100:1, $t_0 = 2.5$ kHz, $Q = 10$ Mode1, 50:1 or 100:1, $t_0 = 2.5$ kHz, $Q = 10$			±4		% %
Max Clock Frequency				500		KHZ
Power Supply Current				2.5	4	mA

The ullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Internal Op Amps).

PARAMETER	CONDITIONS		MIN	TγP	MAX	STINU
Supply Voltage Range			±2.37		# 8	<
Voltage Swings LTC1060A			±4	±4		<
LTC01060 LTC01060, LTC01060A	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1,2,19,20) $R_L = 3.5k$ (Pins 3,18)	•	±3.8	± ± 4		< <
Output Short-Circuit Current Source	V _S = ±5V			25		mA.
Op Amp GBW Product Op Amp Slew Rate Op Amp DC Open Loop Gain	$V_S = \pm 5V$ $V_S = \pm 5V$ $R_L = 10k$, $V_S = \pm 5V$			2 7 85		MHz V/µs
		l				

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

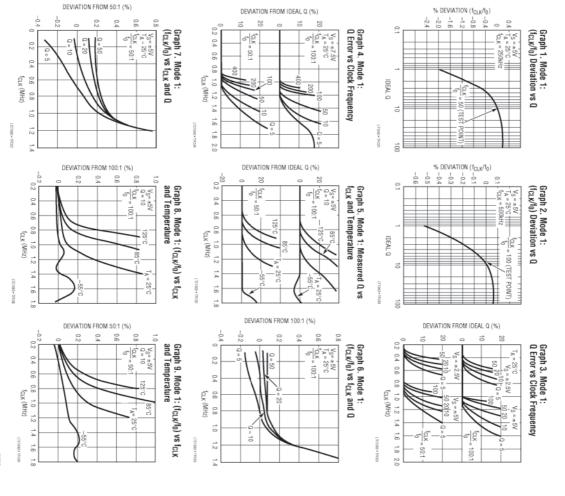
BLOCK DIAGRAM



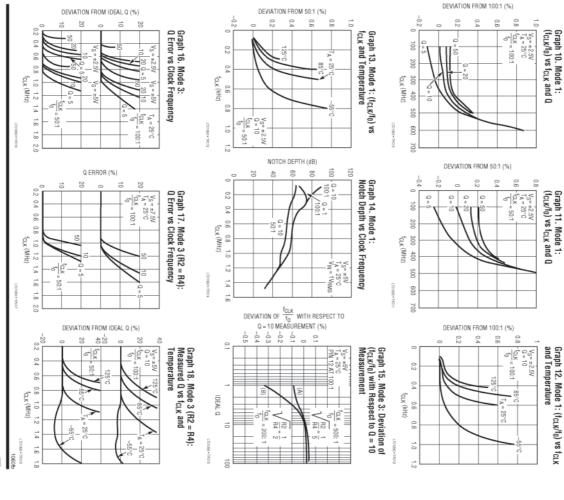
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LTC 1060

TYPICAL PERFORMANCE CHARACTERISTICS

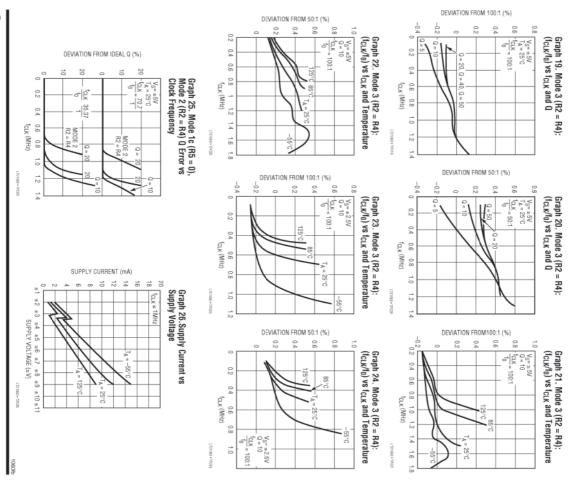


TYPICAL PERFORMANCE CHARACTERISTICS



LTC 1060

TYPICAL PERFORMANCE CHARACTERISTICS







PIN DESCRIPTION AND APPLICATIONS INFORMATION

Power Supplie:

The V+_A and V+_D (pins 7 and 8) and the V-_A and V-_D (Pins 14 and 13) are, respectively, the analog and digital positive and negative supply pins. For most cases, Pins 7 and 8 should be tied together and bypassed by a 0.1 µF disc ceramic capacitor. The same holds for Pins 13 and 14. If the LTC1060 operates in a high digital noise environment, the supply pins can be bypassed separately. Pins 7 and 8 are internally connected through the IC substrate and should be biased from the same DC source. Pins 13 and 14 should also be biased from the same DC source.

The LTC1060 is designed to operate with $\pm 2.5 V$ supply (or single 5V) and with $\pm 5 V$ to $\pm 8 V$ supplies. The minimum supply, where the filter operates reliably, is $\pm 2.37 V$. With low supply operation, the maximum input clock frequency is about 500kHz. Beyond this, the device exhibits excessive Q enhancement and center frequency errors.

Clock Input Pins and Level Shift

of 1000 4th Order Bandpass Filter" circuit. Again, under to ±4.5V, Pin 9 should be connected to ground (same input clock pins (10,11) share the same level shift pin operation, the negative supply pins and the LSh pin should clock levels can be T²L or CMOS. With single supply cycle of the input clock should be close to 50%. For clock these conditions, the clock levels can be T²L or CMOS. The be biased at 1/2 supplies, as shown in the "Single 5V Gain be tied to the system ground. The AGND, Pin 15, should potential as the AGND pin). Under these conditions the CMOS clock levels. With dual supplies equal or higher clocks are recommended. offsets. For clock frequencies above 1MHz, T²L level Fast rising clock edges, however, improve the filter DC from the clock input levels and from its rise and fall times frequencies below 1 MHz, the (f_{CLK}/f_0) ratio is independent typically 1.5V \pm 0.1V above the LSh pin potential. The duty The clock logic threshold level over temperature is The level shift (LSh) Pin 9 is used to accommodate T²L or

50/100/Hold (Pin 12)

By tying Pin 12 to (V^+_A and V^+_D), the filter operates in the 50:1 mode. With $\pm 5V$ supplies, Pin 12 can be typically 1V below the positive supply without affecting the 50:1

operation of the device. By tying Pin 12 to 1/2 supplies (which should be the AGND potential), the LTC1060 operates in the 100:1 mode. The 1/2 supply bias of Pin 12 can vary around the 1/2 supply potential without affecting the 100:1 filter operation. This is shown in Table 1.

When Pin 12 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as a S/H circuit holding the last sample. The hold step is 20mV and the droop rate is 150µV/second!

Table 1

TOTAL POWER SUPPLY	VOLTAGE RANGE OF PIN 12 FOR 100:1 OPERATION
JV	2.5 ± 0.5V
10V	5V ± 1V
15V	7.5V ± 1.5V

S1_A, S1_B (Pins 5 and 16)

These are voltage signal input pins and, if used, they should be driven with a source impedance below 5kΩ. The S1_A, S1_B pins can be used to alter the CLK to center frequency ratio (f_{CLK}/f₀) of the filter (see Modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see Modes 4 and 5). When these pins are not used, they should be tied to the AGND pin.

S_{A/B} (Pin 6)

When S_{AB} is high, the S2 input of the filter's voltage summer (see Block Diagram) is tied to the lowpass output. This frees the S1 pin to realize various modes of operation for improved applications flexibility. When the S_{AB} pin is connected to the negative supply, the S2 input switches to ground and internally becomes inactive. This improves the filter noise performance and typically lowers the value of the offset V_{OS2} .

AGND (PIn 15)

This should be connected to the system ground for dual supply operation. When the LTC1060 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and bypassed with a 0.1 µF capacitor, as shown in the application, "Single 5V, Gain of 1000 4th Order Bandpass Filter." The positive inputs of all the

LTC 1060

APPLICATIONS INFORMATION

internal op amps, as well as the reference point of all the internal switches are connected to the AGND pin. Because of this, a "clean" ground is recommended.

f_{CLK}/f₀ Rati

The f_{CLK}/f_0 reference of 100:1 or 50:1 is derived from the filter center frequency measured in mode 1, with a Q = 10 and $V_S = \pm 5V$. The clock frequencies are, respectively, 500kHz/250kHz for the 100:1/150:1 measurement. All the curves shown in the Typical Performance Characteristics section are normalized to the above references.

Graphs 1 and 2 in the Typical Performance Characteristics show the (f_{CLK}/f_0) variation versus values of ideal Ω . The LTC1060 is a sampled data filter and it only approximates continuous time filters. In this data sheet, the LTC1060 is treated in the frequency domain because this approximation is good enough for most filter applications. The LTC1060 deviates from its ideal continuous filter model when the (f_{CLK}/f_0) ratio decreases and when the Ω 's are low. Since low Ω filters are not selective, the frequency domain approximation is well justified. In Graph 15 the LTC1060 is connected in mode 3 and its (f_{CLK}/f_0) ratio is adjusted to 200:1 and 500:1. Under these conditions, the filter is over-sampled and the (f_{CLK}/f_0) curves are nearly independent of the Ω values. In mode 3, the (f_{CLK}/f_0) ratio typically deviates from the tested one in mode 1 by \pm 0.1%.

f₀ x Q Product Ratio

This is a figure of merit of general purpose active filter building blocks. The $f_0 \times \Omega$ product of the LTC1060 depends on the clock frequency, the power supply voltages, the junction temperature and the mode of operation.

At 25°C ambient temperature for ±5V supplies, and for clock frequencies below 1MHz, in mode 1 and its derivatives, the f₀ × Q product is mainly limited by the desired f₀ and Q accuracy. For instance,from Graph 4 at 50:1 and for f_{CLK} below 800kHz, a predictable ideal Q of 400 can be obtained. Under this condition, a respectable f₀ × Q product of 6.4MHz is achieved. The 16kHz center frequency will be about 0.22% off from the tested value at 250kHz clock (see Graph 1). For the same clock frequency of 800kHz and for the same Q value of 400, the f₀ × Q product can be further increased if the

clock-to-center frequency is lowered below 50:1. In mode 1c with R6 = 0 and R6 = ∞ , the (f_{CLK}/f_0) ratio is 50/ $\sqrt{2}$. The $f_0 \times \Omega$ product can now be increased to 9MHz since, with the same clock frequency and same Ω value, the filter can handle a center frequency of 16kHz $\times \sqrt{2}$.

For clock frequencies above 1MHz, the f₀ x Q product is limited by the clock frequency itself. From Graph 4 at ±7.5V supply, 50:1 and 1.4MHz clock, a Q of 5 has about 8% error; the measured 28kHz center frequency was skewed by 0.8% with respect to the guaranteed value at 250kHz clock. Under these conditions, the f₀ x Q product is only 140kHz but the filter can handle higher input signal frequencies than the 800kHz clock frequency, very high Q case described above.

Mode 3, Figure 11, and the modes of operation where R4 is finite, are "slower" than the basic mode 1. This is shown in Graph 16 and 17. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies. Graph 16 was drawn with a small capacitor, C_{C_1} placed across R4 and as such, at $V_S = \pm 5V$, the $(1/2\pi R4C_C) = 2MHz$. With $V_S = \pm 2.5V$ the $(1/2\pi R4C_C)$ should be equal to 1.4MHz. This allows the Q curve to be slightly "flatter" over a wider range of clock frequencies. If, at $\pm 5V$ supply, the clock is below 900kHz $(0r4000kHz for V_S = \pm 2.5V)$, this capacitor, C_C , is not needed.

For Graph 25, the clock-to-center frequency ratios are altered to 70.7:1 and 35.35:1. This is done by using mode 1c with R5 = 0, Figure 7, or mode 2 with R2 = R4 = $10k\Omega$. The mode 1c, where the input op amp is outside the main loop, is much faster. Mode 2, however, is more versatile At 50:1, and for $T_A = 25^{\circ}C$ the mode 1c can be tuned for center frequencies up to 30kHz.

Output Noise

The wideband RMS noise of the LTC1060 outputs is nearly independent from the clock frequency, provided that the clock fitself does not become part of the noise. The LTC1060 noise slightly decreases with ±2.5V supply. The noise at the BP and LP outputs increases for high Q's. Table 2 shows typical values of wideband RMS noise. The numbers in parentheses are the noise measurement in mode 1 with the S_{A/B} pin shorted to V⁻ as shown in Figure 25.



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APPLICATIONS INFORMATION

Table 2. Wideband RMS Noise

Vs	$\frac{f_{CLK}}{f_0}$	NOTCH/HP (μV _{RMS})	BP (μV _{RMS})	LP (SWBΛη)	CONDITIONS
±5V	50:1	49 (42)	52 (43)	75 (65)	Mode1, R1 = R2 = R3
±5√	100:1	70 (55)	80 (58)	90 (88)	Q = 1
±2.5V	50:1	33 (31)	36 (32)	48 (43)	
±2.5V	100:1	48 (40)	52 (40)	66 (55)	
±5V	50:1	20 (18)	150 (125)	186 (155)	Mode 1, Q = 10
±5V	100:1	25 (21)	220 (160)	240 (180)	R1 = R3 for BP out
±2.5V	50:1	16 (15)	100 (80)	106 (87)	R1 = R2 for LP out
±2.5V	100.1	20 (17)	150 (105)	150 (119)	
±5V	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4
±5V	100:1	72	72	80	Q = 1
±2.5V	50:1	40	40	42	
±2.5V	100.1	50	50	53	
±5V	50:1	135	120	140	Mode 3, R2 = R4, Q = 10
±5V	100:1	170	160	185	R3 = R1 for BP out
±2.5V	50:1	100	88	100	R4 = R1 for LP and HP out
±2.5V	100:1	125	115	130	

Short-Circuit Currents

are allowed as long as the power supplies do not exceed Short circuits to ground, positive or negative power supply Above ±5V and at elevated temperatures, continuous ±5V and the ambient temperature stays below 85°C.

short circuits to the negative power supply will cause allowed to exceed 80mA device will get damaged if the short-circuit current is excessive currents to flow. Under these conditions, the

DEFINITION OF FILTER FUNCTIONS

external clock and a few resistors, closely approximates Each building block of the LTC1060, together with an rrequency domain. 2nd order filter functions. These are tabulated below in the

1. Bandpass function: available at the bandpass output Pins 2 (19). (Figure 1.)

$$G(s) = H_{0LP} \frac{\omega_0^2}{s^2 + s(\omega_0/0)}$$

$$G(s) = H_{OBP} \frac{s\omega_{o}/Q}{s^{2} + (s\omega_{o}/Q) + \omega_{o}^{2}}$$

 $H_{OBP} = Gain at \omega = \omega_0$

 $f_0 = \omega/2\pi$; f_0 is the center frequency of the complex between input and output is -180°. pole pair. At this frequency, the phase shift



Lowpass function: available at the LP output Pins 1 (20). (Figure 2.)

sured at the filter BP output.

der bandpass function. The Q is always mearatio of f₀ to the -3dB bandwidth of the 2nd orQ = Quality factor of the complex pole pair. It is the

HOLP DC gain of the LP output



LTC 1060

DEFINITION OF FILTER FUNCTIONS

3. **Highpass function:** available only in mode 3 at the ouput Pins 3 (18). (Figure 3.)

Allpass function: available at Pins 3 (18) for mode 4, 4a

 $G(s) = H_{0AP} \frac{[s^2 - s(\omega_0/Q) + \omega_0^2]}{s^2 + s(\omega_0/Q) + \omega_0^2}$

 $H_{OAP} = gain of the allpass output for <math>0 < f < \frac{T_{CLK}}{2}$

$$G(s) = H_{OHP} \frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

$$H_{OHP} = \text{ gain of the HP output for } f \rightarrow \frac{f_{CLK}}{2}$$

4. Notch function: available at Pins 3 (18) for several

the numerator complex zero pair is the same as the

response is a straight line. In mode 5, the center frequency

modes of operation.

G(s) = (H_{0N2})
$$\frac{s^2 + \omega^2_0}{s^2 + (s\omega_0/Q) + \omega_0^2}$$

 $H_{ON2} = gain of the notch output for <math>f \rightarrow \frac{I_{CLK}}{2}$

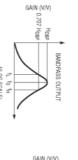
a notch at f_z.

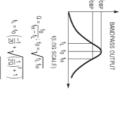
For high numerator Q's, the magnitude response will have f₂, of the numerator complex zero pair, is different than f₀ denominator. Under these conditions, the magnitude For allpass functions, the center frequency and the Q of

 $H_{ON1} = gain of the notch output for f \rightarrow 0$

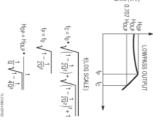
 $f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

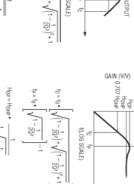
HIGHPASS OUTPUT













MODES OF OPERATION

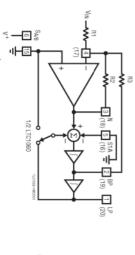
Table 3. Modes of Operation: 1st Order Functions

7	6b	6a	MODE
LP	LP	Ę	PIN 2 (19)
AP	LP	푸	PIN 3 (18)
100(50) R3	$\frac{f_{CLK}}{100(50)} \cdot \frac{R2}{R3}$	f _{CLK} • R2 100(50) • R3	fc
<u>f_{CLK}</u> • R2 100(50) • R3			f _Z

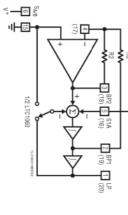
MODES OF OPERATION

Table 4. Modes of Operation: 2nd Order Functions

თ	4a	4	32	ω	26	2a	2	10	16	1a	_	MODE	
LР	ГP	LP	LP	ГÞ	F	гP	LP	ГÞ	LP	LP	LP	PIN 1 (20)	
ВP	BP	ВР	BP	BP	ВР	ВP	ВР	ВР	BP	ВР	ВР	PIN 2 (19)	
CZ	AP	AP	Notch	HP	Notch	Notch	Notch	Notch	Notch	ВР	Notch	PIN 3 (18)	
$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \bullet \sqrt{\frac{R2}{R4}}$	f _{CLK} 100(50)	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R6}{R5 + R6}}$	$\frac{f_{GLK}}{100(50)} \cdot \sqrt{\frac{R6}{R5 + R6}}$	f _{CLK} 100(50)	f _{CLK} 100(50)	f ₀	
$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 - \frac{R1}{R4}}$			$\frac{f_{CLK}}{100(50)} \cdot \sqrt{\frac{R_h}{R_l}}$		$\frac{f_{GLK}}{100(50)} \cdot \sqrt{\frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R6}{R5 + R6}}$	f _{CLK} 100(50)	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{1 + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \cdot \sqrt{\frac{R6}{R5 + R6}}$			f ₀	



 $\label{eq:continuous} \begin{array}{l} i_{0}=\frac{i_{O,K}}{100(80)}; i_{n}=i_{0}: h_{OLP}=\frac{R2}{R1}; h_{OBP}=-\frac{R3}{R1}; h_{OHH}=-\frac{R2}{R1}; \alpha=\frac{R3}{R2} \end{array}$ Figure 4. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass



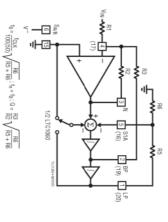
 $f_0 = \frac{f_{Q,K}}{100(50)}; \Omega = \frac{R3}{R2}; H_{0BP1} = -\frac{R3}{R2}; H_{0BP2} = 1 (NON-INVERTING) H_{Q,LP} = -1$

Figure 5. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

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LTC 1060

MODES OF OPERATION



$$\begin{split} & \text{H}_{0H1}(I\rightarrow 0) = \text{H}_{0H2}\left[1\rightarrow\frac{t_{QLK}}{2}\right] = -\frac{R_{2}^{2}}{R^{2}}: \text{H}_{QLP} = \frac{-R_{2}R_{1}}{R_{1}}: \text{H}_{QBP} = -\frac{R_{3}^{2}}{R^{2}}: \text{H}_{QBP} = \frac{R_{3}^{2}}{R^{2}}: \text{RS} < St\Omega \end{split}$$
 Figure 6. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

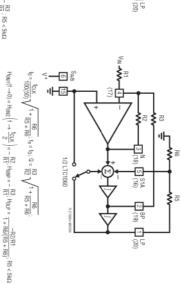


Figure 7. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass

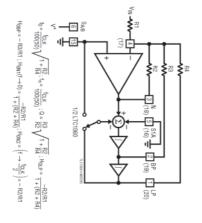


Figure 8. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass

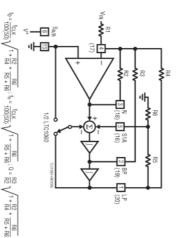
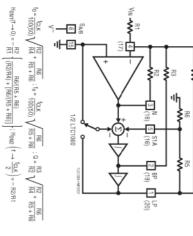


Figure 9. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

 $H_{OM1}(f\to 0) = -\frac{R2}{R1} \left\{ \frac{1 + R6/(R5 + R6)}{1 + (R2/R4) + [R6/(R5 + R6)]} \right\}, H_{OM2}f \left(\to \frac{f_{CLK}}{2}\right) = -R2/R1$

 $H_{OBP} = -R3/R1 : H_{OLP} = \frac{-R2/R1}{1 + (R2/R4) + [R6/(R5 + R6)]}$

MODES OF OPERATION

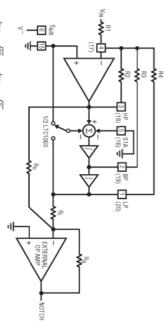


V_{IN} - R1 - (17) $t_0 = \frac{t_{OLK}}{100(50)} \sqrt{\frac{R_2^2}{R^4}}, \Omega = \frac{R3}{R2} \sqrt{\frac{R_2^2}{R^4}}, \\ H_{OHP} = -R2/R1, \\ H_{OBP} = -R3/R1, \\ H_{OLP} = -R4/R1, \\ H_{OBP} = -R3/R1, \\ H_{OLP} = -R4/R1, \\ H_{OLP$ **≸**≅ 1/2 LTC1060 다(16) 는 후(19) 다(20)

Figure 11. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

Figure 10. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

 $H_{OBP} = -R3/R1 ; H_{OLP} = \frac{-R2/R1}{(R2/R4) + [R6/(R5 + R6)]}$



 $f_0 = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_2}{R^4}} \cdot f_n = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_3}{R_1}} : H_{OHP} = -R2/R1; \ H_{OBP} = -R3/R1, H_{OLP} = -R4/R1$ $H_{0W1}(t \to 0) = \frac{R_{9}}{R_{1}} \bullet \frac{R4}{R1} + H_{0N2}\left(t \to \frac{t_{CLK}}{2}\right) = \frac{R_{9}}{R_{h}} \bullet \frac{R2}{R1} + H_{0W}(t = t_{0}) = \Omega\left(\frac{R_{9}}{R_{1}} + H_{0LP} - \frac{R_{9}}{R_{h}} + t_{0HP}\right); \Omega = \frac{R3}{R2} \sqrt{\frac{R2}{R4}} + \frac{R2}{R4} + \frac{R$

Figure 12. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

LTC 1060

MODES OF OPERATION

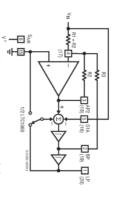


Figure 13. Mode 4: 2nd Order Filter Providing Allpass Bandpass, Lowpass $t_0 = \frac{t_{GLK}}{100(50)}, Q = \frac{R3}{R2}, H_{GMP} = -\frac{R2}{R1}, H_{GLP} = -2, H_{GBP} = -2\left(\frac{R3}{R2}\right)$

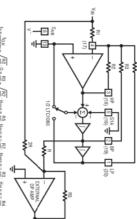


Figure 14. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass $t_0 = \frac{t_{OLK}}{100(50)} \sqrt{\frac{R2}{R4}}, 0 = \frac{R3}{R2} \sqrt{\frac{R2}{R4}}, H_{ONP} = \frac{R5}{2R}, H_{OHP} = -\frac{R2}{R1}, H_{OSP} = -\frac{R3}{R1}, H_{OLP} = -\frac{R4}{R1}$

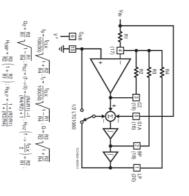


Figure 15. Mode 5: 2nd Order Filter Providing Numeralor Complex Zeros, Bandpass, Lowpass

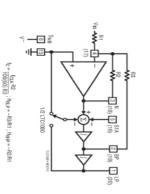


Figure 16. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

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LTC 1060

MODES OF OPERATION

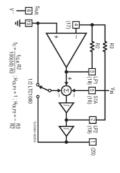


Figure 17. Mode 6b: 1st Order Filter Providing Lowpass

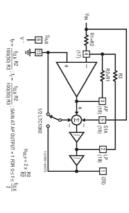


Figure 18. Mode 7: 1st Order Filter Providing Allpass, Lowpass

COMMENTS ON THE MODES OF OPERATION

mode 2, mode 3. In the mode 1 (Figure 4), the input are becoming noticeable above 1MHz clock frequency. than modes 2 and 3. In mode 1, for instance, the Q errors amplifier is outside the resonant loop. Because of this mode 1 and its derivatives (mode 1a, 1b, 1c) are faster There are basically three modes of operation: mode 1

a second order, clock tunable, BP resonator can be achievof the LTC1060. Mode 1a is useful when voltage gain at the depends on the external clock frequency. For high order ed with only 2 resistors. The filter center frequency directly bandpass output is required. The bandpass voltage gain Mode 1a (Figure 5), represents the most simple hook-up clock frequencies to tune the overall filter response. filters, mode 1a is not practical since it may require several nowever, is equal to the value of Q; if this is acceptable

creating problems with the dynamics of the notch filters. In mode 1, a bandpass output with a very depth is shown in Graph 14. Mode 1 is a practical Mode 1 (Figure 4), provides a clock tunable notch; the remaining notch and lowpass outputs. nigh Q, together with unity gain, can be obtained without configuration for second order clock tunable bandpass/

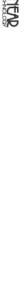
produce a notch with a frequency which is always equal to external resistor ratio the center frequency, nowever, can be adjusted with an the filter building block center frequency. The notch and Modes 1b and 1c (Figures 6 and 7), are similar. They both

The practical clock-to-center frequency ratio range is:

$$\frac{500}{1} \ge \frac{f_{CLK}}{f_0} \ge \frac{100}{1} \left(\text{or } \frac{50}{1} \right); \text{ mode 1b}$$

$$\frac{100}{1} \text{ or } \frac{50}{1} \ge \frac{f_{CLK}}{f_0} \ge \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}}; \text{ mode 1c}$$

overall filter will increase proportionally and so will the BW shown in Graph 25. Figure 19 illustrates how to cascade operation: In the 50:1 mode and with $(R5 = 0, R6 = \infty)$ the clock-to-center frequency ratio becomes $(50/\sqrt{2})$ and cenoperation yield constant Q's; with any filter realization the to maintain the 20:1 ratio constant. All the modes of and in general R5 should not be larger than 5k. Mode fourth order bandpass filter is 20/1. By varying the clock filter. Note that the center frequency to the BW ratio for this obtain a sharp fourth order, 1dB ripple, BP Chebyshev the two sections of the LTC1060 connected in mode 1c to large output offsets. Mode 1c is the fastest mode of (f_{CLK}/f_0) ratio is 500:1. Beyond this, the filter will exhibit can be used to increase the clock-to-center frequency Figure 19, where the BP filter is swept from 1kHz to 20kHz BW's will vary when the filter is swept. This is shown in frequency to sweep the filter, the center frequency of the ter frequencies beyond 20kHz can easily be achieved as ratio beyond 100:1. For this mode, a practical limit for the The input impedance of the S1 pin is clock dependent



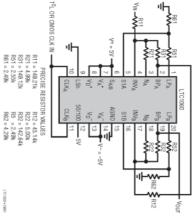
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LTC 1060

COMMENTS ON THE MODES OF OPERATION

Modes 2, 2a, and 2b have a notch output which frequency, when cascading second order functions to create an f₀. For all cases, however, f_n<f₀. These modes are useful f_n, can be tuned independently from the center frequency,

derivatives are slower than mode 1's. input amplifier and its feedback resistors (R2/R4) are now overall elliptic highpass, bandpass or notch response. The part of the resonant loop. Because of this, mode 2 and its



-15dB -ZbdE -15d -10dE -10dB -5dB -5dB 0dB Ode

Figure 19. Cascading the Two Sections of the LTC1060 Connected in Mode 1c to Obtain a Clock Tunable 4th Order 1dB Ripple Bandpass Chebyshev Filter with (Center Frequency)/(Ripple Bw) = 20/1.

summing the highpass and lowpass outputs (mode 3a vidual Q's are 29.6 and the filter maintains its shape and inverting input of the second section op amp. The indidirectly the HP and LP outputs of the first section into the bandpass filter. The first notch is created by summing 3a to obtain a clock tunable 4th order sharp elliptic shows the two sections of an LTC1060 connected in mode sections to obtain high order elliptic filters. Figure 20 through progressive integration; notches are obtained by since it provides a nighpass, bandpass, lowpass output (or f_{CLK}/50) ratio. Mode 3 is a state variable configuration In mode 3 (Figure 11), a single resistor ratio (R2/R4) can performance up to 20kHz center frequency (Figure 21) versatile and useful modes for cascading second order (Rh/Ri). Because of this, modes 3 and 3a are the most above the center frequency through the resistor ratio tune the center frequency below or above the t_{CLK}/100 2nd notch. The dynamics of Figure 20 are excellent be-For this circuit an external op amp is required to obtain the rigure 12). The notch trequency can be tuned below or



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COMMENTS ON THE MODES OF OPERATION

mode 2b section (Figure 22), has a gain exceeding unity which limits the dynamic range of the overall filter. For very selective bandpass/bandreject filters, the mode 3a

approach, as in Figure 20, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the LTC1060.

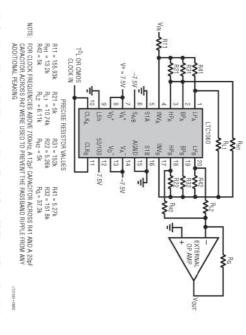


Figure 20. Combining Mode 3 with Mode 3a to Make The 4th Order BP Filter of Figure 21 with Improved Dynamics. The Gain at Each Output Node is < 0dB for all Input Frequencies.

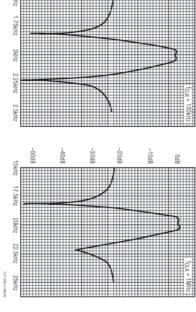


Figure 21. The BP Filter of Figure 20, When Swept From a 2kHz to 20kHz Center Frequency.

-50dB

40dB

-30dB

-20dB

-10dB

0dB

LTC 1060

COMMENTS ON THE MODES OF OPERATION

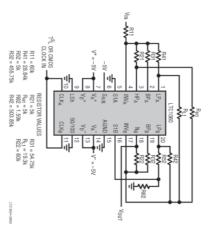


Figure 22. Combining Mode 3 with Mode 2b to Create a 4th Order BR Elliptic Filter with 1dB Ripple and a Ratio of 0dB to Stop Bandwidth Equal to 9/1.

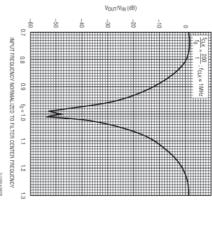


Figure 23. Amplitude Response of the Notch Filter of Figure 22

LTC1060 OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R, C integrators. These offsets are mainly due to the charge injection of the CMOS switches into the integrating capacitors and they are temperature independent.

The internal op amp offsets also add to the overall offset budget and they are typically a couple of millivolts. Because of this, the DC output offsets of switched capacitor filters are usually higher than the offsets of discrete active filters.

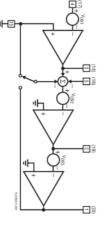


Figure 24. Equivalent Input Offsets of 1/2 LTC1060 Filter Building Block

Figure 24 shows half of an LTC1060 filter building block with its equivalent input offsets V_{OS1} , V_{OS2} , V_{OS3} . All three are 100% tested for both sides of the LTC1060. V_{OS2} is generally the larger offset. When the $S_{A/B}$, Pin 6, of the LTC1060 is shorted to the negative supply (i.e., mode 3), the value of the V_{OS2} decreases. Additionally, with $S_{A/B}$ low, a 20% to 30% noise reduction is observed. Mode 1 can still be achieved, if desired, by shorting the S1 pin to the lowpass output (Figure 25).

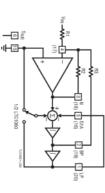


Figure 25. Mode 1(LN): Same Operation as Mode 1 but Lower v_{082} Offset and Lower Noise

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LTC1060 OFFSETS

Output Offsets

to V_{0S3} . The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 5 illustrates this. The DC offset at the filter bandpass output is always equal

especially when the filter handles input signals with large It is important to know the value of the DC output offsets

> increase when: dynamic range. As a rule of thumb, the output DC offsets

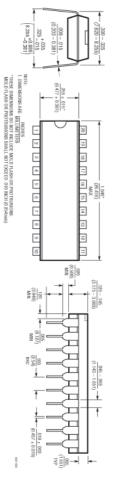
- The Q's decrease.
- 2. The ratio ($f_{\rm CLK}/f_0$) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

Table 5

	3, 4a	26	2a	2, 5	1c	1b	1a	1,4	MODE
	V _{0S2}	$ \begin{bmatrix} V_{OS1}(1+R2/R1+R2/R3+R2/R4) - V_{OSS}(R2/R3)] \\ \bullet \begin{bmatrix} R4k \\ R2 + R4k \end{bmatrix} + V_{OS2} \begin{bmatrix} R2 \\ R2 + R4k \end{bmatrix} : k = \frac{R6}{R5 + R6} $	$ \begin{aligned} & [V_{OS1}(1+R2/R1+R2/R3+R2/R4)-V_{OSS}(R2/R3)] \\ & \bullet \underbrace{\begin{bmatrix} R4(1+k) \\ R2+R4(1+k) \end{bmatrix}}_{} + V_{OS2}\underbrace{\begin{bmatrix} R2 \\ R2+R4(1+k) \end{bmatrix}}_{} : k = \frac{R6}{R5+R6} \end{aligned} $	[V _{OS1} (1 + R2/R1 + R2/R3 + R2/R4) – V _{OS3} (R2/R3)] • [R4/(R2 + R4)] + V _{OS2} [R2/(R2 + R4)]	V _{OS1} [(1/Q) + 1 + R2/R1] = V _{OSS} /Q	V _{0S1} [(1/Q) + 1 + R2/R1] - V _{0S3} /Q	V _{0S1} [1 + (1/Q)] - V _{0S3} /Q	V _{0S1} [(1/Q) + 1 + H _{0LP}] - V _{0S3} /Q	V _{0SN} PIN 3 (18)
	V _{0S3}	V ₀₈₃	V _{0S3}	V _{0S3}	V _{0S3}	V _{OS3}	V _{0S3}	V ₀₈₃	V _{0SBP} PIN 2 (19)
$-V_{OSS}\left\langle \frac{R4}{R3}\right\rangle$	$V_{OS1}\left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3}\right] - V_{OS2}\left(\frac{R4}{R2}\right)$	~ (V _{OSN} – V _{OS2}) (1 + R5/R6)	~(V _{OSN} - V _{OS2}) (R5 + R6) (R5 + 2R6)	V _{OSN} - V _{OS2}	$\sim (V_{OSN} - V_{OS2}) \frac{(R5 + R6)}{(R5 + 2R6)}$	~ (V _{OSN} - V _{OS2}) (1 + R5/R6)	V _{OSN} - V _{OS2}	V _{OSN} - V _{OS2}	V _{OSLP} PIN 1 (20)

PACKAGE DESCRIPTION

N Package 20-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



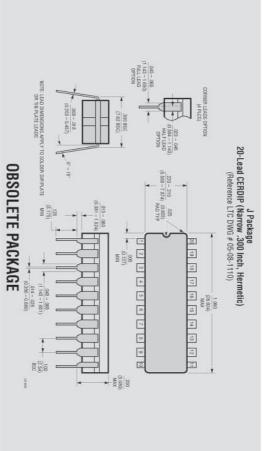


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LTC 1060

PACKAGE DESCRIPTION



SW Package 20-Lead Plastic Small Outline (Wide .300 Inch)

