Stacked Power Module with Integrated Thermal Management

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***Abstract*—Current power electronics devices are unable to realize their full capabilities due to the challenges of standard planar packaging including heat dissipation, reliability and parasitic inductance. This work aims to address all of these challenges simultaneously, thus creating a revolutionary approach to power packaging which significantly improves overall capability. The new approach stacks power devices between copper layers with an integrated heat sink. By stacking devices, the module is no longer constrained by the limitations of planar packaging; however it is limited by the ability to remove heat which is solved by integrating heat sinks directly in contact with both the top and bottom of each die. The key-enabling feature of this packaging approach is the multi-functional components (MFCs) which act as electrical, thermal and mechanical attachments concurrently. This co-designed approach aims to eliminate single function components such as wirebonds and heat sinks whose sole purpose is electrical conduction or heat removal, respectively, and replace them with MFCs. This work describes the fabrication of the module and also shows thermal, fluid, and mechanical modeling results. The modeling showed a total package thermal resistivity of 0.25 K-cm^2/W. This new power module configuration has the potential to significantly reduce size, weight and cost while improving reliability and performance.**

Keywords—power module, integrated heat sink, half bridge, stacked devices, direct die cooling, multi-functional components

I. INTRODUCTION

There is a trend in power electronics towards more power in smaller packages which leads to significantly higher power densities and the need to remove more heat [1]. The devices can handle the high currents and voltages but must often be derated due to the limitations of the packaging. Current power electronics modules are large and heavy. Most of the mass and volume results from the packaging, not the electronic components. A conventional power package is shown in Fig. 1 and contains a direct bond copper (DBC) substrate that has devices soldered to one side and a heat spreader and/or heat sink attached to the other. A thermal material interface (TIM) separates the heat spreader from the heat sink. Wirebonds are used to make the electrical connections.

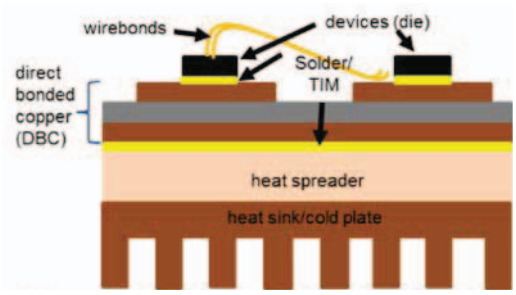

Fig. 1. Standard power module configuration

There are three primary challenges associated with current power modules: heat removal, reliability, and parasitic inductance. Most research to date has explored options of addressing only one of these challenges by methods such as adding a more compliant die attach or incorporating a better heat sink. As power electronics requirements increase, the importance of increasing performance by focusing on improving all these challenges simultaneously also increases.

A. Power Module Challenge 1: Heat Dissipation

Thermal management is crucial in high power electronics due to the extremely large amount of heat that is dissipated by the devices [2]. The amount of power that a module can achieve is most often temperature limited; therefore, if the heat can more effectively be removed, the module can operate at a higher power density. In addition, most reliability concerns are strongly temperature dependent; therefore, reducing device temperature will improve reliability. The most efficient thermal solutions allow for double-sided cooling which allows heat to be dissipated from both the top and bottom surfaces.

B. Power Module Challenge 2: Reliability

The three primary sources of mechanical failure in power modules are wirebond failure, large area contact stress failure, and substrate (DBC) cracking. [3] There has been significant research into improving each of these failure mechanisms individually. A number of efforts have looked into eliminating the wirebonds to improve reliability [4, 5, 6, 7].

The second primary failure location is the large area contacts, both the die attach and substrate attach, due to CTE

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mismatch [8]. A variety of research into compliant and conductive thermal interface materials such as sintered silver, copper springs, and carbon nanotubes have been investigated to alleviate failures due to CTE mismatch [9]. In addition, CTE matched materials such as TiW, AlSiC, and CuMo heat spreaders have also been used [12].

The third failure location is the DBC which fails due to CTE mismatch between the copper and ceramic. Some methods that have been explored to improve DBC reliability include alternative substrates such as direct bond aluminum (DBA) or active metal braze (AMB) boards [10] as well as dimpling or stepping the copper edges [14].

The problem with most of these solutions is that they only improve upon one aspect of the complete reliability challenge. The solution presented in this work addresses all of these challenges concurrently by utilizing a completely new approach to power module design that eliminates the DBC, wirebonds and large area contacts (both at the die and substrate levels).

C. Power Module Challenge 3: Parasitic Inductance

Parasitic inductance is a primary concern in power electronics modules [11]. Wirebonds and long planar leads in planar power packaging topologies is a significant cause of parasitic inductance. Stacking devices and eliminating wirebonds are ways to reduce inductance.

D. Co-Designed Power Module

The standard power module design process is sequential starting with an electrical engineer designing the circuit, then a mechanical engineer designing the packaging, and finally a thermal engineer specifying a heat sink. This approach leads to a module that is not optimized, nor does it perform at its peak potential. Therefore, there is a need in the power electronics industry to develop co-designed packaging solutions which simultaneously optimize the electrical, thermal and mechanical design solutions.

Chip stacking has become very popular recently in commercial electronics. Chip stacking reduces system size, increases power density, reduces inductance, and improves electrical performance. But chip stacking creates a significant thermal challenge due to the difficulties in dissipating heat through adjacent devices that are generating their own heat. This is especially true in power modules, which have significantly more heat dissipation then other electronics modules; therefore, an advanced thermal solution is required.

Some chip stack applications have been developed for power electronics. A commercial module is the Power Stack [12]. In this module, power devices are stacked but there is no integrated heat sink and it still requires solid dielectrics. There have also been a number of patents related to stacking power devices, also none of which have eliminated the solid dielectrics nor integrated a heat sink [13, 14, 15].

II. STACKED POWER MODULE WITH INTEGRATED COOLING

The module presented in this work consists of a half-bridge module with stacked die and integrated cooling. The structure of the module is shown in Fig. 2 next to a half-bridge circuit schematic. A half-bridge module was demonstrated because it is the building block of many power circuits (inverters and converters). This module's structure is both modular and scalable to accommodate any number of configurations of diodes and switching devices. The half-bridge module shown consists of two diodes and two switching devices (ex. IGBTs, MOSFETS, etc.). The devices are packaged in a series arrangement as opposed to a more typical anti-parallel configuration to reduce inductance [16].

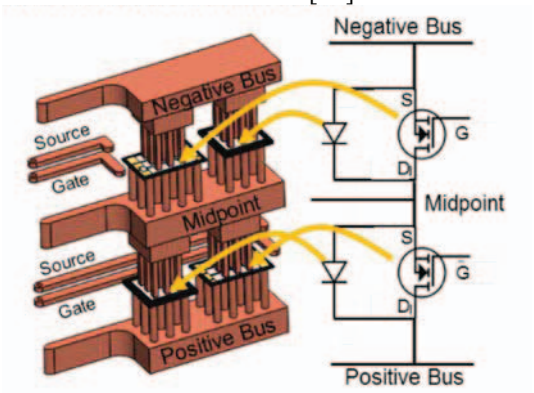

Fig. 2. Half-bridge circuit schematic indicating the location of the two switches and two diodes in the assembly.

There are five main layers, specified in Fig. 3, that alternate between machined electrically conductive material (Layers 1, 3 and 5) and devices (Layers 2 and 4). In this module, the electrically conductive layers are fabricated out of copper and the devices are silicon carbide (SiC). The base layer (Layer 5) acts as the positive bus in the circuit. It connects the drain of the switching device to the cathode of the associated diode (Layer 4). The next layer (Layer 3) consists of a conductive layer that acts as the midpoint on the circuit schematic. It electrically connects the source of the lower switching device and the anode of the lower diode to the cathode of the upper diode and the drain of the upper switching device (Layer 2). The final layer (Layer 1) acts as the negative bus in the half bridge module connecting the source of the upper switching device to the anode of the diode. During fabrication, the module was assembled in two similar parts, labeled at the upper and lower diode-switch structure in Fig. 3.

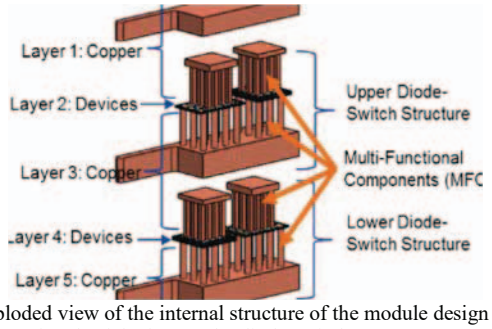

Fig. 3. Exploded view of the internal structure of the module design showing the locations of each of the layers, the diode-switch structures, as well as the multi-functional components.

This design depicts the type of electronics package that can be realized when a co-design approach is used to account for the electrical, thermal and mechanical aspects of the design up

front. This package has eliminated many of the single function components (e.g. wirebonds, heat sinks, encapsulants, solid dielectrics) and replaced them with multi-functional components (MFCs), which are labeled in Fig. 3 and are a key enabling feature of this design. The MFCs serve three purposes: (1) heat dissipation by removing heat directly from the devices, (2) electrical by completing the electrical circuit, and (3) low stress mechanical interconnects.

The improvements in the thermal, electrical and mechanical (reliability) domains are depicted in Fig. 4. In the thermal domain, a fluid (either air or dielectric fluid) is passed directly over each device and its associated thermal fins on both the top and bottom of the die, allowing double-sided cooling. In the mechanical domain, the three primary failure mechanisms have been eliminated; there is no DBC, significantly fewer wirebonds, and no large area contacts between different materials. In the electrical domain, the stacked structure reduces the parasitic inductance as well as improves overall power density by reducing volume. Even the cooling fluid serves multiple purposes: thermal and voltage blocking.

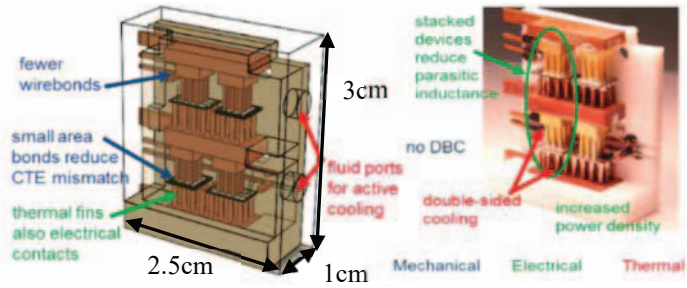

Fig. 4. Locations of the thermal, mechanical and electrical improvements of the power module assembly. Overall module dimensions are also shown.

III. Fabrication Process

The process shown below was developed after a variety of experiments to optimize the fabrication methodology.

A. Step 1: Wirebond the MOSFETs

The first step is to wirebond the gate and source sense wires to the bare MOSFET. The primary source wirebonds have been eliminated from the structure and replaced with MFCs. To reduce complexity and as a result of low failure risk, the gate and source cense wirebonds remain. The gate wires are not a primary failure mechanism because they carry very little current and have a very small temperature rise in this configuration. The 5-mil wirebonds were placed onto the MOSFET, then secured into place using a high temperature epoxy to reduce the likelihood of breaking during subsequent handling. The non-secured ends of the wirebonds were left long for ease of handling and will be cut to size later in the assembly process. The completed step is shown in Fig. 5.

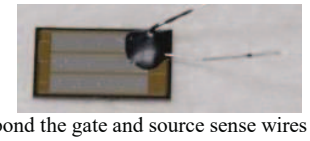

Fig. 5. Step 1: Wirebond the gate and source sense wires on the MOSFET and secure into place.

B. Step 2: Align and Attach the MFCs to the Devices

The second step is to attach the MFCs to the tops of each device. This is the most critical alignment step, especially for the MOSFETs since the connections must adhere to the source fingers. The MFCs, shown in Fig. 6a, were machined out of copper using an EDM (electrical discharge machining) tool to ensure precise dimensions, then plated with electroless nickel immersion gold. An alignment fixture was machined out of aluminum for both the MOSFET and diode to allow proper placement of the device on the MFC. A silver epoxy, Epo-tek EK1000, was chosen as the die attach material due to its high thermal conductivity (35 W/mK), high operating temperature (200°C), shear strength, and its ability to adhere to the aluminum top surface of the device. The assembly was cured according to the datasheet to maximize thermal and electrical properties. The completed diode and MOSFET assemblies are shown in Fig. 6b and c, respectively.

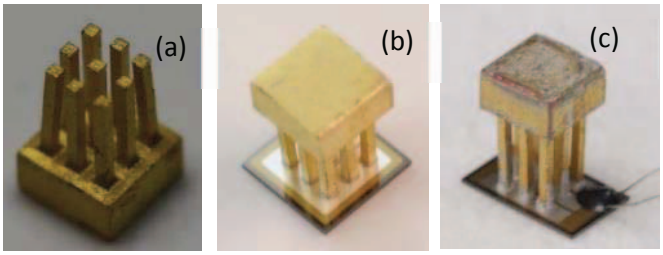

Fig. 6. (a) Shows the MFC. Images of the MFCs attached to the (a) diode and (b) MOSFET

C. Step 3: Align and Bond Diode-Switch Structures

Step 3 assembles the diode-switch structures which comprise one diode/MFC part, one MOSFET/MFC part, and a larger MFC part. The larger MFC was machined out of a commercial copper heat sink, the SLF-1 Ultra, which was chosen due to its fin dimensions. The machined aluminum alignment part is shown in Fig. 7a. Each of the diode/MFC parts are placed into the alignment part, then the silver epoxy (Epo-tek EK1000) is applied to the bottoms of both devices as well as the fins of the large MFC. The large MFC is then placed into the alignment part (Fig. 7b) and slight pressure is applied ensuring good contact. The assembly is then cured as in Step 2.

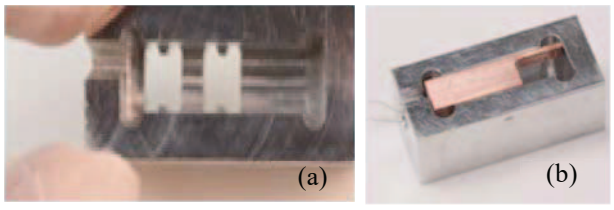

Fig. 7. Assembly process for Step 3 showing (a) the machined alignment part and (b) the larger MFC placed on top of the devices to complete the assembly.

The assembly process is repeated using the same alignment fixture for the other diode-switch structure except that the diode and MOSFET are in the opposite alignment holes.

D. Step 4: Align and Bond Complete Stack

The next step bonds the two diode-switch structures to the top of the layer 1 copper (negative bus). Since all the critical device alignment has already been done, the assembly is simply

stacked inside a machined aluminum box as is shown in Fig. 8 and attached using the same silver epoxy (Epo-tek EK1000).

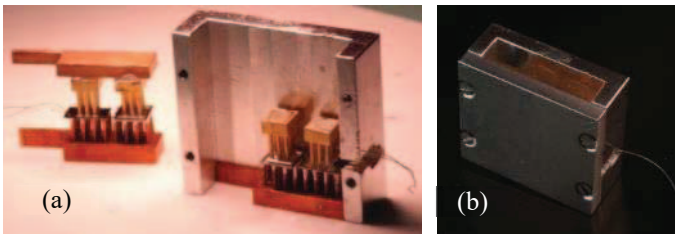

Fig. 8. Assembly process for Step 4 indicating how the diode-switch structures fit into the stacked assembly box.

E. Step 5: Secure into Housing and Attach Gate Wires

Step 5 places the stacked assembly into the additively manufactured (AM) housing and completes wirebond connections. Machined copper L-shaped connectors are first placed into slots on the side of the housing, then the complete half-bridge stack is set into a cavity at the bottom of the housing, shown in in Fig. 9. The wirebonds are then cut to size and wirebonded to the L-shaped connectors, shown in Fig. 9. The L-shaped connectors are then secured into place using high temperature epoxy. The final assembly with all mechanical, electrical and thermal contacts is shown in Fig. 9.

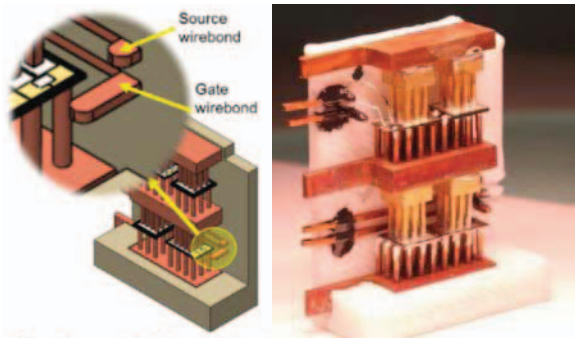

Fig. 9. Complete stacked assembly with all electrical and thermal contacts.

F. Step 6: Fluidically Seal Housing

The final fabrication step involves fluidically sealing the housing. The housing, shown in Fig. 10a, is a two-part assembly AM using polycarbonate. This step includes securing the second half of the assembly using epoxy then treating the entire exterior of the package to fluidically seal the package for testing. The final assembly is shown in Fig. 10b indicating the fluid inlet and outlet on the right side and the relationship of the housing to the half-bridge structure.

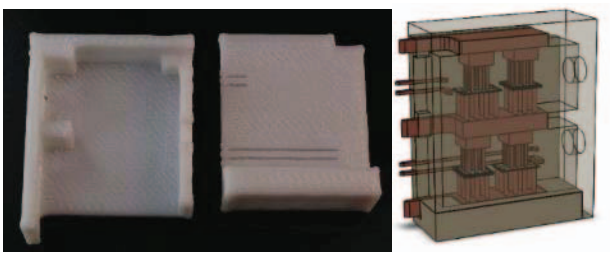

Fig. 10. (a) Image of the two sides of the additively manufactured housing and (b) location of the stacked half-bridge assembly in the housing.

IV. Results and Discussion

A series of models have been completed to predict the thermal and mechanical performance of the power module. Modeling was done using the flow simulation capabilities of SOLIDWORKS. This is a finite volume approach that solves the conjugate heat transfer problem. An initial mesh of 706,000 elements was used and an additional mesh with 50% more elements was used to verify mesh independence. Results for both meshes agreed, so the less dense mesh was used. The model was run for flow rates of 0.01, 0.025, 0.05, 0.1, 0.2 and 0.4 kg/s at power levels of 100, 200 and 500 W/cm^2. Temperature results of the thermal-fluid modeling are shown as an inset in Fig. 11 for a device heat flux of 500 W/cm^2 and a mass flow rate of 0.1 kg/sec. The fluid used for the analysis was HFE7500, a dielectric fluid, with an inlet temperature of 20 °C. The increase in device temperature is 124.6 °C at 500 W/cm^2 which leads to a total package thermal resistivity of 0.25 K-cm^2/W. This resistivity is significantly less than standard power modules, which are 0.6 – 3.3 K-cm^2, and on par with the best modules [2]. At 100 W/cm^2 and 200 W/cm^2 the chip temperature rise was 25.3 °C and 50.2 °C, respectively and similar thermal resistivity.

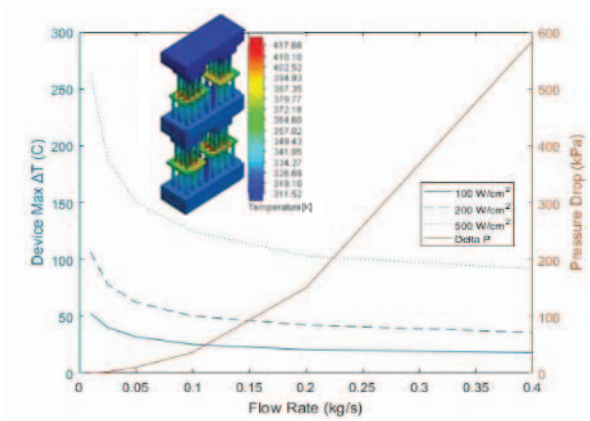

Fig. 11. Plot showing the tradeoff between device temperature (blue) versus pressure drop (red) for various flow rates and power dissipations. Inset shows temperature profile for 500 W/cm2 heat dissipation and 0.1 kg/sec.

Fig. 11 shows the tradeoff between pressure drop and device temperature for varying heat fluxes and flow rates. The plot shows that for a heat flux of 500 W/cm2, the optimal flow rate for this module is around 0.1 kg/sec. This is the point at which any further increase in flow rate would equate to minimal reduction in chip temperature rise for a significant increase in pressure drop. Flow rates less than 0.1 kg/sec are in a regime where small variations in flow rate can result in large fluxuations in device temperature.

The pressure drop profile on a center cut through the package is shown in Fig. 12a for 0.1 kg/sec mass flow rate. The inlet and outlet are labeled on Fig. 12 and are located at the upper right and lower right corners, respectively. The majority of the pressure drop occurs at the outlet of the package and in the 180 degree bend when the fluid goes from the upper to lower sections. Future iterations will eliminate the outlet constrictions as well as improving on the bend to reduce pressure drop. At 0.1 kg/sec the pressure drop is acceptable for most Army applications.

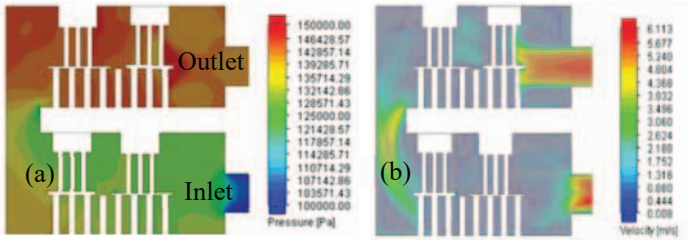

Fig. 12. (a) Pressure contours for 0.1 kg/sec mass flow rate and (b) Velocity vectors for 0.1 kg/sec mass flow rate.

Fig. 12b shows a well distributed velocity profile around all the devices at 0.1 kg/sec. Some flow stagnation is observed behind some pin fins which can reduce heat transfer. Future fin optimizations can help to alleviate this.

In addition to the thermal analysis, SOLIDWORKS was used to evaluate the thermal stress in the package based on a zero stress temperature of 150 ºC and the operating temperatures for 0.1 kg/s and 500 W/cm^2. Fig. 13 shows the von Mises stress for the active surfaces of the diodes and MOSFETs. The max stress is 157 MPa, which is localized at the corner of one of the square shaped fins on the upper MOSFET. The average stress is 53.9 MPA. Both values are significantly below the ultimate strength in tension of 310 MPa.

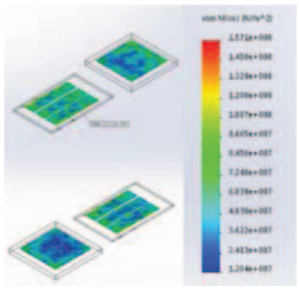

Fig. 13. Von Mises stress contours for 500 W/cm^2 power dissipation per chip and 0.1 kg/sec mass flow rate.

CONCLUSIONS

This report has shown the first power module which stacks devices with an integrated heat sink. This power module has eliminated the three primary failure locations from the module (wirebonds, large area contacts including die attach and substrate attach, and the DBC) leading to a more reliable module. Stress analysis has shown the maximum von Mises stresses are 50% less than the ultimate strength in tension of SiC. The thermal-fluidic modeling has shown a package thermal resistance of 0.25 K-cm^2/W, which is significantly lower than standard power modules and on par with the best power modules. Challenges that were overcome during fabrication include accounting for various chip thicknesses, repeatable alignment and bonding, and ensuring quality electrical and thermal contacts. The cost of such a module is expected to be reduced due to the elimination of the expensive DBC and size reduction. This module focused on a co-designed approach which emphasizes multi-functionality of all components. The MFCs are a key enabling feature of this module which act as thermal, mechanical, and electrical contacts interfacing with the SiC devices. This module has included additional multi-functional features including (1) eliminating the solid dielectrics and using the dielectric fluid as both the cooling fluid and dielectric and (2) the exterior plastic acts as both the heat sink enclosure and the module housing. This paper has presented both a new power module configuration as well as a new approach to power module design.

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