HAUTE ÉCOLE D'INGÉNIERIE ET DE GESTION DU CANTON DE VAUD

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Formal verification
Verification of a arithmetic logic unit (ALU)
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Module to verify

We are interested in the verification of an arithmetic logic unit able to manage 8 operations, on two input vectors.
A generic parameter `SIZE` allows to define the operands size.
The input/output are :

Nom	Taille	Description
`a_i`	SIZE	First operand
`b_i`	SIZE	Second operand
`mode_i`	3	Operation mode
`c_o`	1	Carry out
`s_o`	SIZE	Result

The expected results are the following :

mode_i	**s_o**	**c_o**
`"000"`	`a_i+b_i`	carry out
`"001"`	`a_i-b_i`	carry out
`"010"`	`a_i or b_i`	undefined
`"011"`	`a_i and b_i`	undefined
`"100"`	`a_i`	undefined
`"101"`	`b_i`	undefined
`"110"`	`s_o(0)= '1' when a_i=b_i else '0'`	undefined
`"111"`	`0`	undefined

The mathematical operations are computed with unsigned numbers.
A second generic parameter `ERRNO` allows to inject errors in the design. Its behavior is the following :

1. When in the $[0, 15]$ interval the result is valid ;
2. When in the $[16, 24]$ interval, the result is unvalid.

This generic parameter allows to test your assertions by trying various `ERRNO` values
You can modify its value in the `alu.sby` file.