

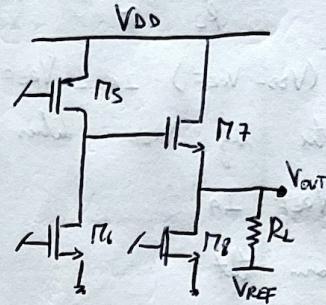
Output Stages

→ Class - A (Transistors Are Always Active)

The right buffer stage is the source follower, where we set the output node at $V_{DD} - V_{EE}$ in order not to have a current into R_L when no input signal is applied ($V_{REF} = \frac{V_{DD} - V_{EE}}{2}$)

Let's assume to have a positive signal at the gate of M_7 . The gain of the stage is:

$$\frac{V_{OUT}}{V_{G,7}} = \frac{R_L}{R_L + \frac{1}{g_{m,7}}}$$



where $g_{m,7}$ is NOT constant, since it depends on the current value.

As $V_{G,7} \uparrow$, the current $I_7 \uparrow$, so $g_{m,7} \uparrow$ and overall $\left(\frac{V_{OUT}}{V_{G,7}}\right) \uparrow$. On the negative swing instead, $I_7 \downarrow$ and M_7 may turn off. In order to avoid the output clipping we need to have

$$R_L \cdot I_8 \geq \Delta$$

being Δ the peak (negative) voltage at the output.

This stage is also adopted in power AMPLIFIERS, as we may compute the

$$\text{POWER EFFICIENCY } \eta = \frac{V_p^2 / 2R_L}{I_8 V_{DD}} \stackrel{\Delta}{=} \frac{\text{POWER DELIVERED TO THE LOAD}}{\text{AVERAGE POWER DRAWN FROM SUPPLY}}$$

assuming that no clamping takes place, and that

$$\begin{cases} V_{DD} = 2V_{REF} \\ V_p \leq V_{REF} \end{cases}$$

$$\Rightarrow \eta \leq \frac{V_{REF}^2}{2R_L I_8 2V_{REF}} \leq \frac{V_{REF}^2}{4 \cdot V_{REF} \cdot V_{REF}} = \frac{1}{4}$$

→ Class - B (Push - Pull)

In order to avoid static power consumption, we may substitute the current generator with a pmos follower, so that

- on the positive swing the nmos turns on while the pmos is off
- on the negative swing the pmos turns on while the nmos is off
- for $-V_T \leq V_{G,7} - V_{REF} \leq V_T$ we have a dead zone that causes Crossover Distortion

therefore we have MORE DISTORTION, but BETTER POWER EFFICIENCY.

- (40) • The power delivered to the load is again $\frac{V_p^2}{2R_L}$ mighty distortion
- On the positive swing a current flows from V_{DD} to V_{REF} , whose mean value is
- $$I_A = \frac{1}{T/2} \int_0^{T/2} \frac{V_p}{R_L} \sin\left(\frac{2\pi}{T}t\right) dt = \frac{V_p}{R_L} \cdot \frac{2}{T} \frac{T}{2\pi} \cdot \left[\cos\left(\frac{2\pi}{T}t\right)\right]_0^{T/2}$$
- $$= \frac{V_p}{R_L} \cdot \frac{1}{\pi} \cdot 2 = \frac{2}{\pi} \frac{V_p}{R_L}$$

$$\Rightarrow \bar{P} = (V_{DD} - V_{REF}) \cdot I_A = V_{REF} \cdot I_A$$

On the negative swing V_{REF} delivers the same current towards ground, so again

$$\bar{P} = V_{REF} \cdot I_A.$$

Remembering again that

$$\begin{cases} V_p \approx V_{REF} \\ V_{DD} = 2V_{REF} \end{cases}$$

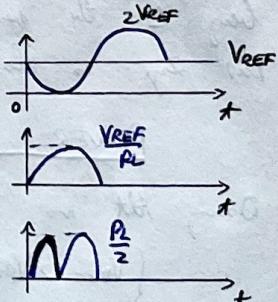
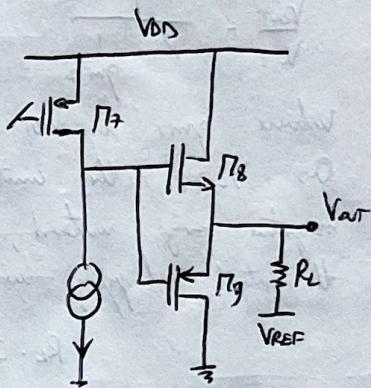
$$\eta \leq \frac{\frac{V_{REF}^2}{2R_L}}{V_{REF} \cdot 2 \cdot \frac{V_{REF}}{\pi} \cdot \frac{V_{REF}}{R_L}} = \frac{\pi}{4} \approx 78\%$$

We have that across each transistor

$$\begin{cases} V_{DS,max} = 2V_{REF} \\ I_{DSK} = \frac{V_{REF}}{R_L} \end{cases} \quad (\text{neglecting the overdrive})$$

$$P(t) = \frac{V_{REF}}{R_L} \sin(\theta) V_{REF} \left[1 - \sin(\theta) \right]$$

$$P_{max} = \frac{V_{REF}^2}{4R_L} \quad \left[\theta = \frac{\pi}{6} \right] \quad \left(\text{half of the maximum power delivered to the load!} \right)$$



→ CLASS A-B

To limit distortion due to the dead-zone of the push-pull stage, we shall bias the transistors M8 and M9 at the edge of their full conduction.

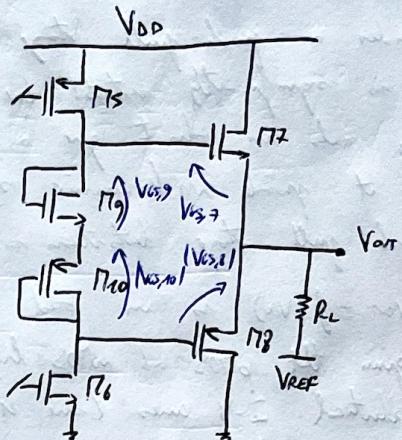
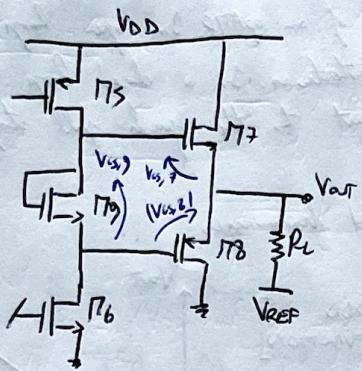
We may implement this voltage shifter by using a diode:

$$V_{GS,7} + V_{GS,8} = V_{GS,9}$$

$$\sqrt{\frac{I_7}{k_7}} + V_{T,IN} + \sqrt{\frac{I_7}{k_2}} + V_{T,P} = \sqrt{\frac{I_7}{k_6}} + V_{T,IN} \Rightarrow I_7 = \left(\frac{\sqrt{I_7/k_6} - V_{T,P}}{\sqrt{I_7/k_6} + \sqrt{I_7/k_2}} \right)^2$$

{DEPENDENT ON ABSOLUTE VALUES (BAD)!}

42



We may use the TRANSLINEAR PRINCIPLE by adding the complementary transistors, in such a way that the NBL in the $M_7 - M_8 - M_9 - M_{10}$ loop is depending only on V_{GS} terms and we can control more easily the currents.

$$\sqrt{\frac{I_7}{k_7}} + \sqrt{\frac{I_7}{k_8}} + V_{Tm} + V_{TFP} = \sqrt{\frac{I_9}{k_9}} + \sqrt{\frac{I_9}{k_{10}}} + V_{Tn} + V_{TFP}$$

$$\downarrow \\ I_7 = I_C \left(\frac{\sqrt{1/k_9} + \sqrt{1/k_{10}}}{\sqrt{1/k_7} + \sqrt{1/k_8}} \right)^2$$

So we can properly tailor the current (static one) in M_7 and M_8 by using the transistors M_9 and M_{10} .

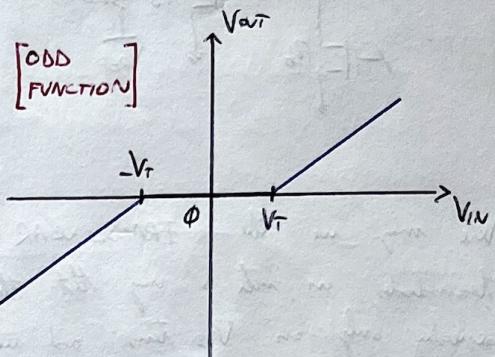
$\begin{cases} \text{BIAS OF THE OUTPUT STATE} \Rightarrow \text{not by } R_{L\min} \text{ (avoid clipping)} \\ \text{SIZES OF } M_9 \text{ AND } M_{10} \Rightarrow \text{not by } I_2 \end{cases}$

DISTORTION AND FEEDBACK

Let's consider a push-pull stage or output stage of an opAMP. In open-loop operation, the output is significantly distorted due to crossover distortion. In a closed loop configuration, the feedback acts in such a way to give a pre-distorted signal to the push-pull stage and thereby minimize harmonic signals.

In a push-pull stage distortion is dominated by odd harmonics:

→ $V_{out} = f(V_{in})$ is an odd function,
given that pMOS and nMOS have
identical I-V curves (same n
and same V_T)



→ if we drive the stage with

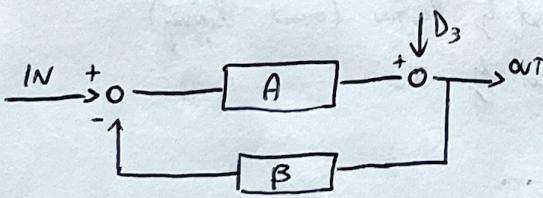
$$v_{in} = A_0 \sin(\omega t)$$

the signal out though T_{L2} is a replica of the signal out though T_{L1}
but with a $\frac{1}{2}$ shift, $\approx (\pi = \frac{2\pi}{\omega T})$

$$i_1(t) = A_0 + A_1 \sin(\omega_1 t + \phi_1) + A_2 \sin(\omega_2 t + \phi_2) + A_3 \sin(\omega_3 t + \phi_3) + \dots$$

$$i_2(t) = A_0 + A_1 \sin(\omega_1 t + \phi_1 + \pi) + A_2 \sin(\omega_2 t + \phi_2 + 2\pi) + A_3 \sin(\omega_3 t + \phi_3 + 3\pi) + \dots$$

$$i_L = i_1 - i_2 = 2A_1 \sin(\omega_1 t + \phi_1) + 2A_3 \sin(\omega_3 t + \phi_3) + \dots$$



$$\text{PRE-DISTORTION} \\ -D_3^{out} \cdot A \cdot \beta + D_3 = D_3^{out}$$

$$D_3^{out} = \frac{D_3}{1 + A\beta} \Rightarrow \frac{D_3^{out}}{D_3} = \frac{1}{1 + \text{loop gain}}$$

