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ELECTRONIC SYSTEMS

2021-22 academic year
prof. Franco ZAPPA

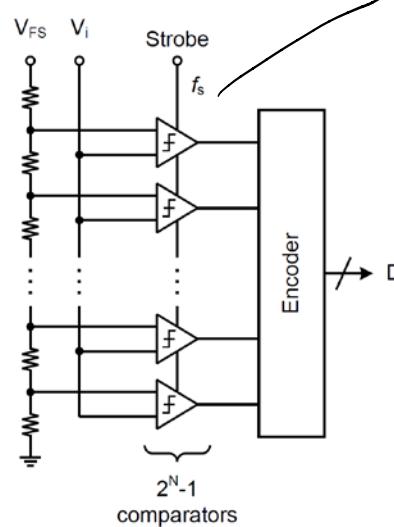


- More speed and/or reduced complexity
- " " " " serial (pipeline) processing
- " " " " parallel processing



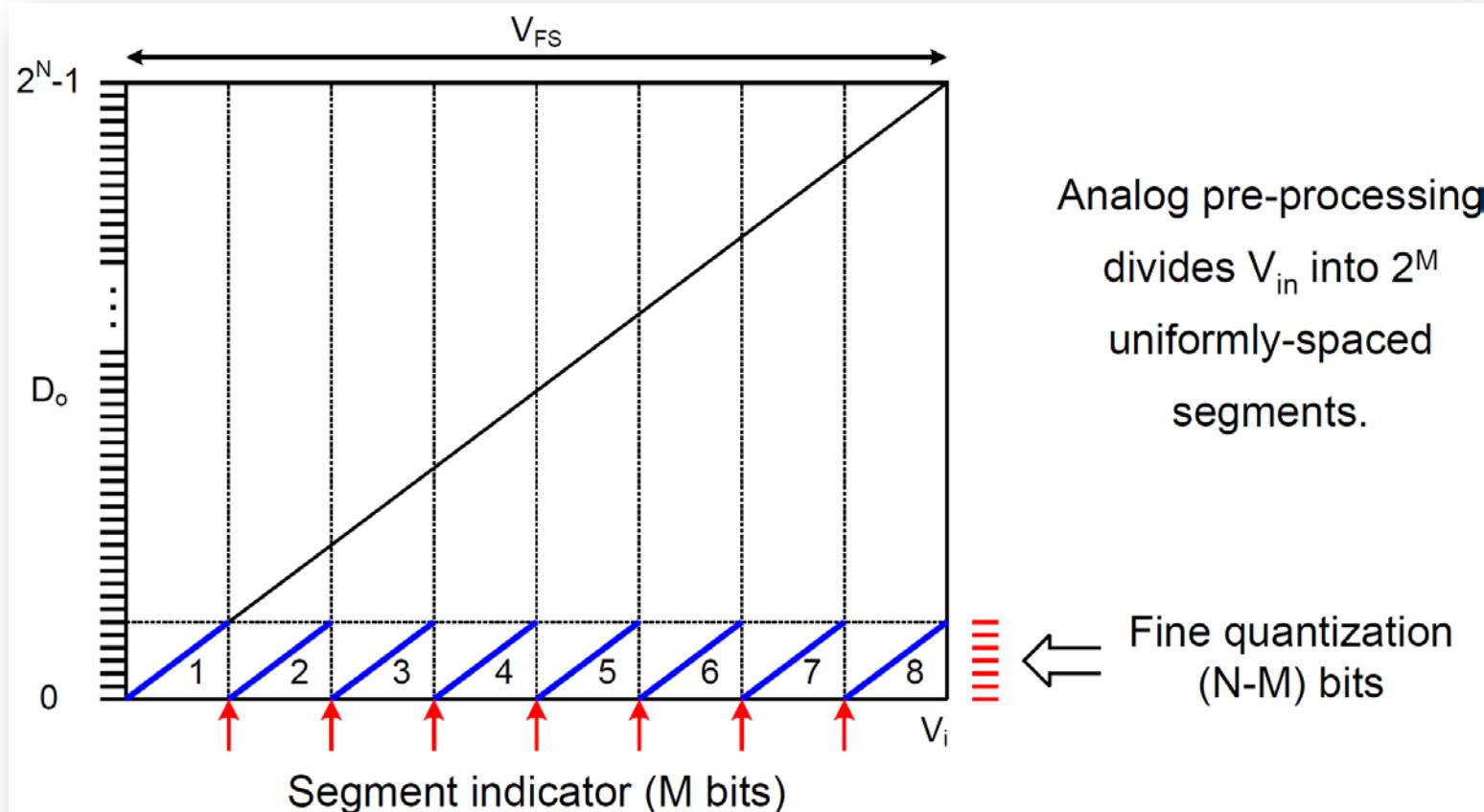
Subranging ADC

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ho tutti i Comparatori elementati in serie
e' un peccato perché da metà scala siano metà comparatori spenti e metà zonosi
Allora posso usare solo dei comparatori per vedere 2 alle livello
ho i segnali e poi in base a questo devo decidere se sono
comparatori attivare.

Therefore... **segmented quantization**

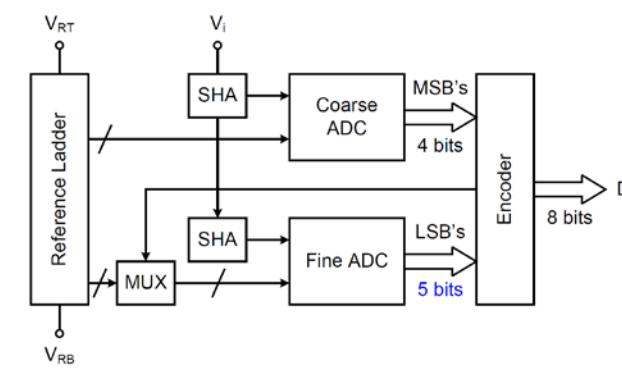


In standard Flash ADCs, comparators near V_{in} are important for fine conversion, hence low efficiency



Subranging ADC

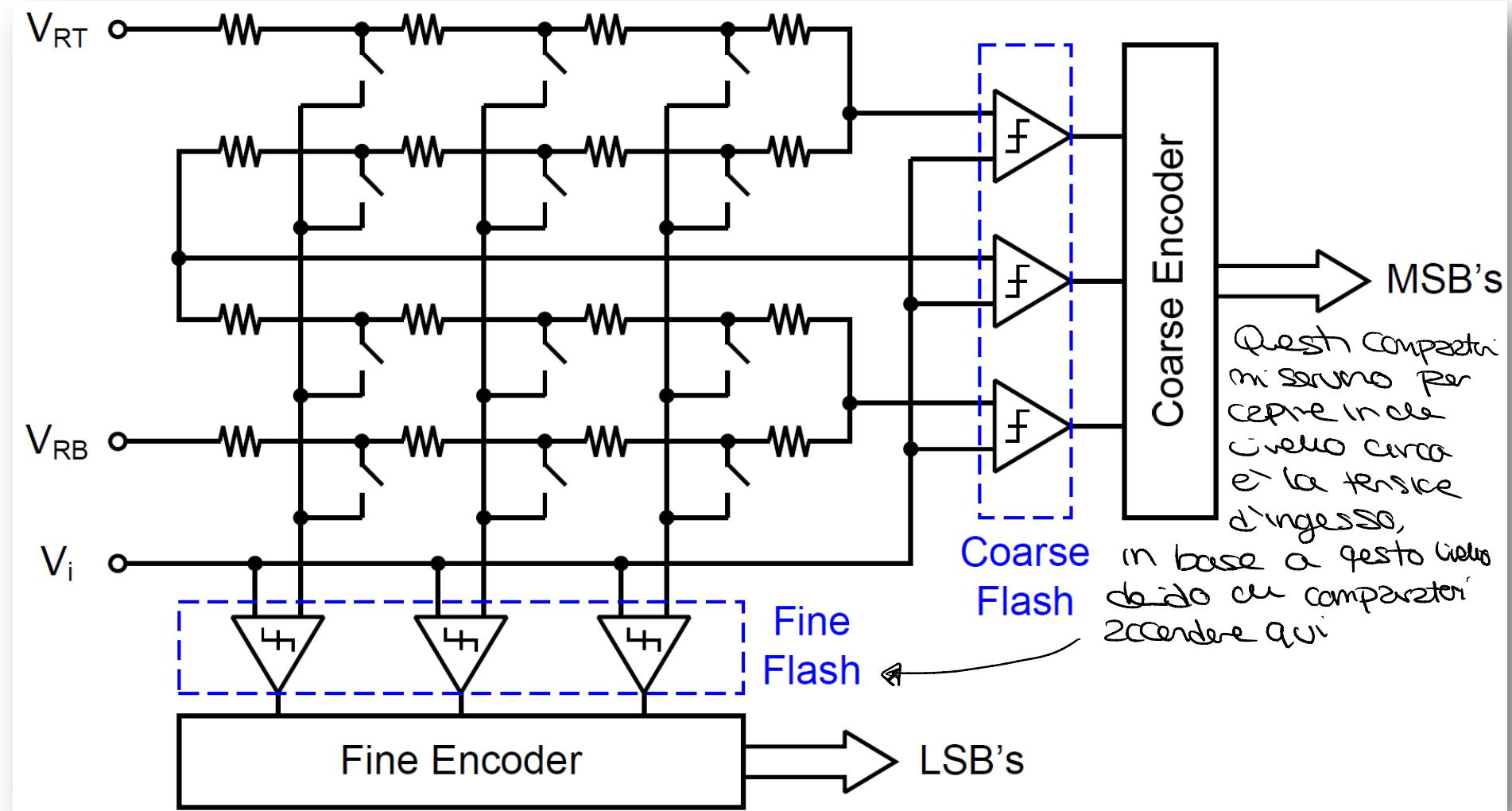
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Redundancy in Fine ADC provided by over- and under-range comparators

Quindi per un ADC da 8 bit non ho bisogno di 256 comparatori ma ce ne servono solo 16 + 16.

Questo ADC è più veloce di quello flash.



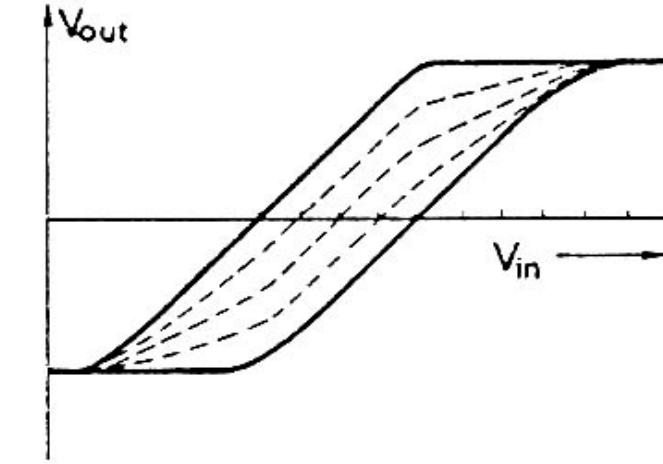
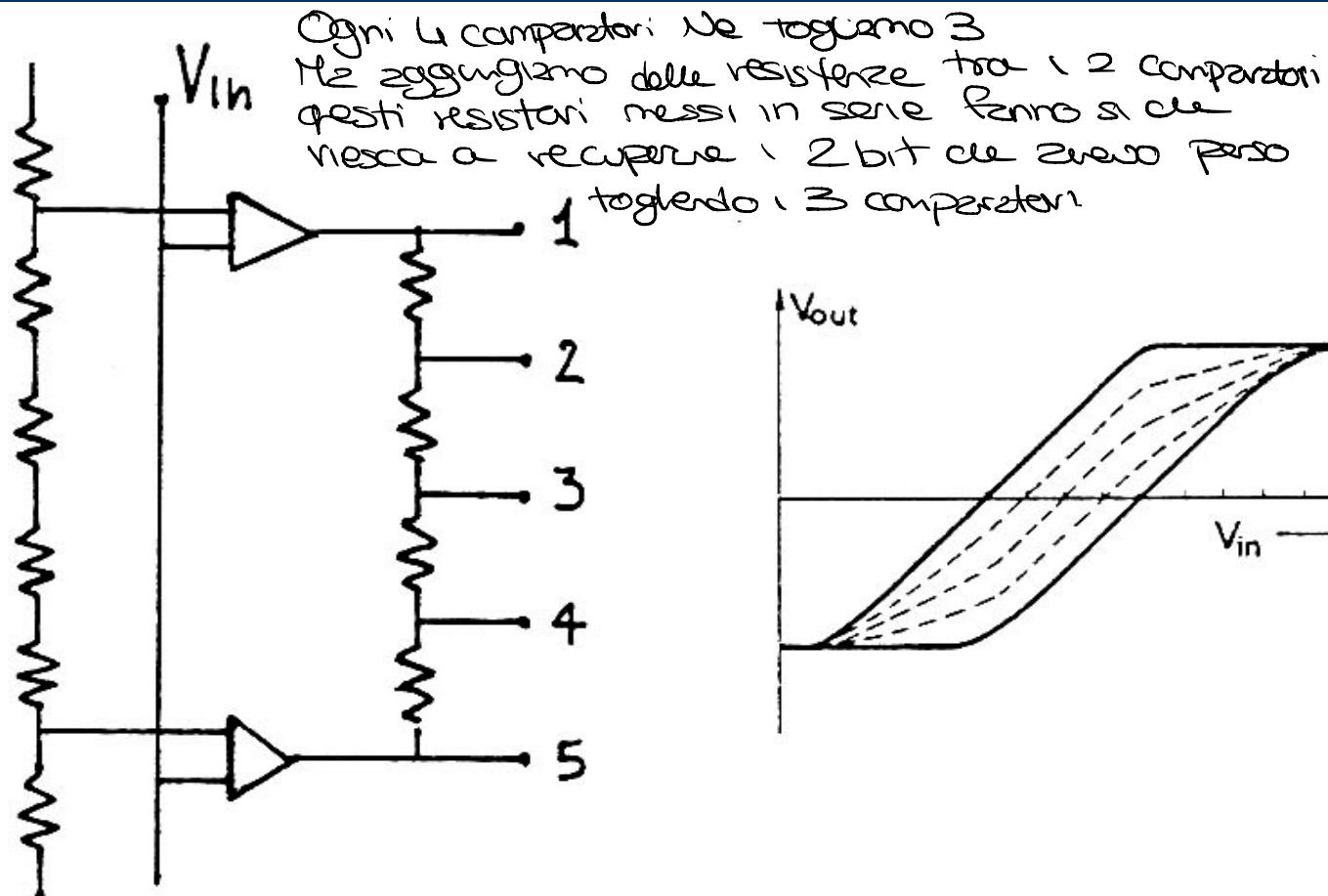
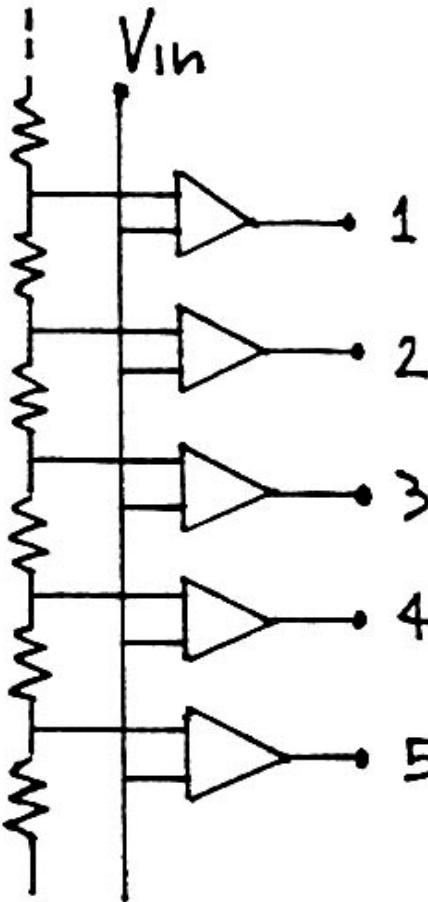
- Coarse comparators are connected to the coarse reference ladder taps
- After getting MSBs, the fine ladder taps are enabled and fine LSB are computed



Interpolation Flash ADC

Un altro modo per ridurre l'area degli ADC

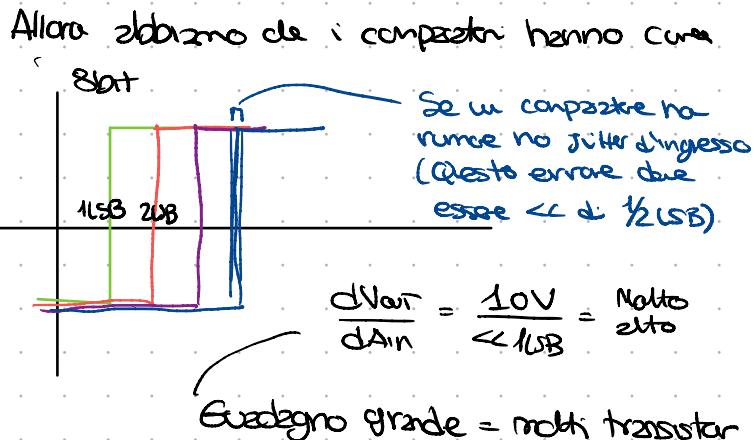
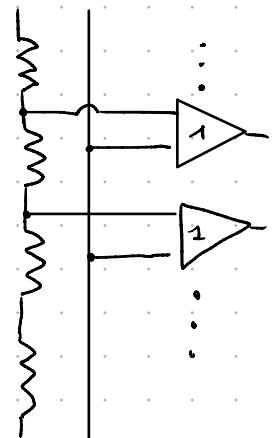
Standard ADC
flash.



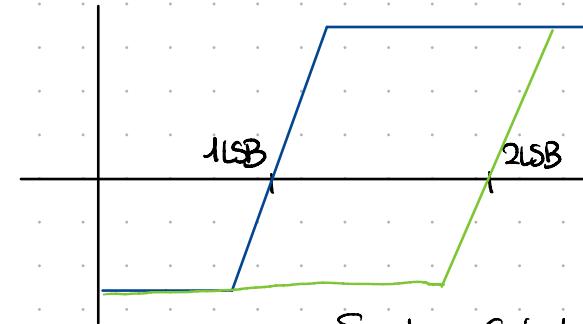
Example, for an 8 bit interpolation ADC:

- instead of 256 comparators, it needs just 64 ($\frac{3}{4}$ are removed)
- huge reduction of silicon area, power dissipation, input stray capacitance, layout
- improved dynamic performances (settling time, speed, ...)

Dato uno standard Flash ADC abbiamo che:

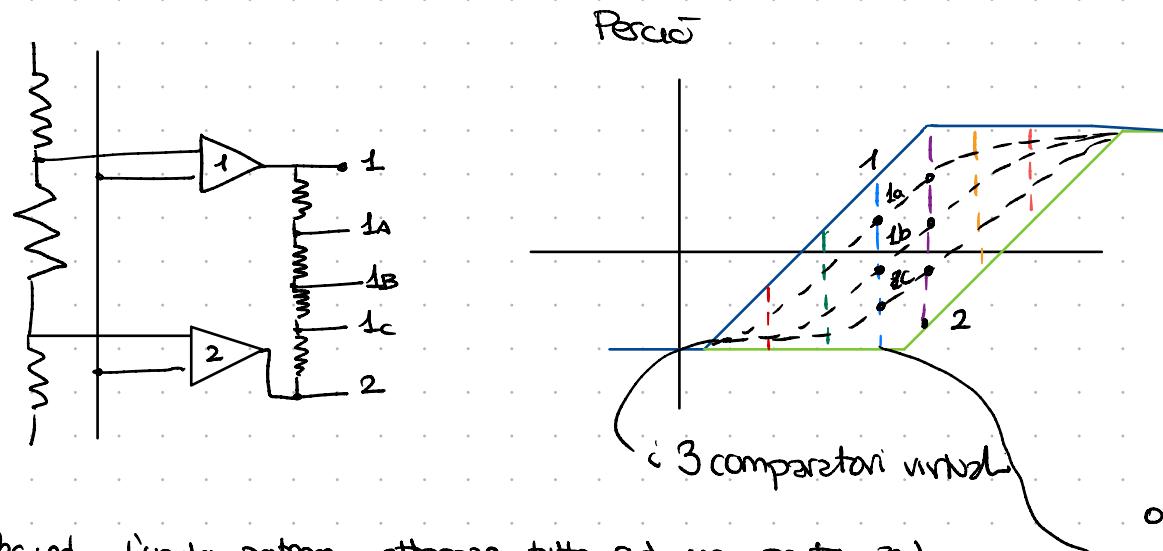


Se invece usiamo un 6 bit ho che



Se ho 6 bit posso saltare certe celme e quindi posso usare meno transistor.

Se tolgo 3 comparatori e' come avessi 6 bit



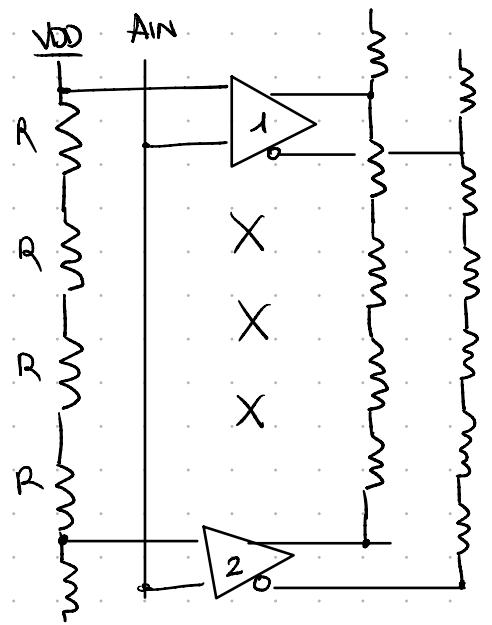
Per vedere l'uscita potremo attaccare tutto ad una porta AND con un pin sompresa 1. Per facilità per comandarla possiamo usare comparatori che vanno da 0 a VDD e quindi avere threshold per la AND 2.5V. Esistono anche i comparatori con 2 uscite una non invertente e una invertente, il vantaggio è di abbattere 2 output di cui muoversi in verso opposto. Possono usare questi "comparatori" in questo ADC per fare:

Uso 3 comparatori con basso guadagno

$$G = \frac{dV_{out}}{dA_{IN}} = \frac{10V}{\frac{5}{2^8} \cdot 4}$$

Questo fa sì che con le resistenze in mezzo ho che posso vedere il comportamento degli altri 3 comparatori virtuali.
Per sapere se ho che i 3 "comparatori" sono on o off basta che veda se sono sopra o sotto lo zero per quel valore

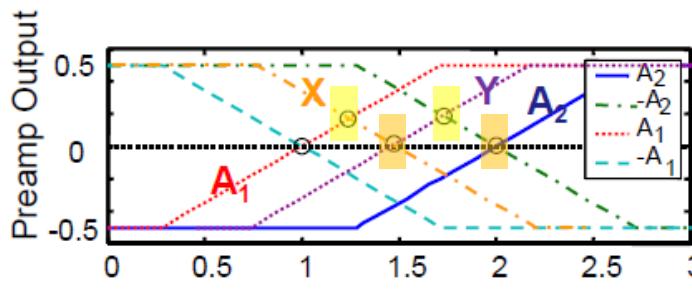
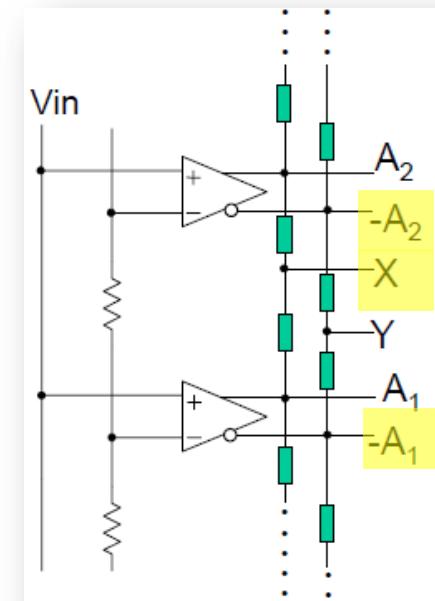
Esempio 1 e 1a sono ON 1b, 1c e 2 sono OFF



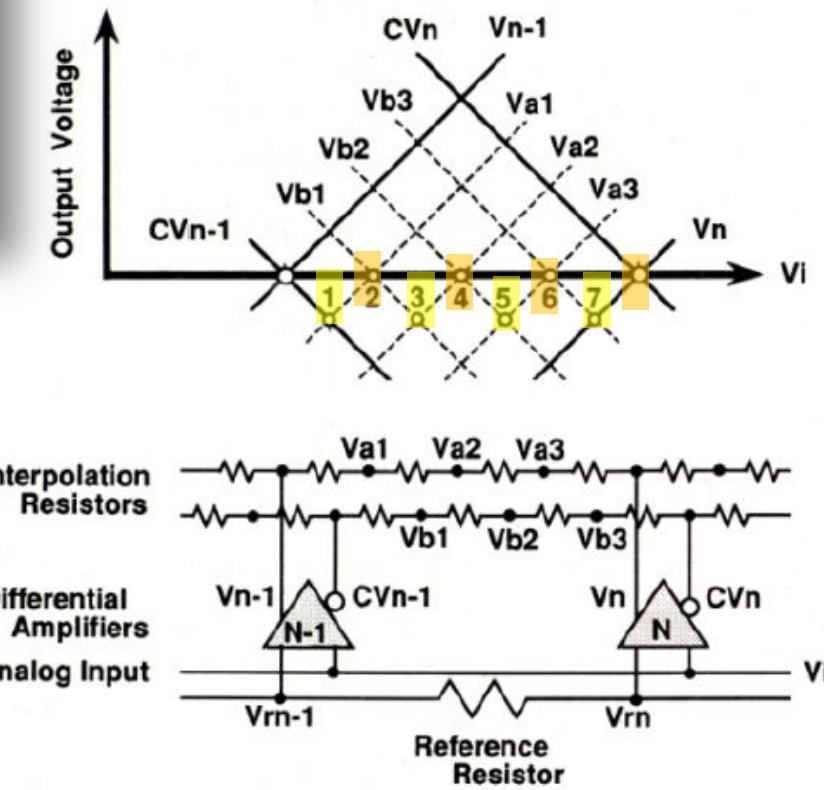
Grazie alla doppia uscita di tensione abbiamo che possiamo guadagnare 2 bit in più se all'uscita non usiamo semplicemente porte logiche ma anche comparatori.



Interpolation Flash ADC: higher order interpolation



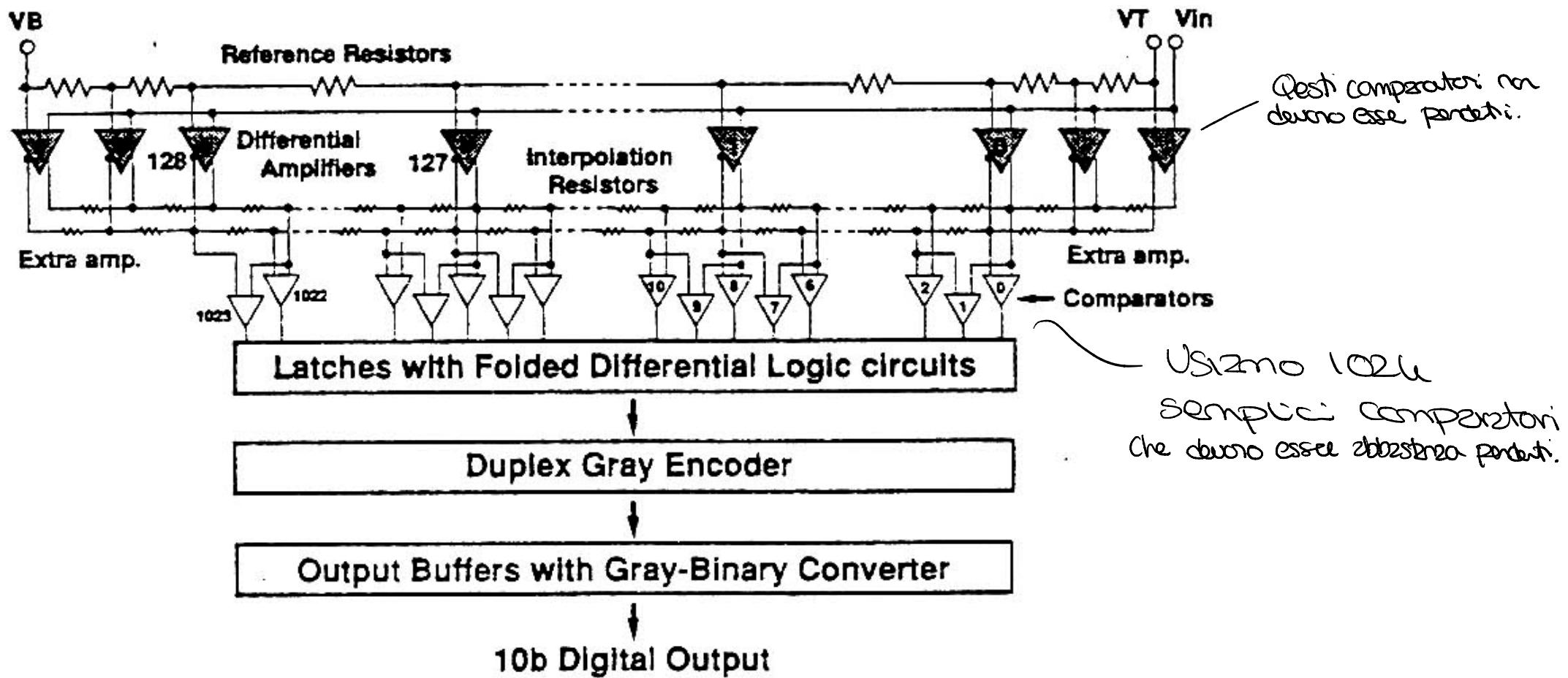
2 sets of interpolation resistors
to get 2 plus 2 extra intermediate points,
hence 2 extra bits!



- Resistors produce additional levels
 - With 4 resistors per side, the “interpolation factor” $M=8$
→ extra 3bits
 - ($M \rightarrow$ ratio of latches/preamps)
- Ref: H. Kimura et al., “A 10-b 300-MHz Interpolated-Parallel A/D Converter,” JSSC April 1993, pp. 438-446



Interpolation Flash ADC



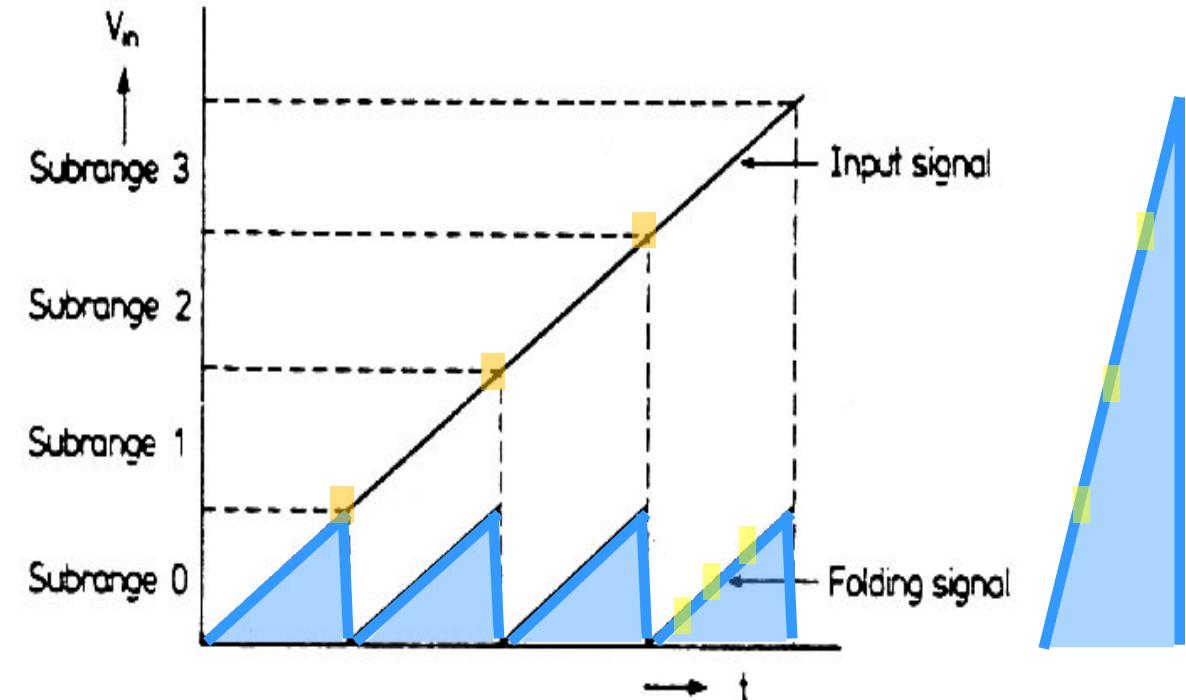
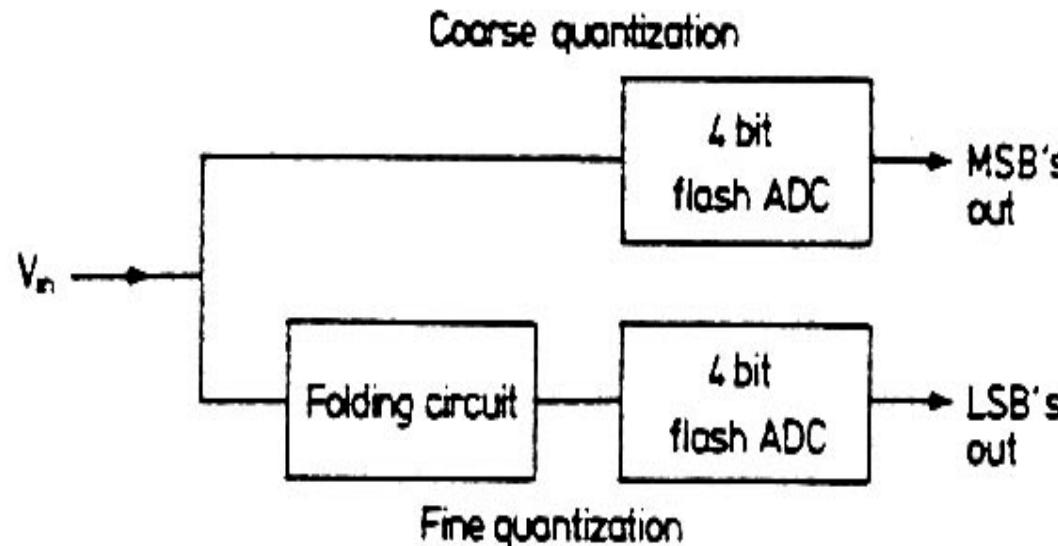
Example of a 10bit ADC with 300Msps:

- 128 differential OpAmps ($G=10$), each with 4+4 resistors and 8 comparators
- same total number of comparators ($128 \cdot 8 = 1024$), hence same area and dissipation
- but advantages for a reduced C_{in} ($128/1024$), better DNL ($V_{osOpAmp}/8$ e $V_{osComp}/Gain$)



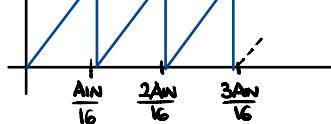
Folding Flash ADC

Se ho solo 2 conversioni a 6 bit ma voglio un uscita a 8 bit come faccio?



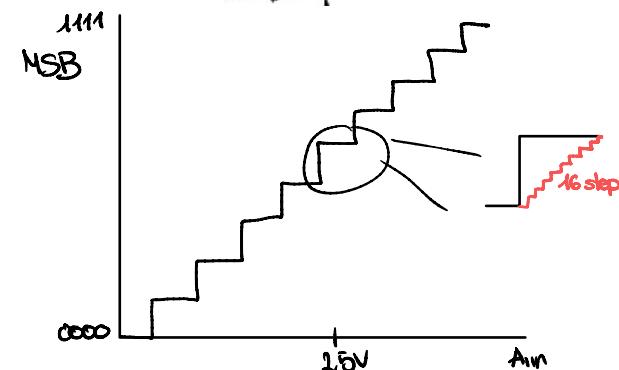
30 comparators instead of 256

MSB sono quelli dati dal convertitore a 6bit, poi per avere 8 bit d'uscita devo dividere ogni step per 16 cosa volto a 30 comparatori invece di 256.
Il folding avviene cioè fissando dei

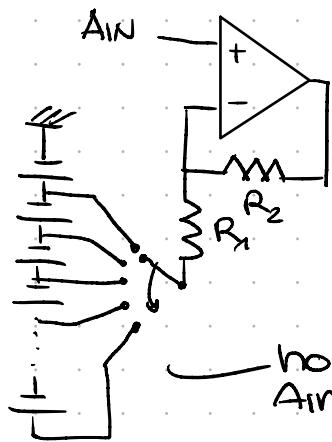


Analog pre-processing aimed at obtaining separately:

- the MSBs through a low-resolution flash ADC)
- the LSBs through a “folding” analog circuit followed by (amplification and) ADC



Nella rettifica la cosa difficile da fare è il folding circuit.
Possiamo vedersi come

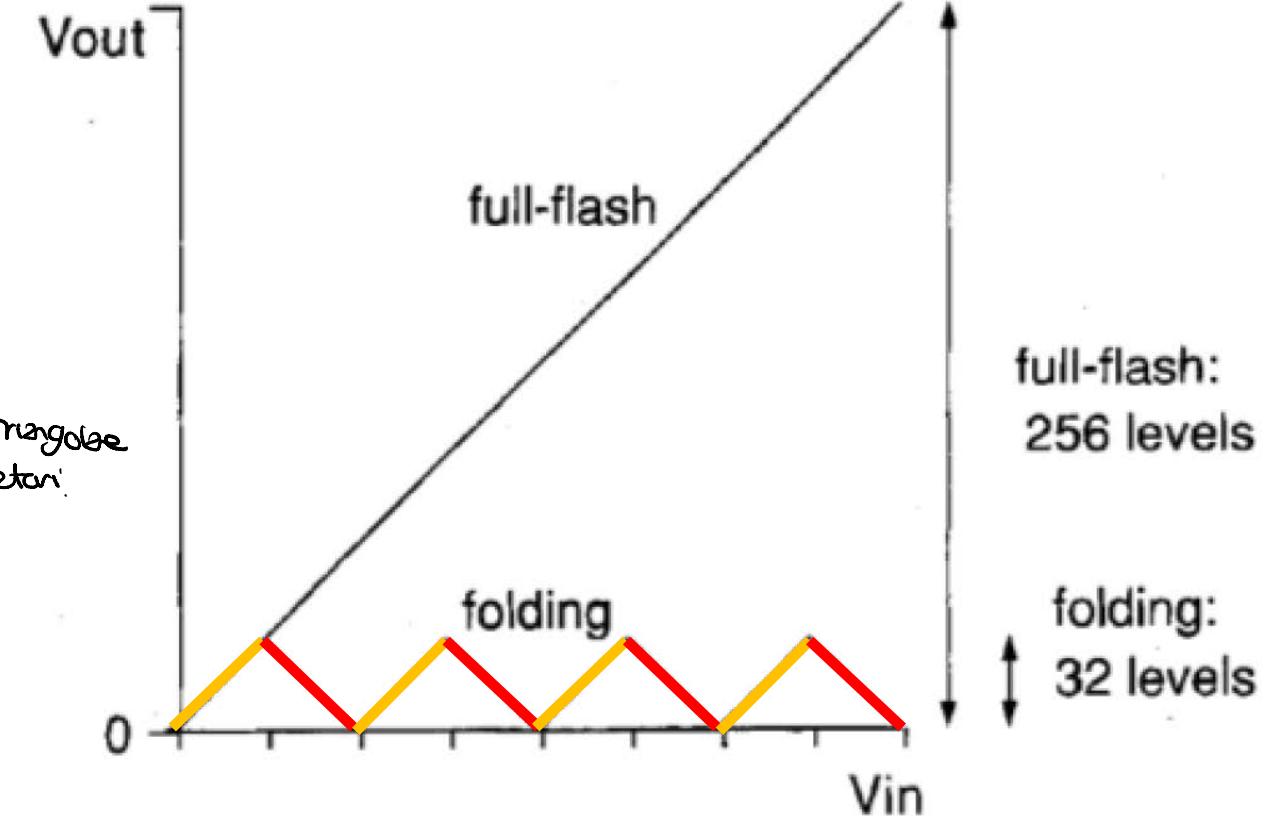
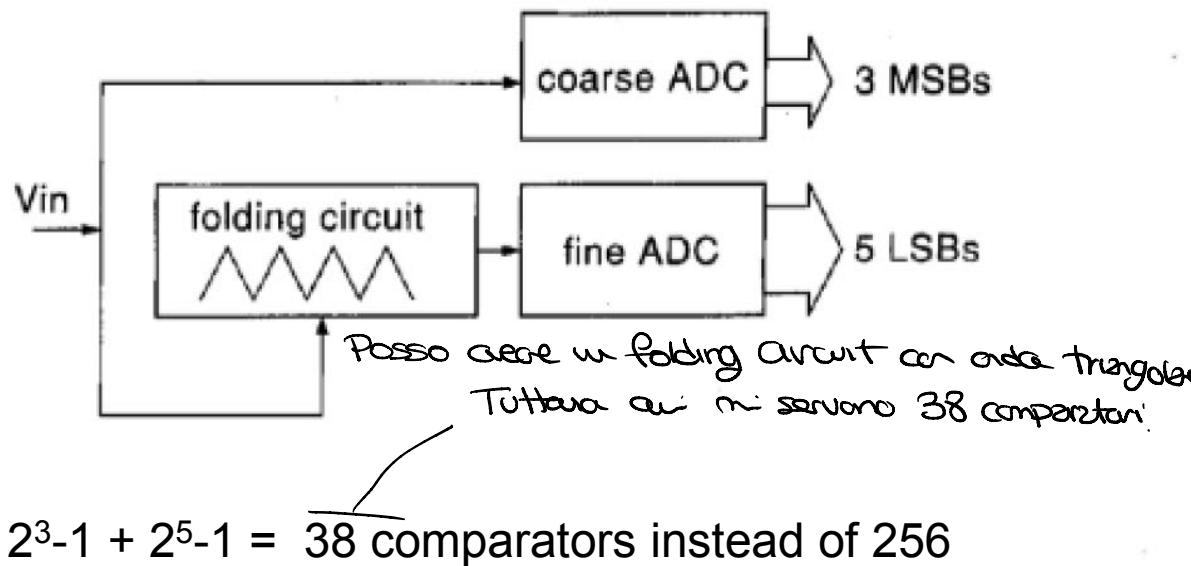


ho 16 batterie e scelgo a quale collegarmi dipendente dal veloce di Ain.



Folding Flash ADC

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Different ways of folding

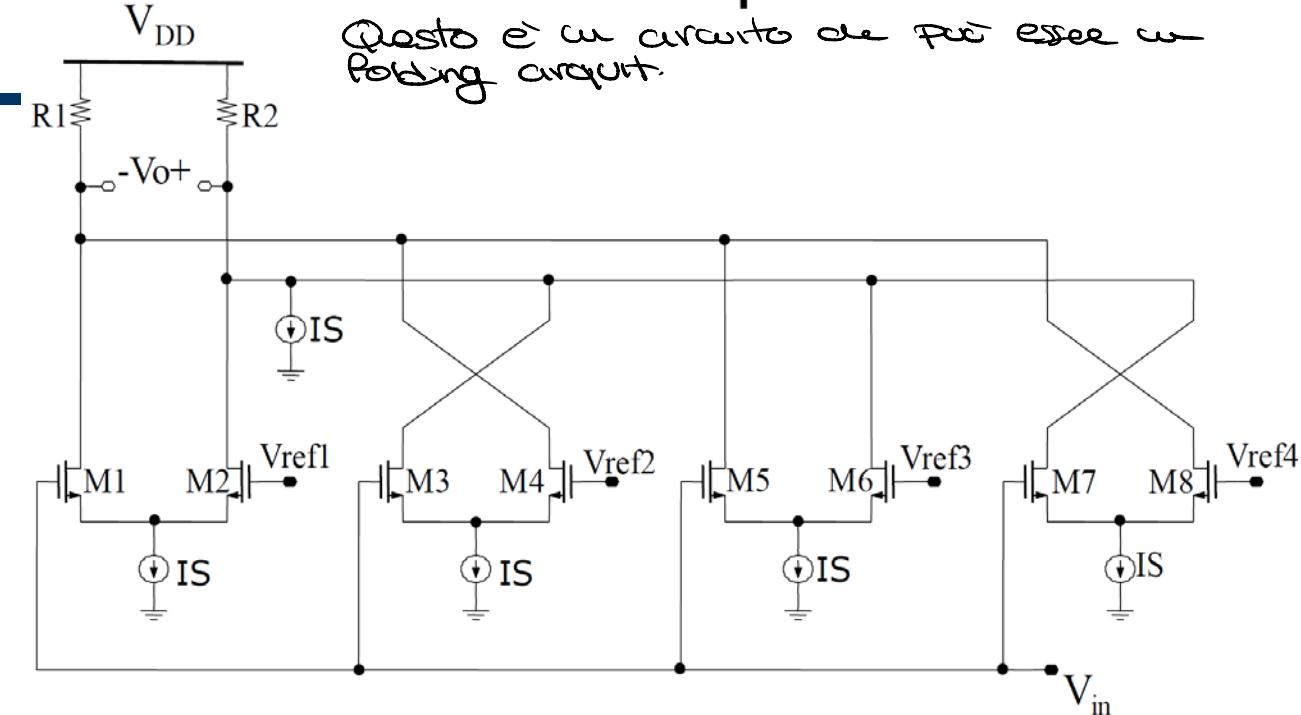


Folding Flash ADC

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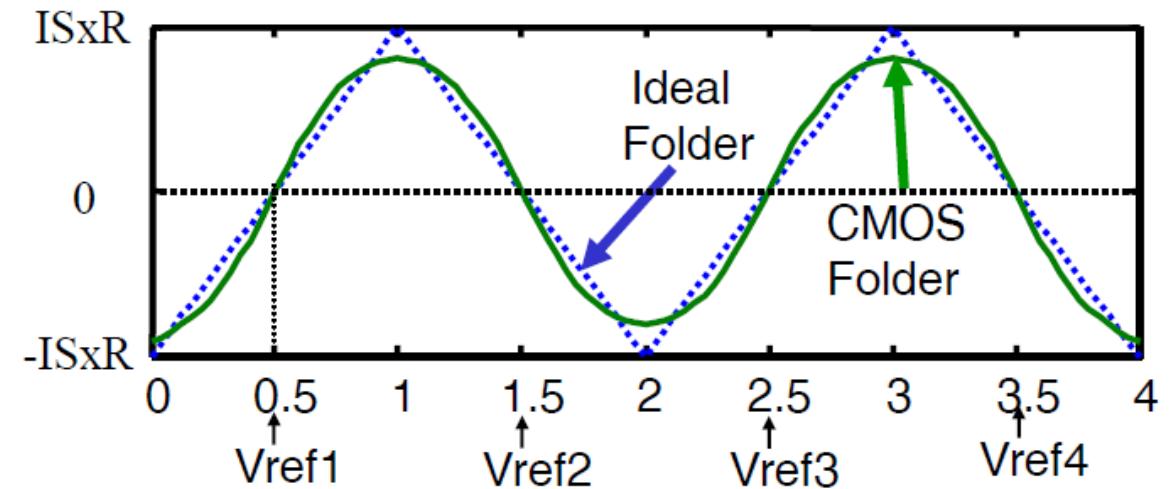
Example of how to generate folds:

- via source-coupled pairs
- with $V_{ref1} < V_{ref2} < V_{ref3} < V_{ref4}$
- as V_{in} changes, only one of M1, M3, M5, M7 is on



Questo è un circuito che può essere un folding circuit.

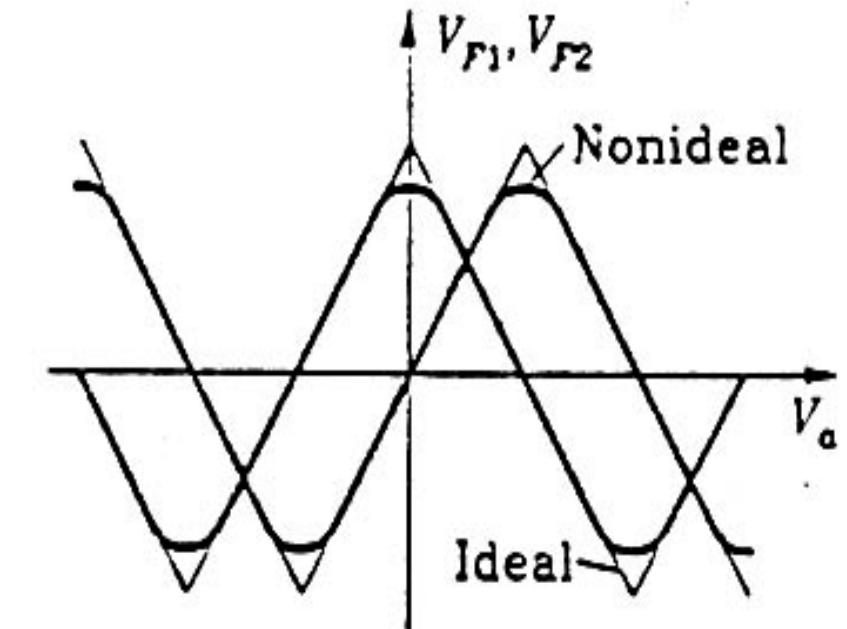
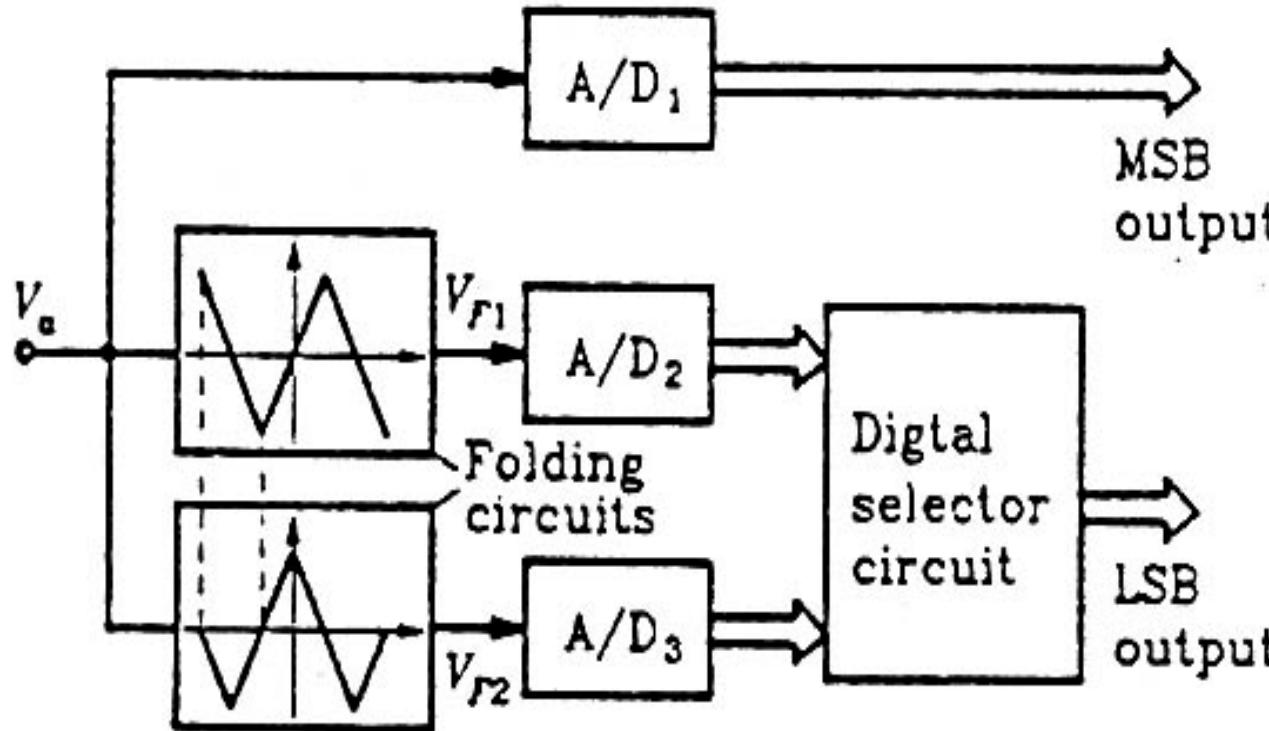
- Actually, curves are rounded,
- therefore, accurate only at zero-crossings
- In fact, most folding ADCs do not use the folds, but only the zero-crossings!





Folding Flash ADC

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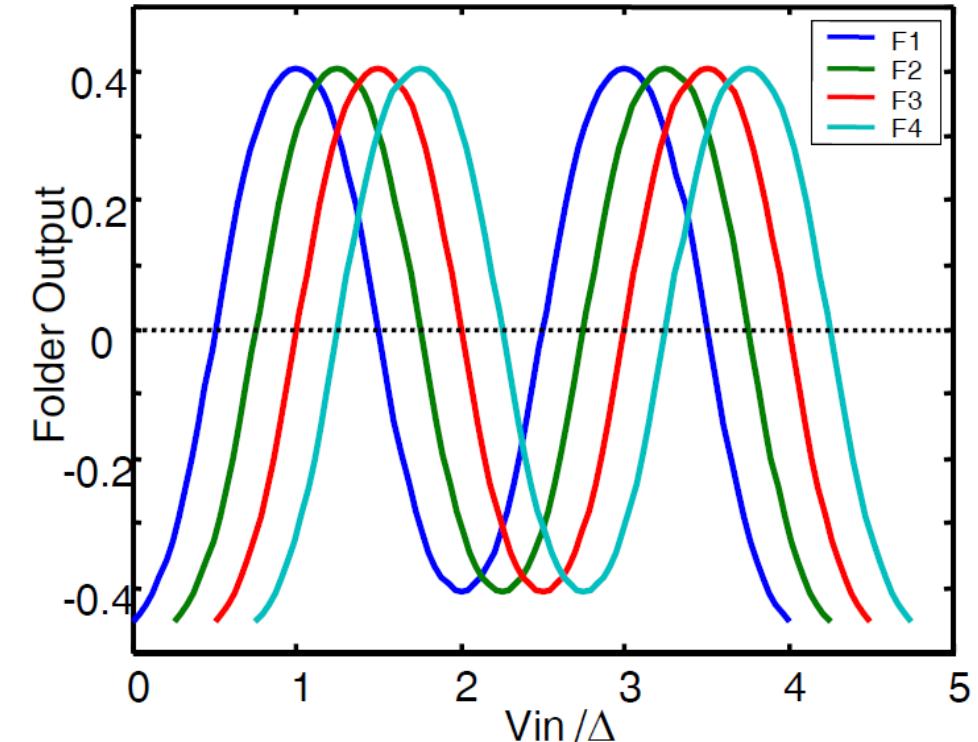
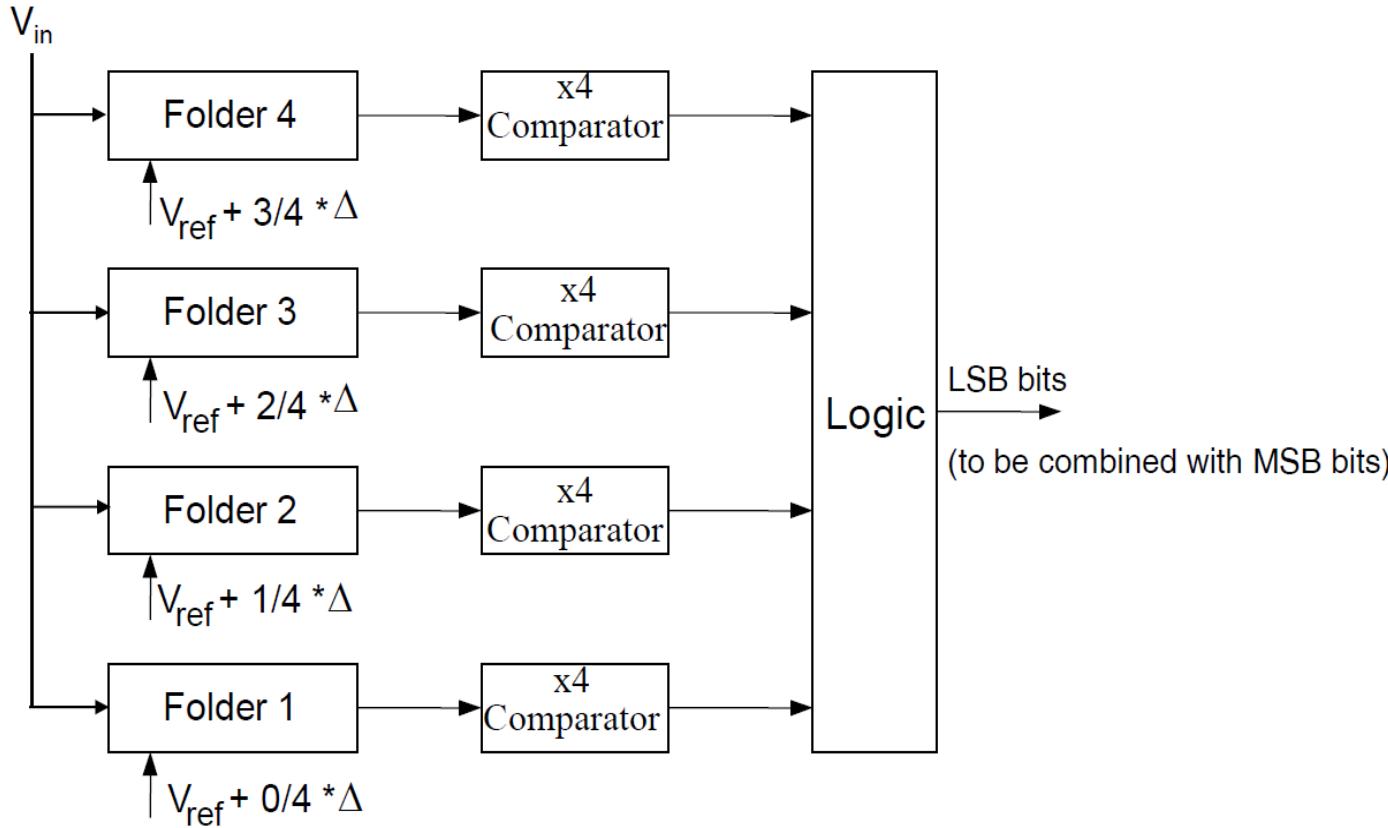


Example of a double folding circuit, in order to avoid non idealities of folded edges
... other folding shapes can be used...



Folding Flash ADC

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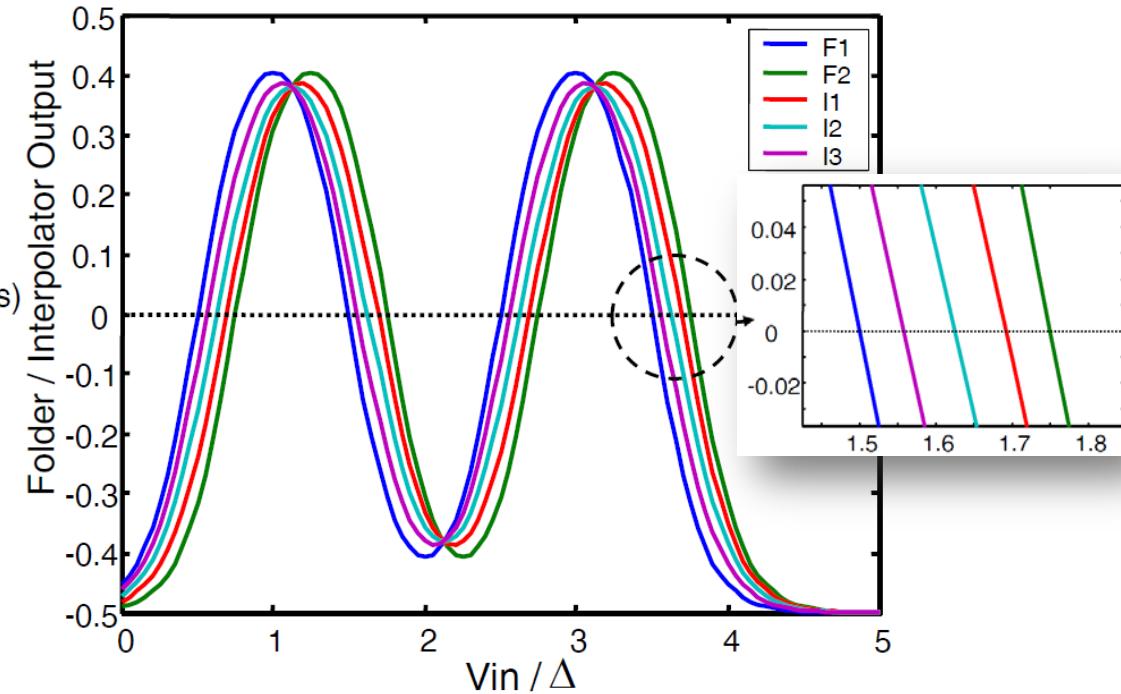
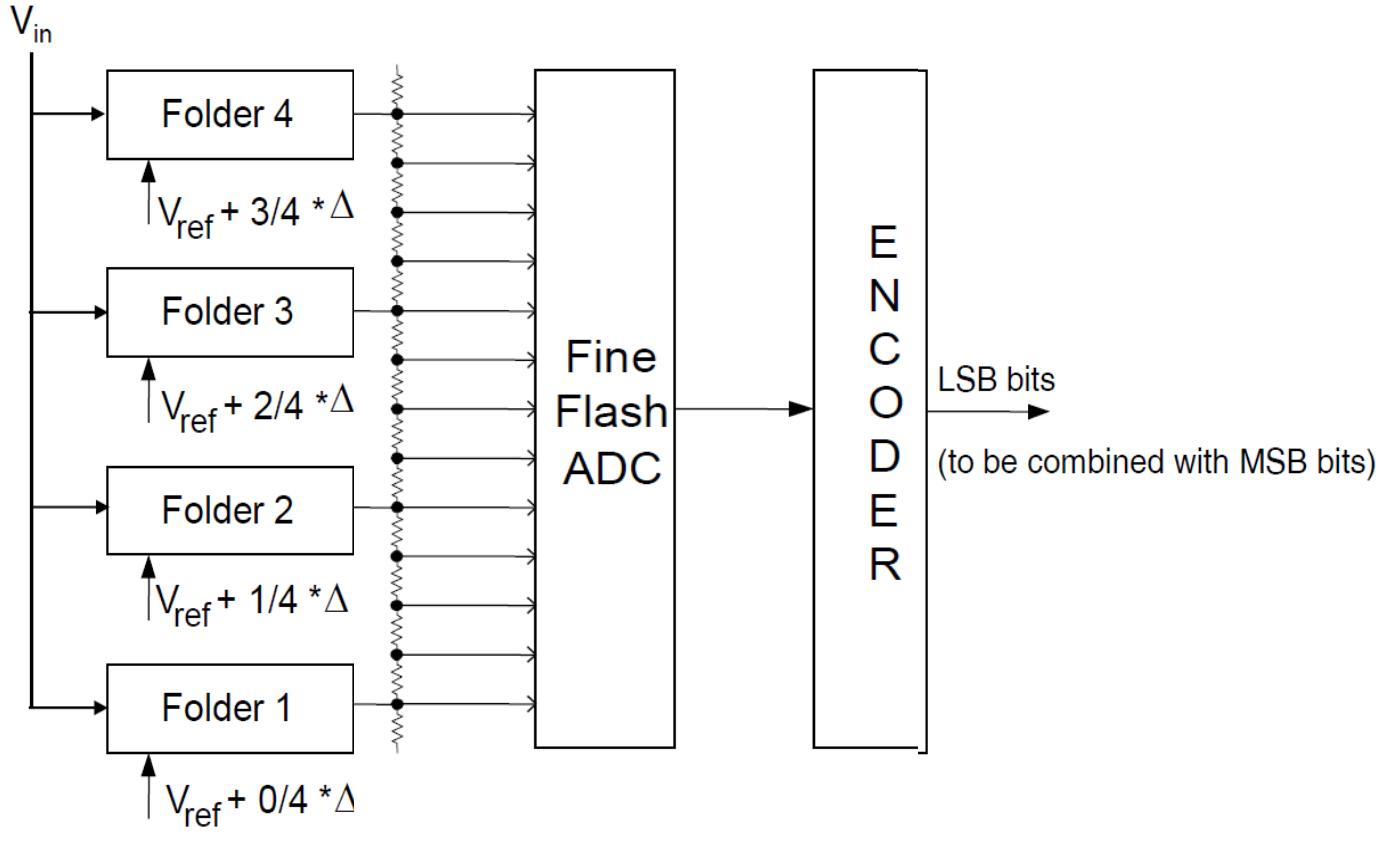


Example of 4 folders with 4 folds each, so 16 zero-crossings, hence + 4 LSB bits
... anywat upper limit... due to added complexity.



Folding + Interpolation Flash ADC

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Example of 4 folders with 4 resistor interpolators each, hence + 4 LSB bits
... other ideas?

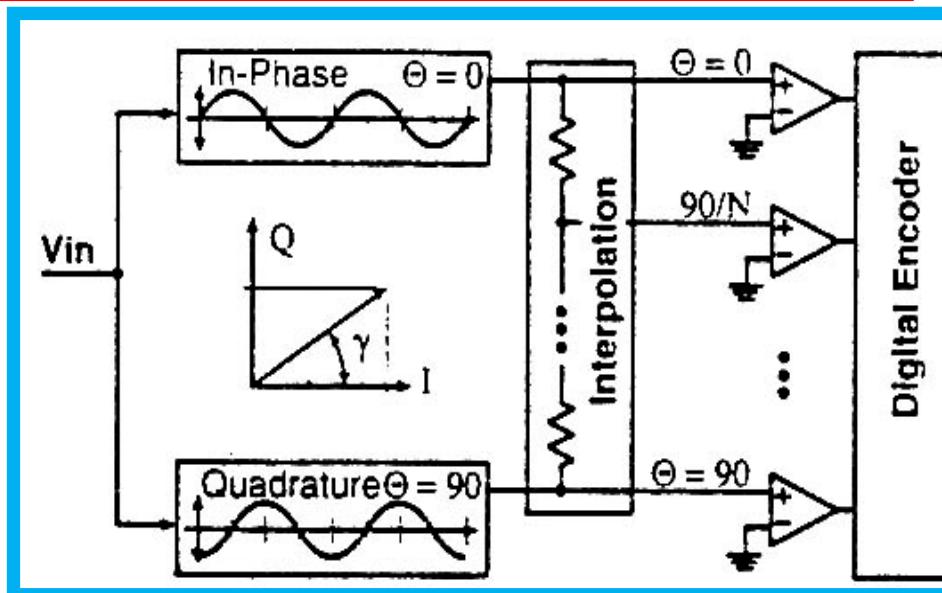
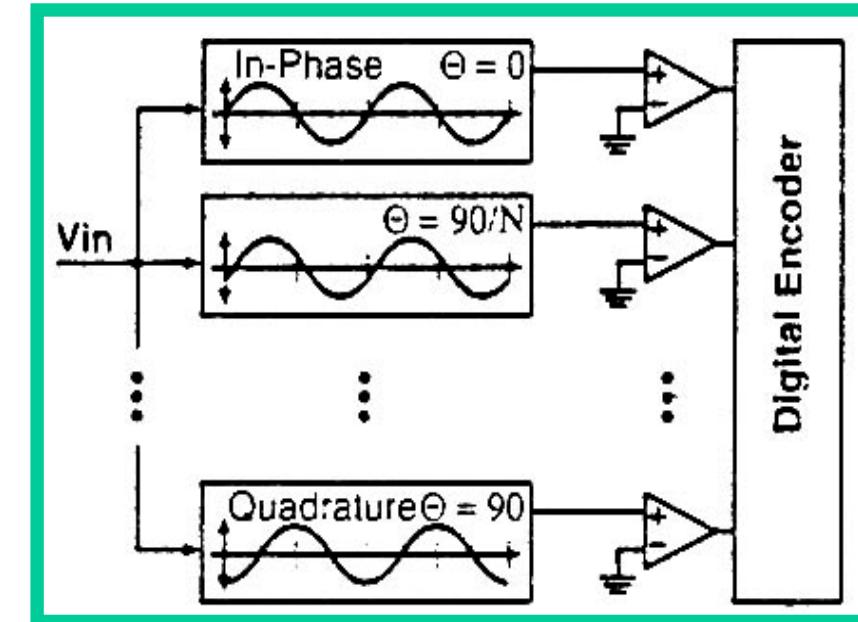
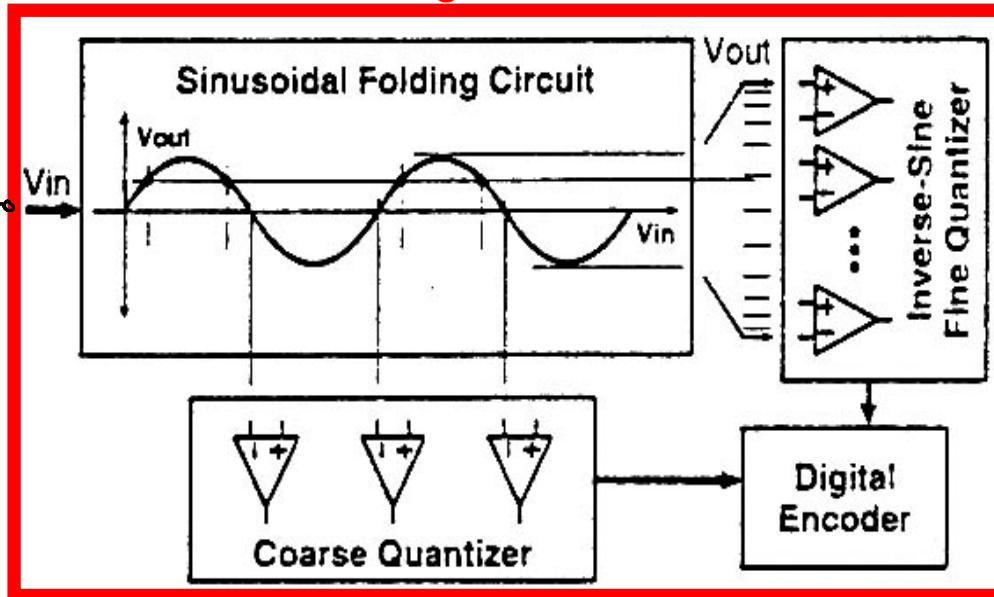


Folding Flash ADC

Sinusoidal folding (followed by non-linear quantization)

Prendiamo il Folding ADC e prendiamo l'usata MSB poi prendiamo un DAC e trasformiamo l'usata in Analogico e la ributtiamo SAI¹ ingresso del Folding ADC fine course e soffraziono i veloci; in questo modo posso ottenere un circuito di folding.

Questo è il blocco base per creare un Half Flash ADC.



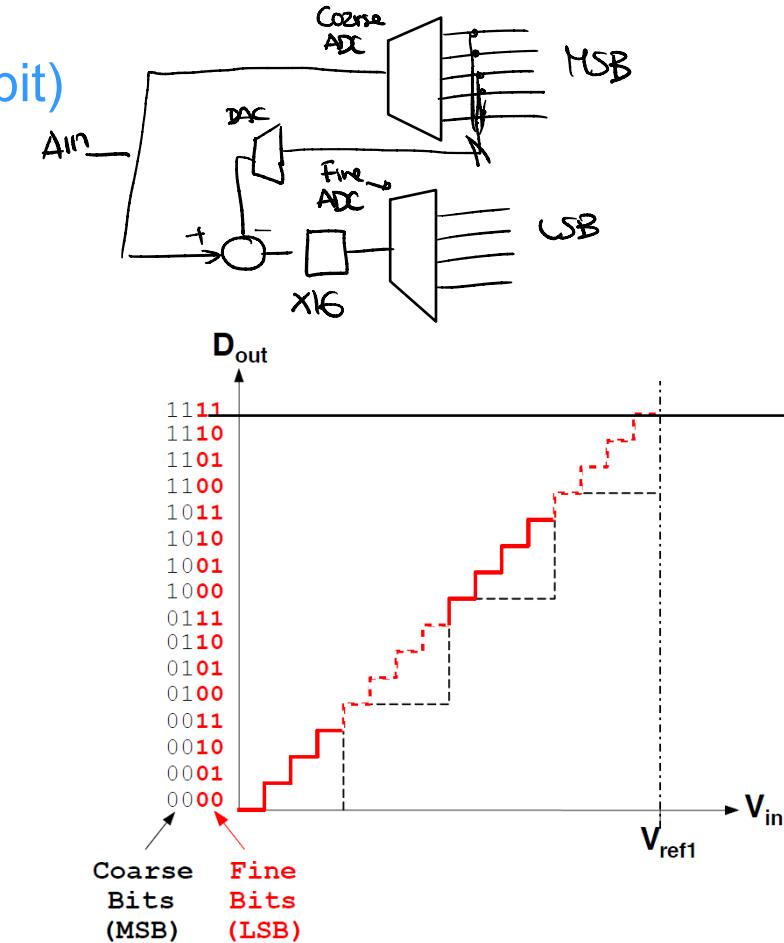
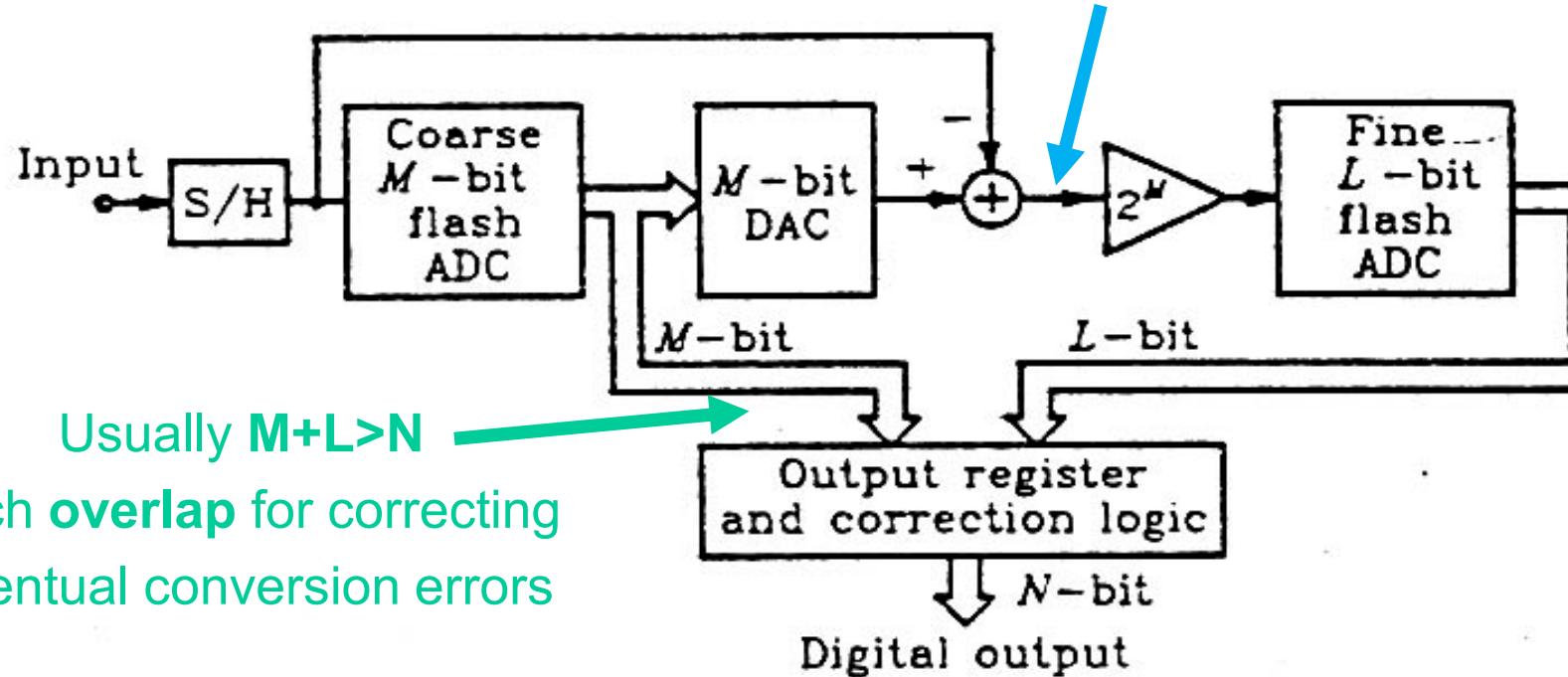
Many folding circuits (256), one for each quantization level

Few (2) folding circuits,
followed by interpolation



Half-Flash ADC

Residual (quantization error in case of just M bit)



Conversion is a two-steps process through two cascaded stages

Such “half-flash” (or “two-step flash”) approach drastically reduces:

components count

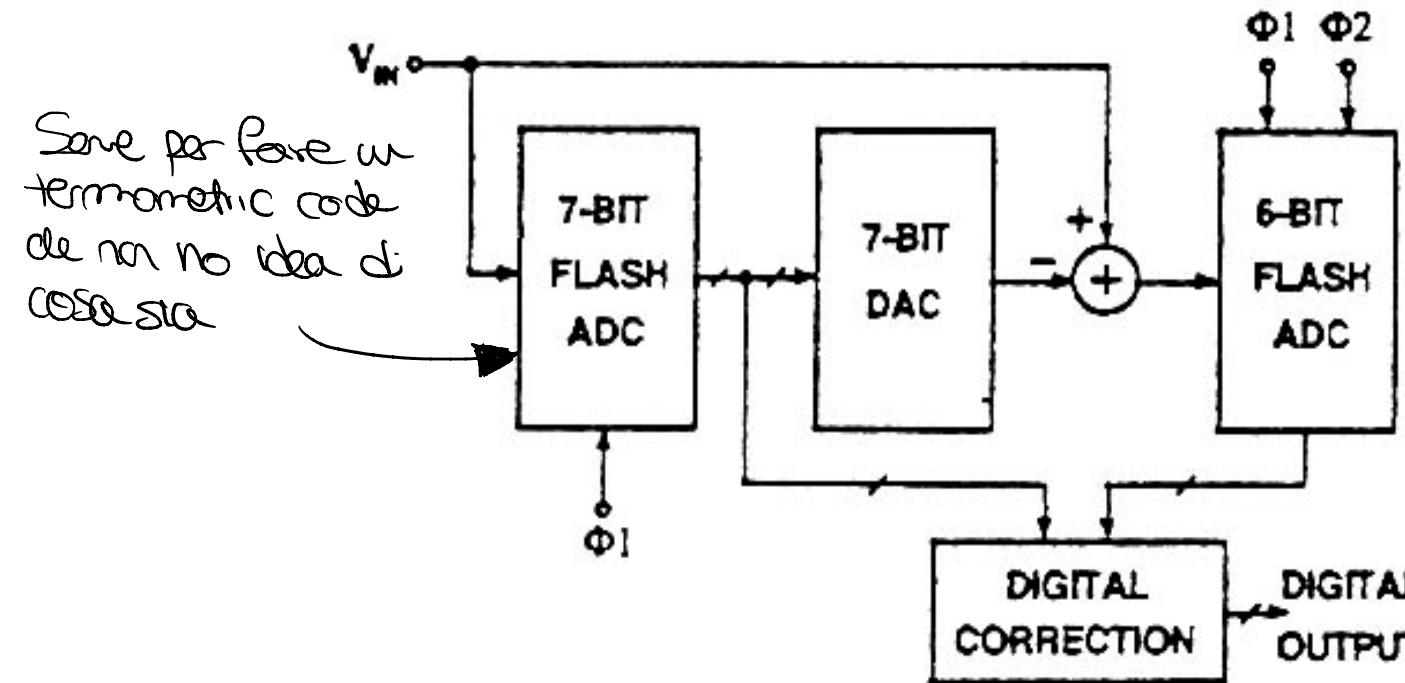
power dissipation

input capacitance



Half-Flash ADC

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PERFORMANCE OF A/D CONVERTER

Differential Linearity	12 b
Conversion Rate	5 MHz
Peak SNDR	65 dB
Input Range	5 V
Power	200 mW
Power Supply	5 V
Input Capacitance	15 pF
Active Area	1.2 mm × 3.0 mm
Technology	1- μ m CMOS

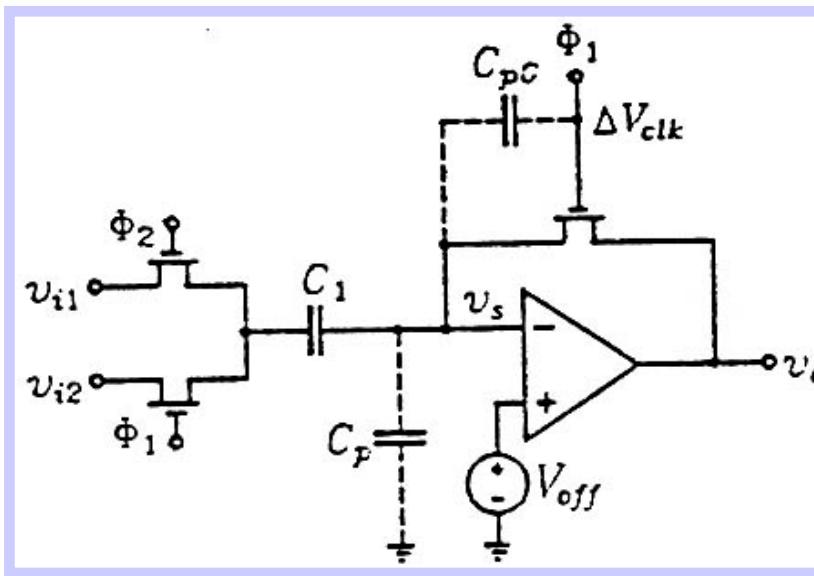
Example 12bit ADC:

a flash ADC should require 4096 comparators

the half-flash ADC instead needs $27+26=192$ comparators (1bit overlap)

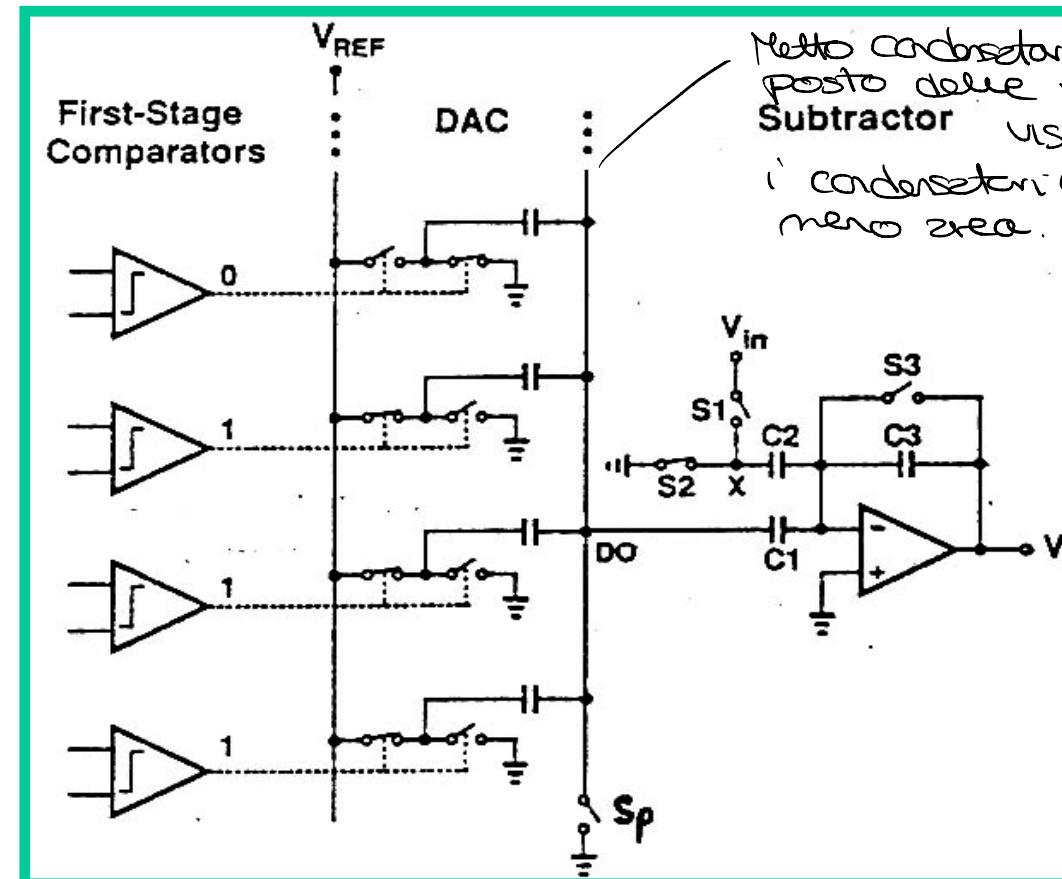


Half-Flash ADC: internal designs



- Φ_1
 - Input Sampling
 - Offset Cancellation
 - Stage 1 Strobed
 - Stage 2 Tracking
- Φ_2
 - Stage 2 Strobed

Very compact comparators
with auto-zeroing



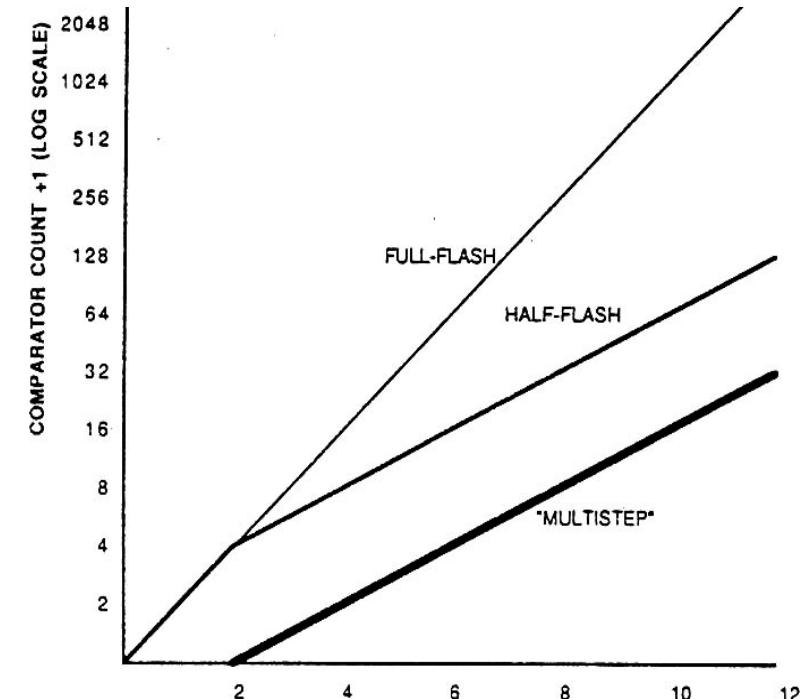
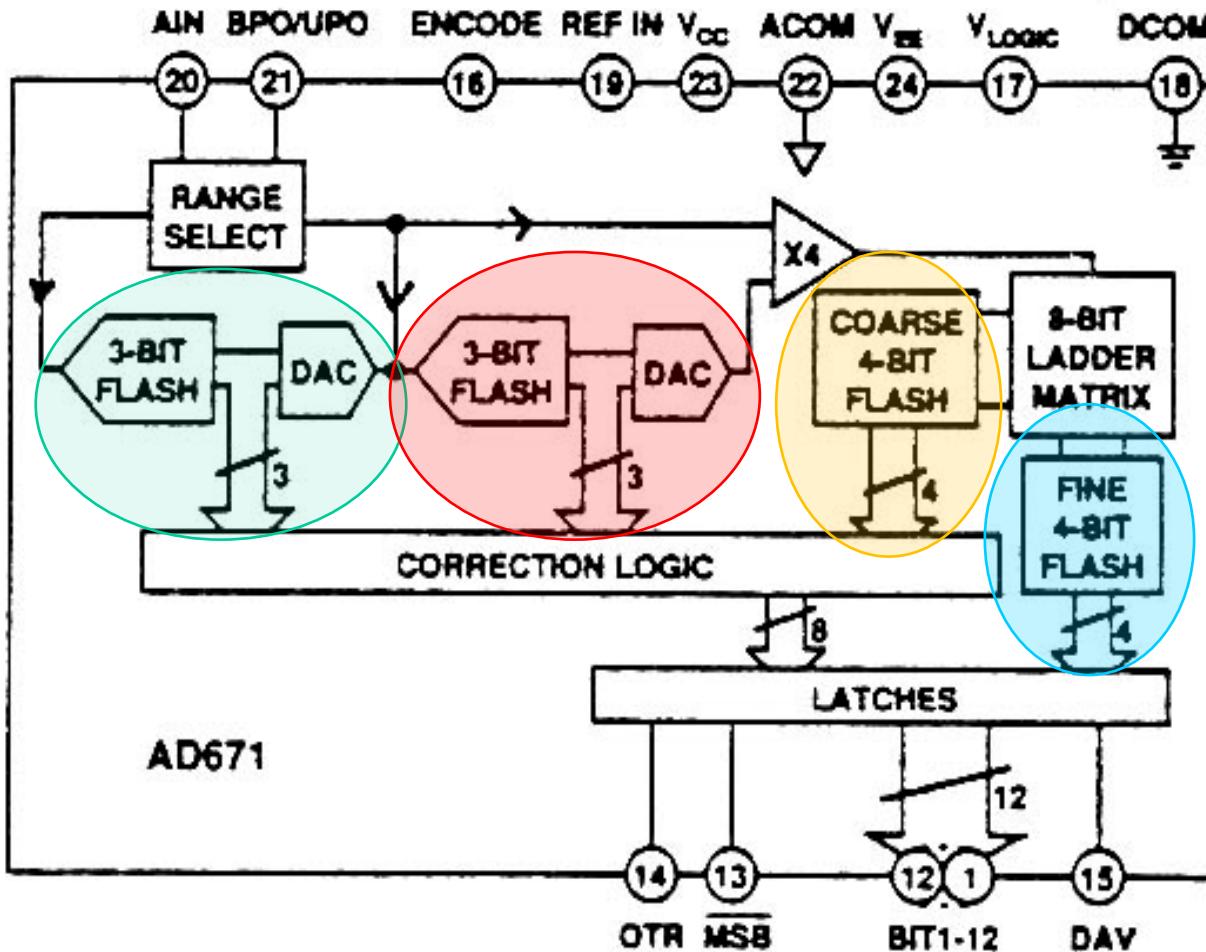
Simple ADC (thermometric output)
and minimal DAC (charge sharing)

Compared to flash ADCs, half-flash ADCs minimize area occupation and power dissipation, though with slower conversion time



Multistep ADC

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Example of a 4-step ADC:

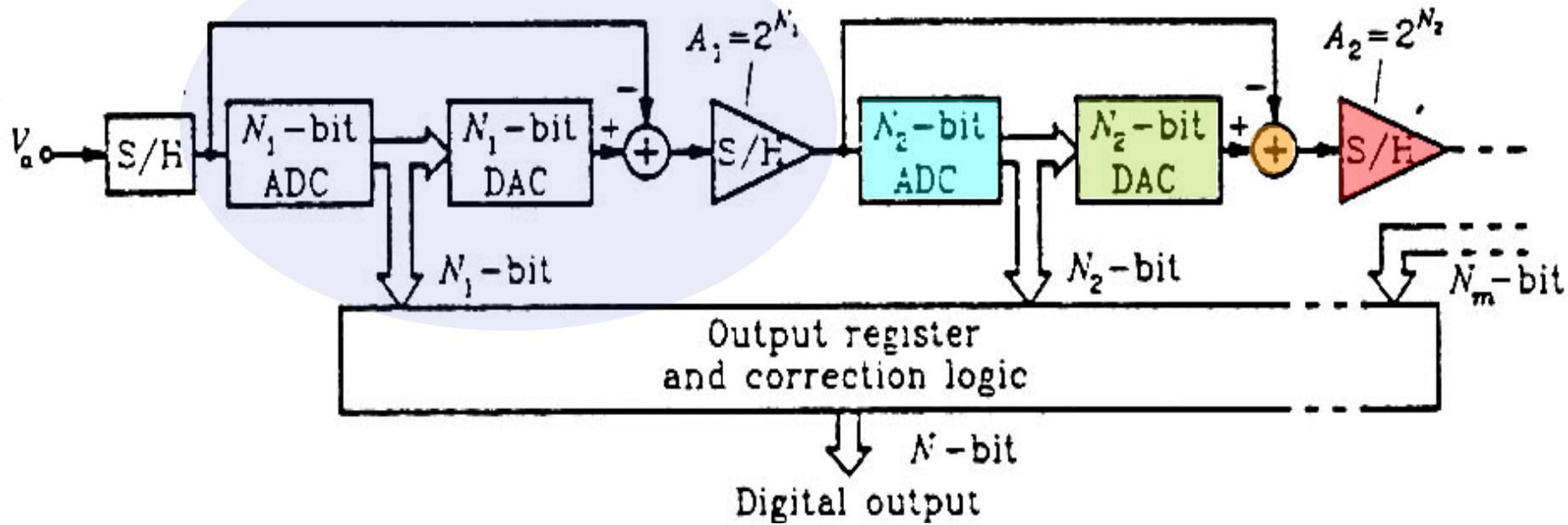
First 3bit and second 3bit flash ADCs, then first 4bit and second 4bit half-flash

Overall just 48 comparators !



Pipelined ADC

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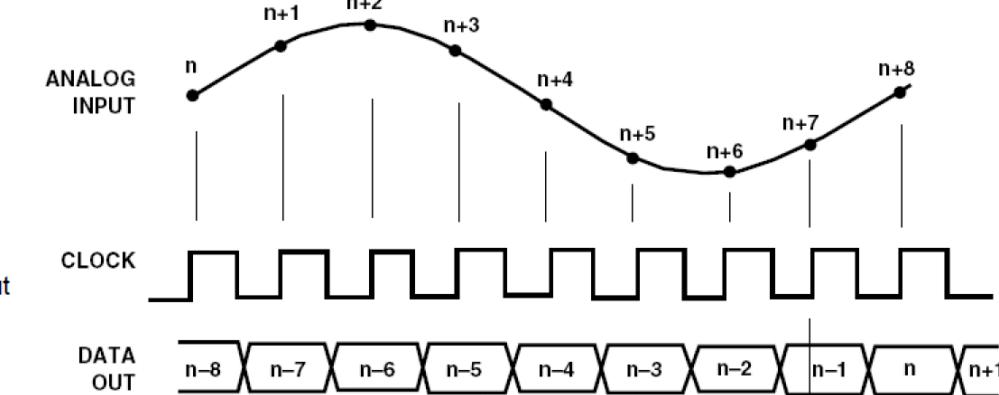
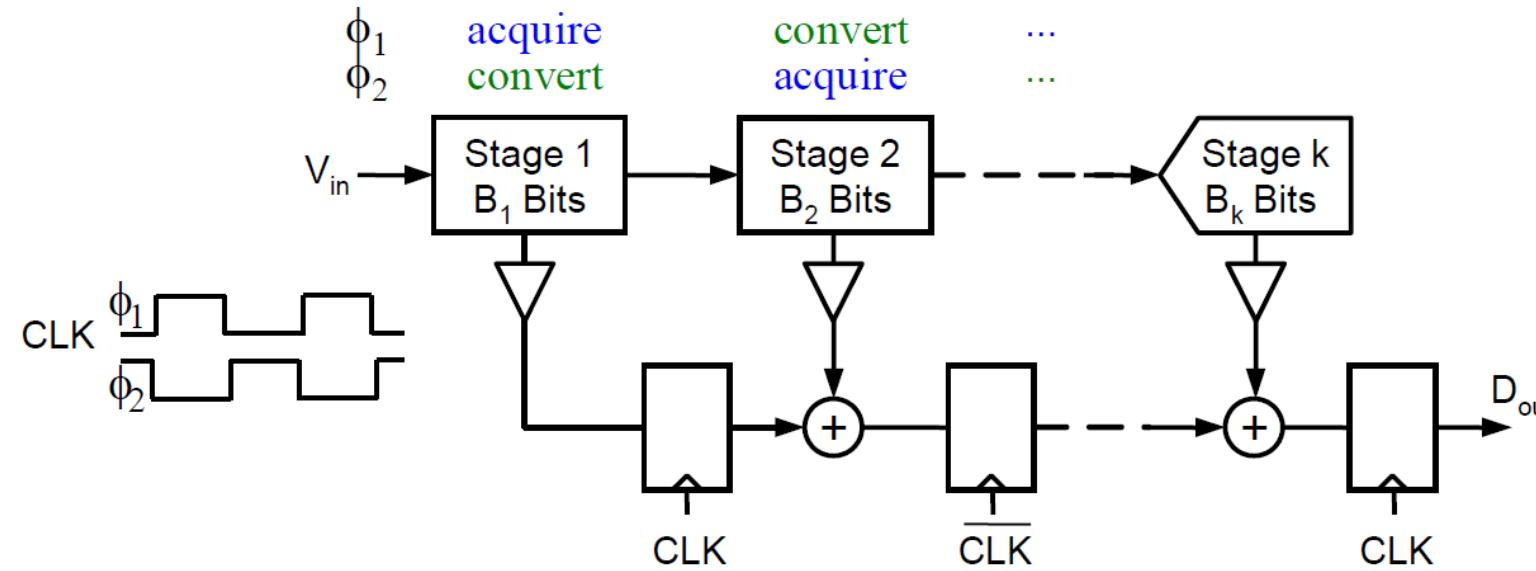
m-stages each one composed by:

ADC Flash (low resolution 1÷4bit), DAC, analog adder and amplifying S&H

Compared to multistep ADC, now S&Hs allow parallel-pipelined processing (like bucket-brigade)



Pipelined ADC - latency



New output data every clock, but a latency of 8 clock cycles
Need for data alignment

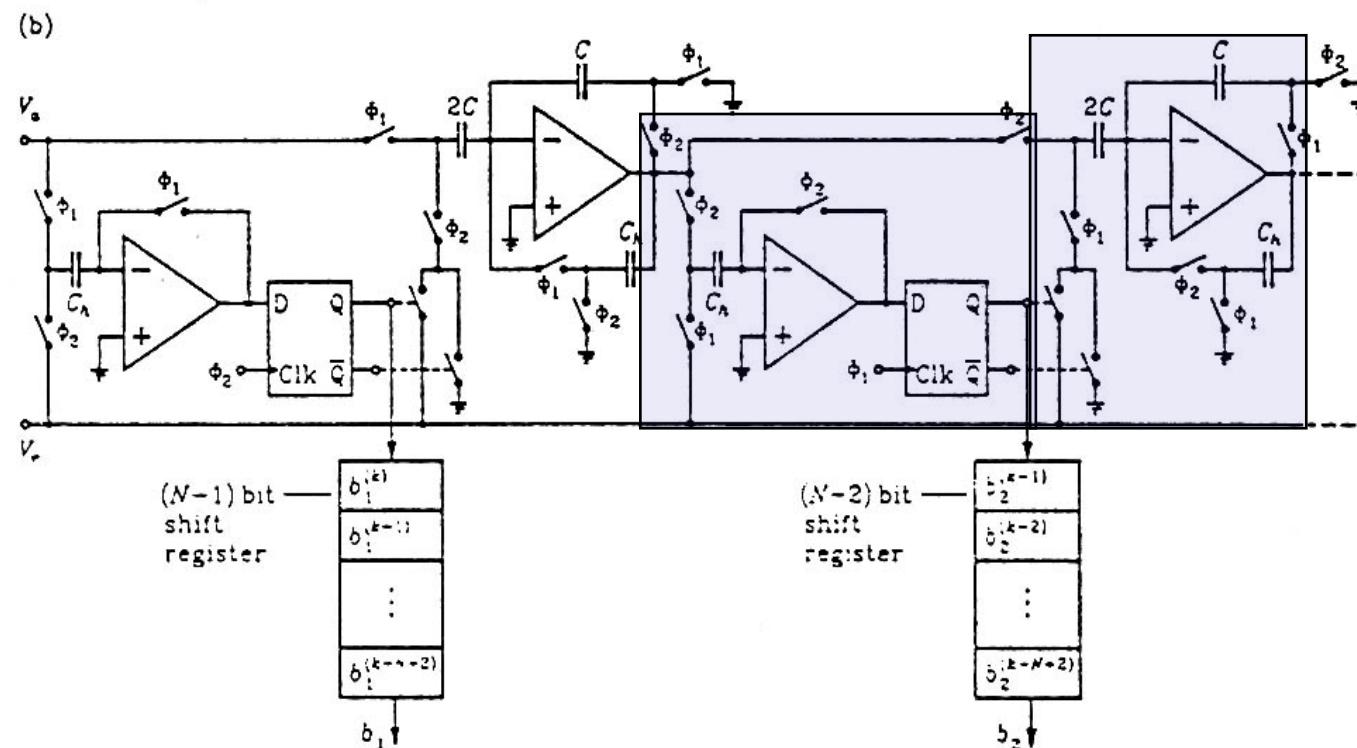
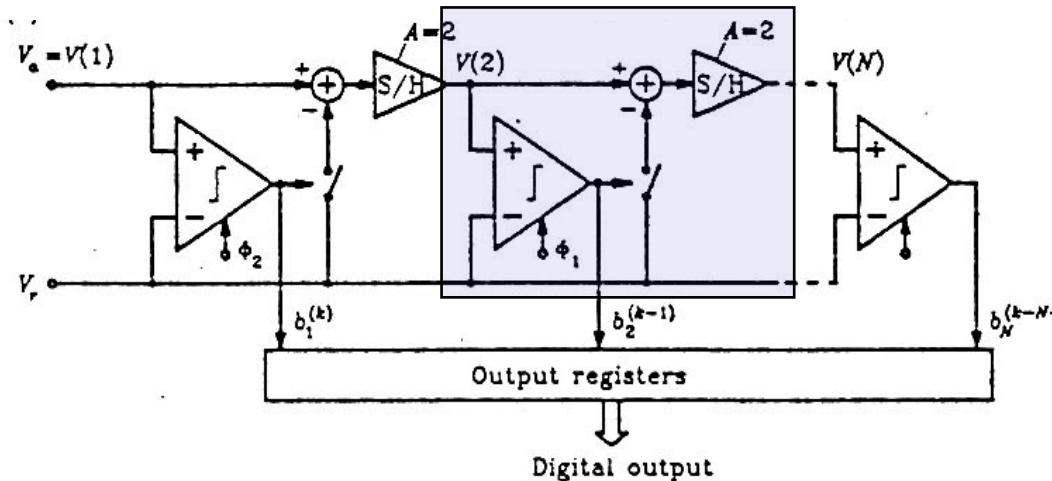


Pipelined ADC: example of N stages of 1bit ADCs each

For example:

Nbit pipelined ADC

with N stages of 1bit each

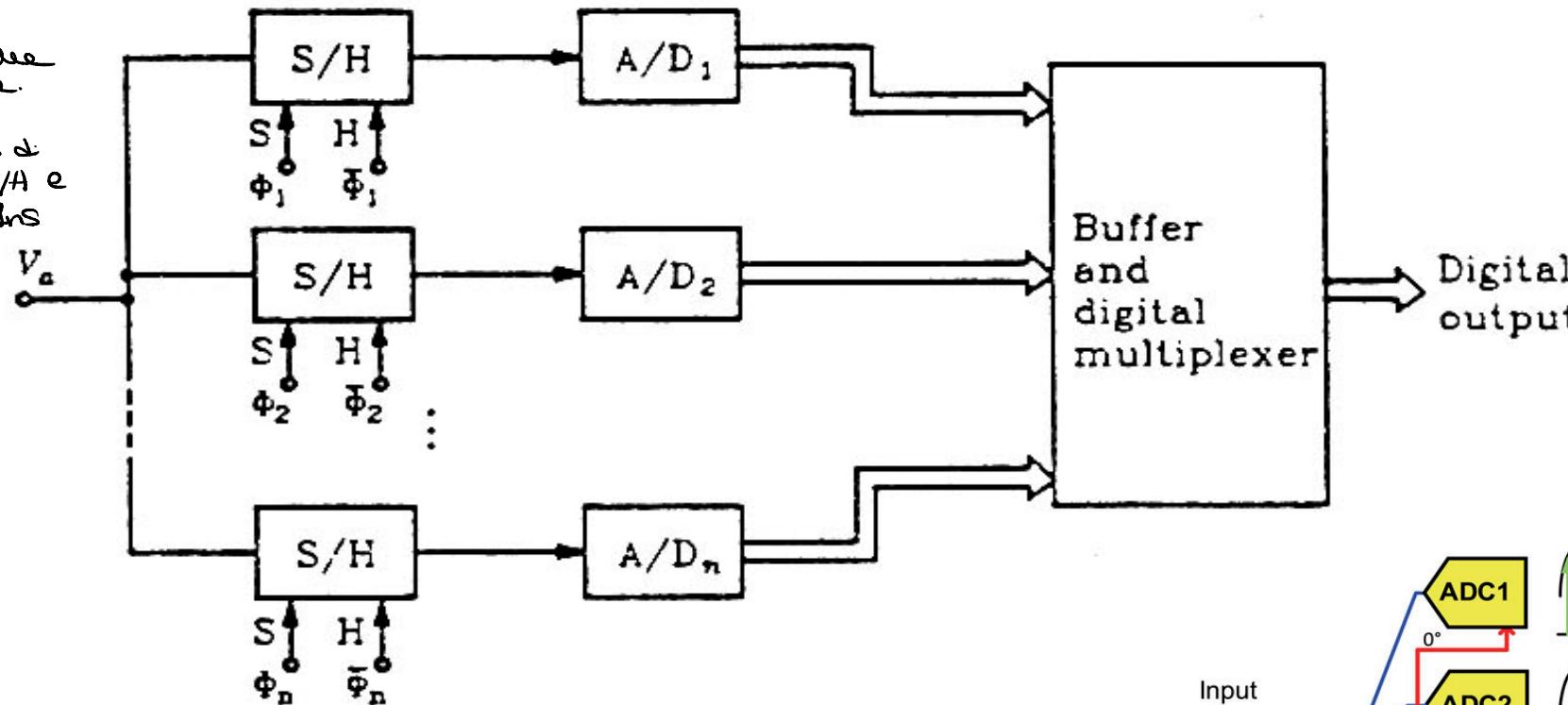




Time-interleaved ADC

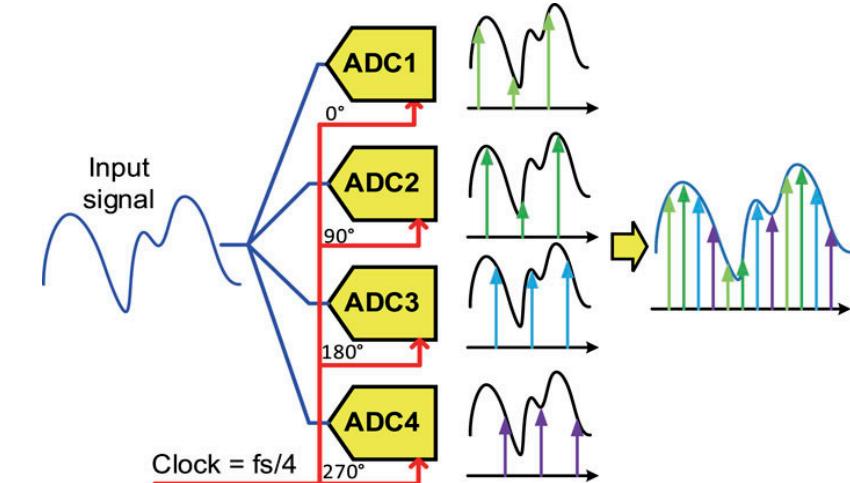
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Voglio un dispositivo molto veloce per le conversioni. Tipo 1ns conversion time.
Non possono esistere.
Altrimenti prendo 10 ADC da 10ns e tempo di conversione è 100 ns e uso 10 S/A e
è zopro e chido in serie dopo l'ins.
Cosa ho sempre il segnale
perché parallelizzo.



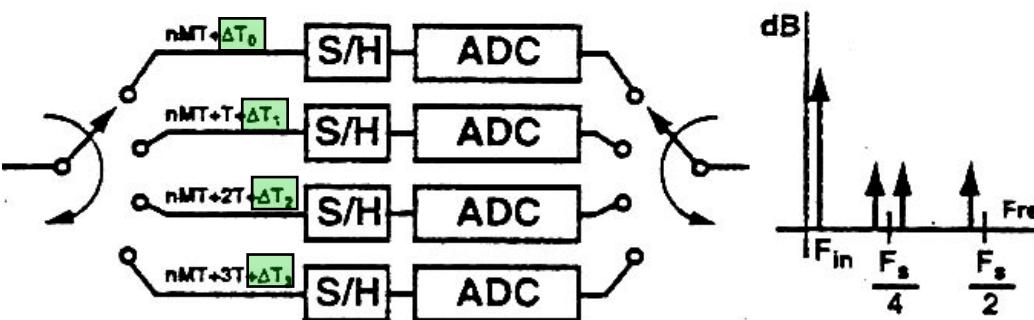
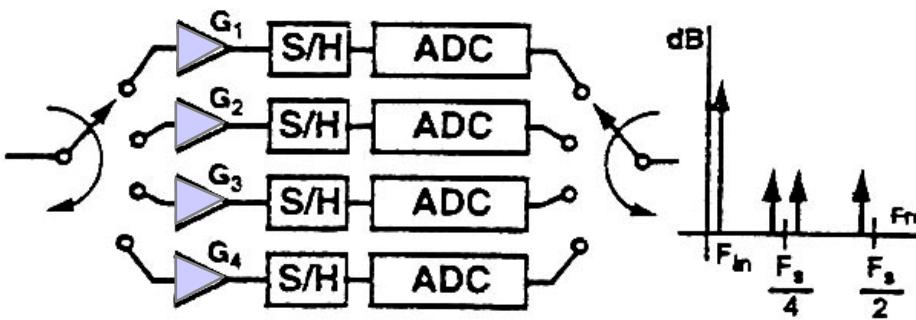
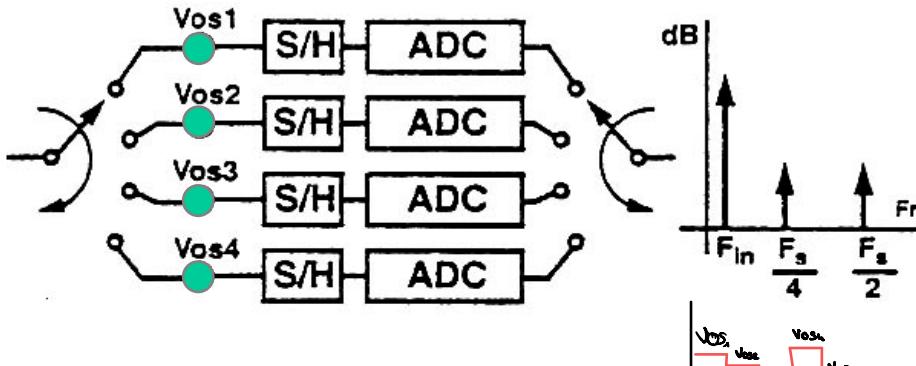
For high f_s more ADC can run in parallel on different samples:

- C channels with identical Nbit ADCs each, with individual S&H
- Each channel samples the input signal at a rate $(C \cdot T_{clock})^{-1}$
- The channels operate in sequence
- Overall sampling rate is N-fold that of a single channel





Time-interleaved ADC: mismatches



Cogni' ciascuno ha il suo offset

Quel'è l'errore che trovi in uscita? Non sarà un offset in DC perché legendo dagli ADC diversi abbiamo un segnale non costante in uscita con periodo $T_P = 4 \cdot T_{sampling}$ quindi avrò uno spettro con spurie ogni moltiplica di $f_S/4$. Può succedere che una di queste spurie cada dentro la banda del mio segnale.

Offsets:

spurious tones at multiples of f_S/C

Consideriamo che ogni S/H ha il suo guadagno diverso degli altri. Allora se estremo con uno sinusoidale subiamo che è come se sopra il mio segnale ci sia uno modulatore dell'output. E quindi ho 2 tone esterne alla frequenza di modulazione.

Gains:

spurious tones at frequencies :

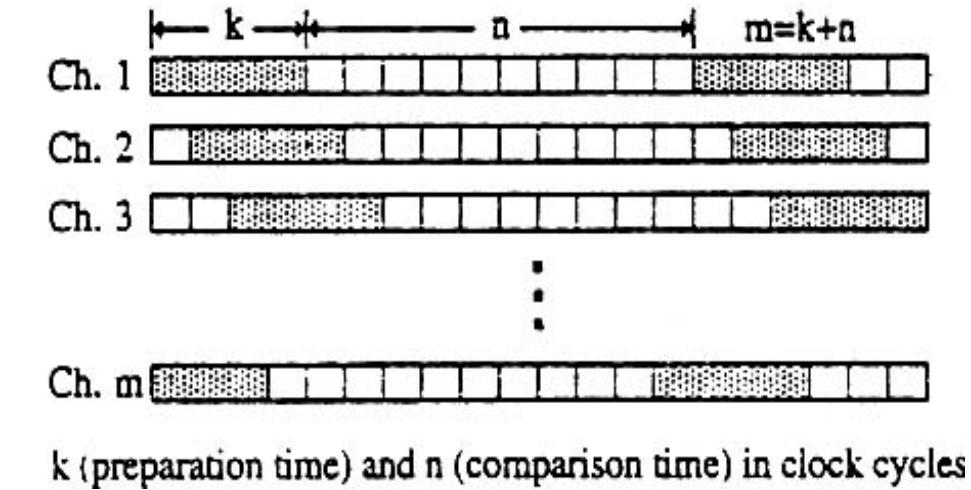
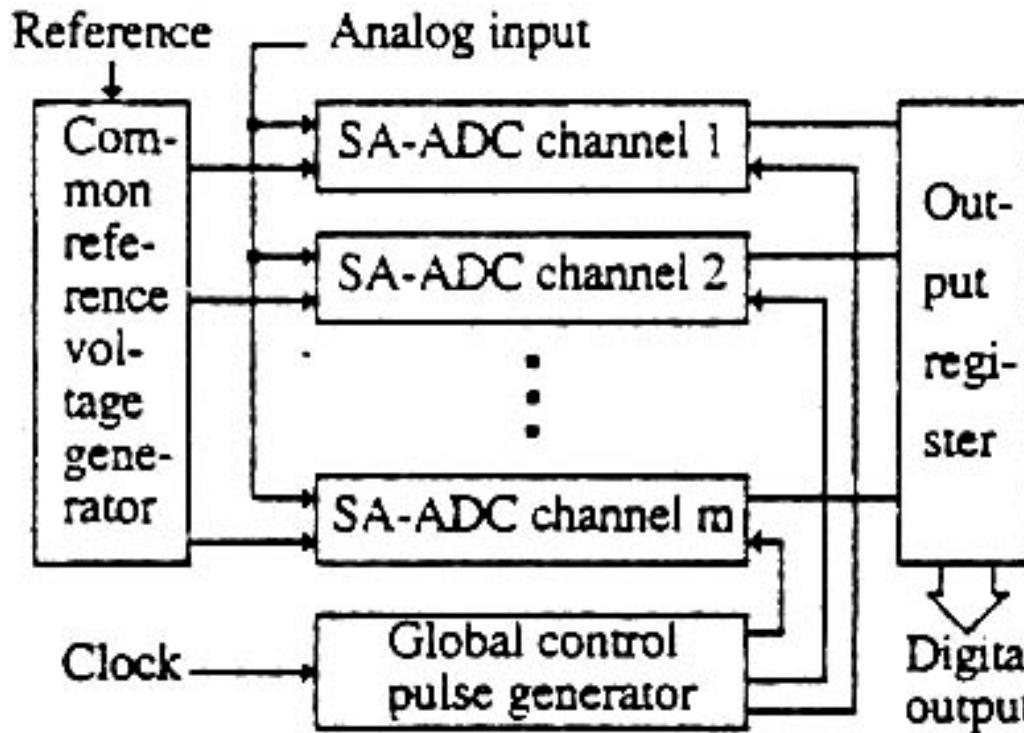
$$f_S/C \pm f_{in} \quad 2 \cdot f_S/C \pm f_{in} \quad \dots \quad (C-1) \cdot f_S/C \pm f_{in}$$

Sampling time:

spurious tones of intensity increasing with f_{in}



Time-interleaved ADC



Example 14 10bit SARs at 5Msps in parallel reach 70Msps with just 267mW



- Many advanced architectures and solutions
- Possibility to mix different processing

Next lesson: **15 – Oversampling**