POLITECNICO
MILANO 1863





ELECTRONIC SYSTEMS

2021-22 academic year

prof. Franco ZAPPA

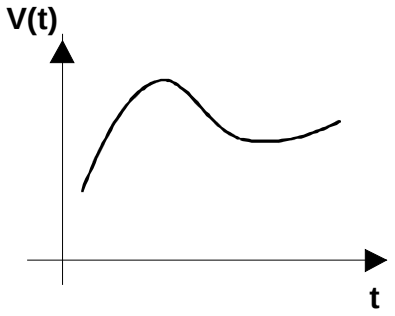
Summary

15 – Oversampling and Sigma-Delta

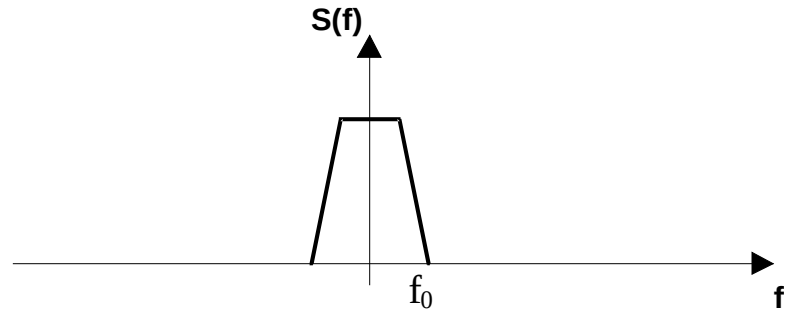
- Why increasing f_S beyond the Shannon minimum
- Standard oversampling
- Advanced Sigma-Delta oversampling
- Why 1bit is equal or even better than many
- Need for DSP for digital filtering and decimation

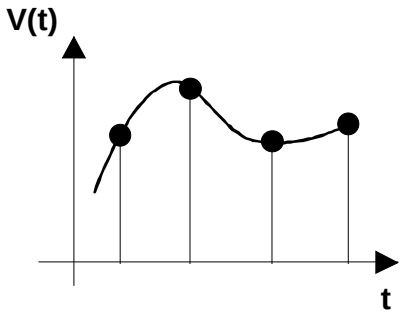
Sampling

Effect of oversampling: spectrum replicas move further away...

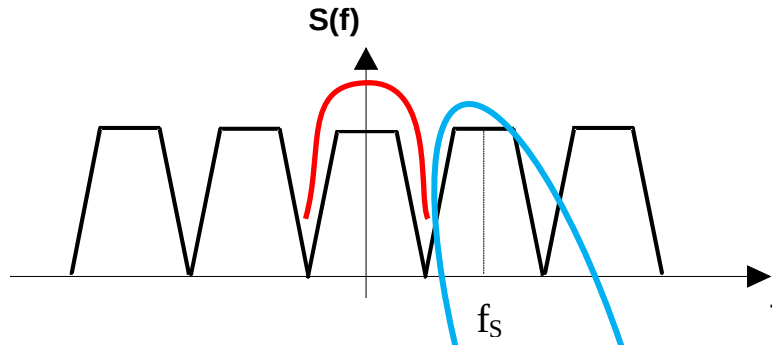


(a)

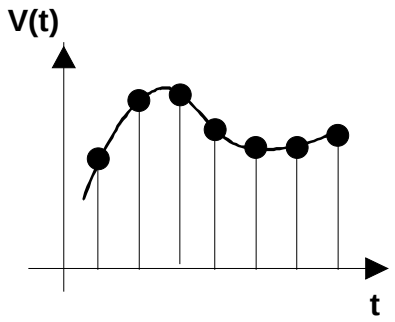




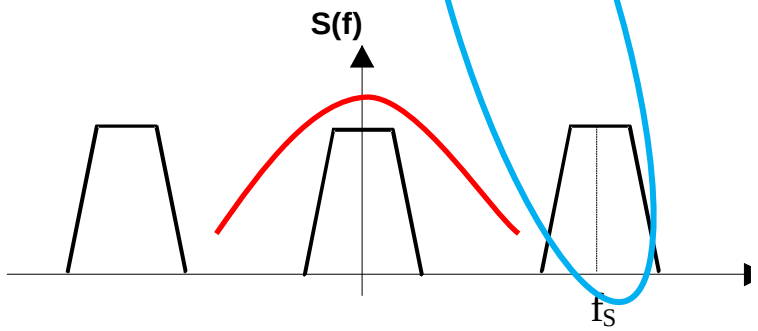
(b)



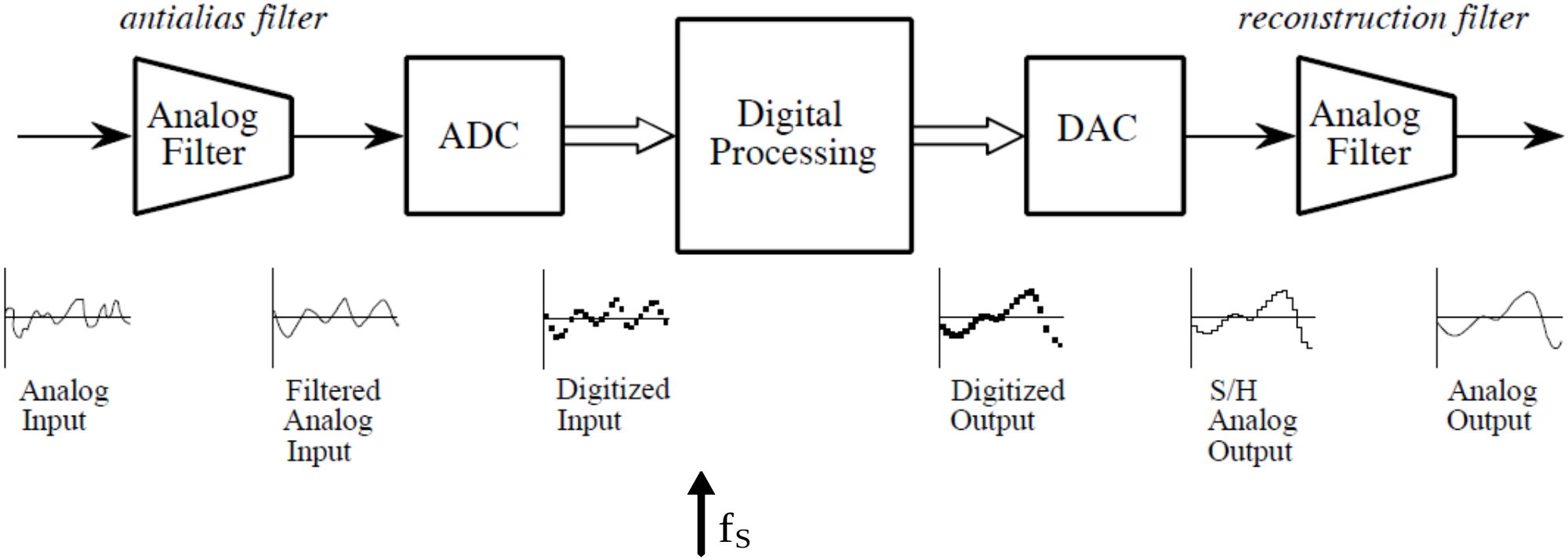
... so easier reconstruction (filter), but EVEN MORE !!!



(c)



Quantization



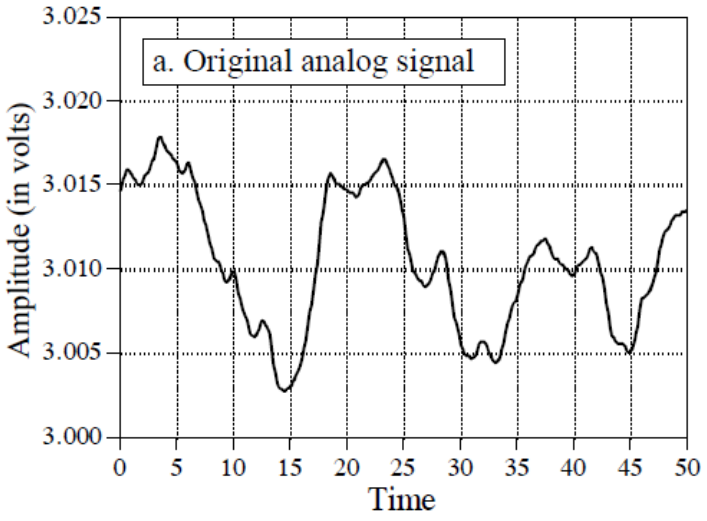
Quantization error:

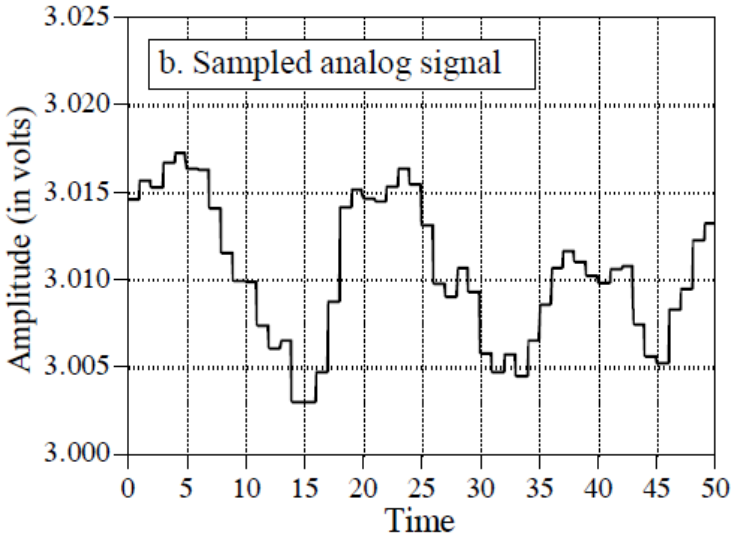
Overall quantization power (variance): $\sigma_q^2 = \left(\frac{FSR}{2^n\sqrt{12}}\right)^2 = \frac{LSB^2}{12}$

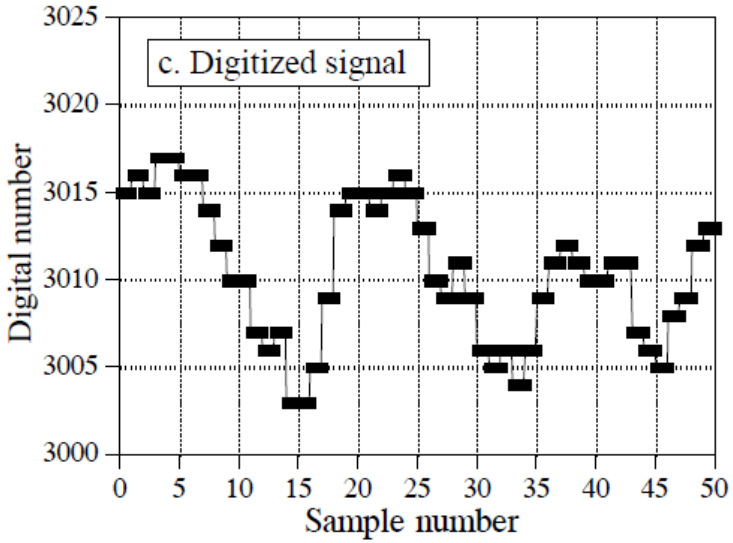
Spectral density: $Q_q(f) = \frac{\sigma_q^2}{f_S/2}$

Example: FSR=5V n=12bit f_S=40ksps σ_q^2= (352μV) ^{2} $Q_q(f)=(3.52\mu V/\sqrt{Hz})^2$

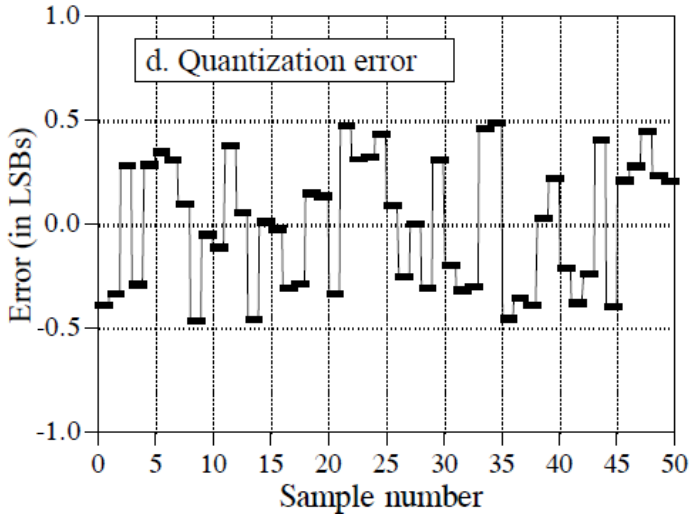
Quantization

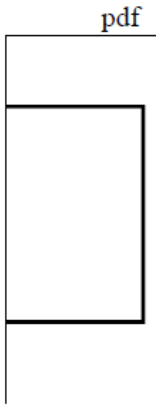






Quantization error = sampled – digitized signal d = b - c

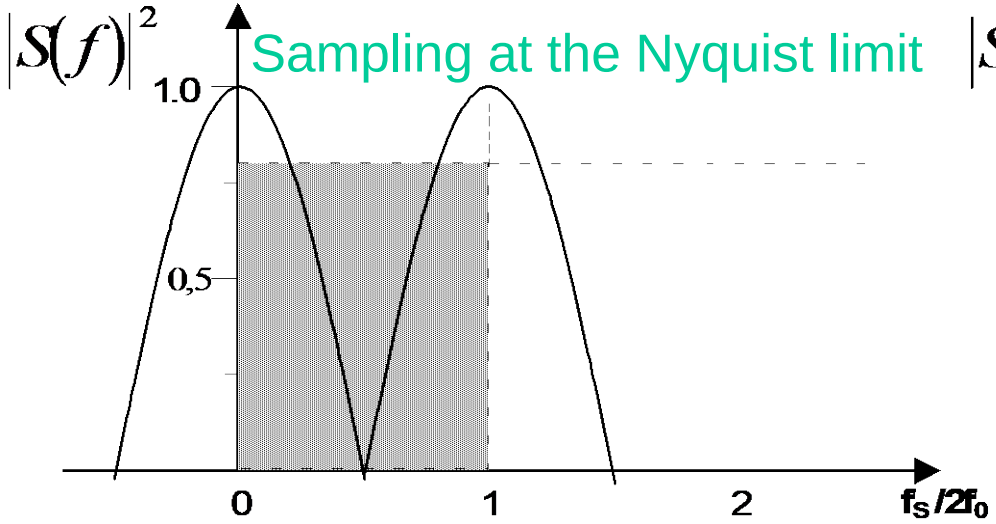


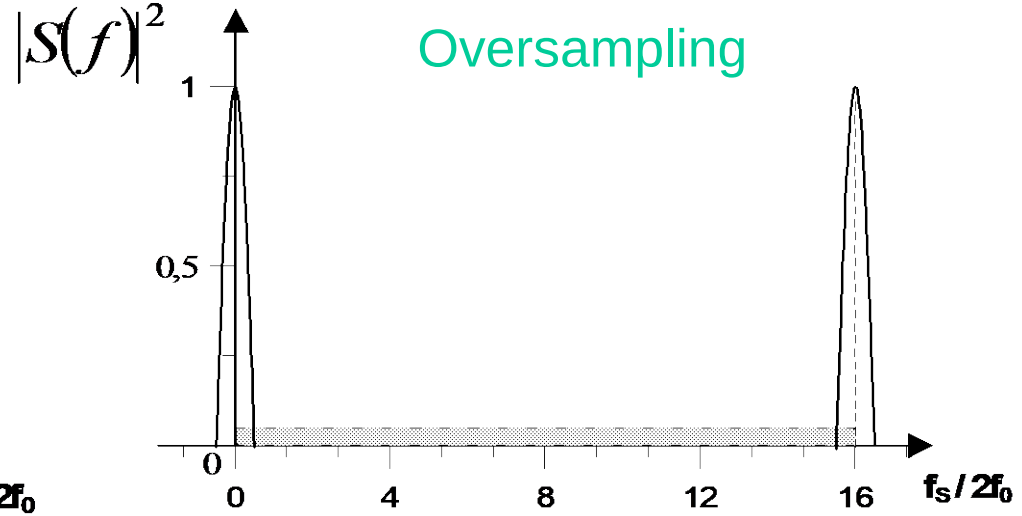


Stephen W. Smith, www.DSPguide.com
"The Scientist and Engineer's Guide to DSP"

Oversampling

Spreads quantization noise across a broader spectrum!!!





Possible (?!?) improvement:

$$\sigma_{out}^2 = \int_0^{f_0} Q_q{}^2(f)\,df = \sigma_q{}^2 \cdot \left(\frac{2f_0}{f_s}\right)$$

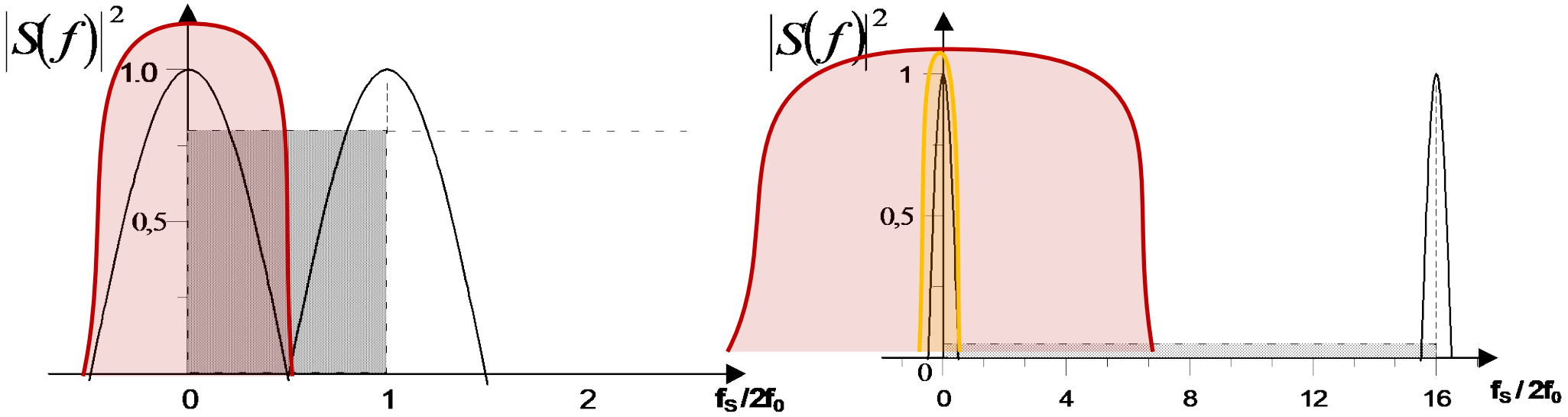
Oversampling factor:

$$OS = \left(\frac{2f_0}{f_s}\right)$$

Oversampling

Sampling at the Nyquist limit

Oversampling



Standard filter at $f_S/2$

SMART filter at f_{max}

since with oversampling $f_S/2$ is no longer f_{max}

Oversampling

Classical ADC:

$$SNR_{teorico} = \frac{V_{eff}}{q} = \frac{FSR/2\sqrt{2}}{\Delta/\sqrt{12}} = \frac{FSR/2\sqrt{2}}{FSR/2^n\sqrt{12}} = 2^{n-1}\sqrt{6}$$

$$SNR_{teoricodB} = 20\log_{10}\left(2^{n-1}\sqrt{6}\right) = 6,02n + 1,76$$

Oversampled ADC:

$$SNR_{out} = \frac{V_{eff}^2}{\sigma_q^2/\sqrt{OS}} = SNR_{teorico} \cdot \sqrt{OS}$$

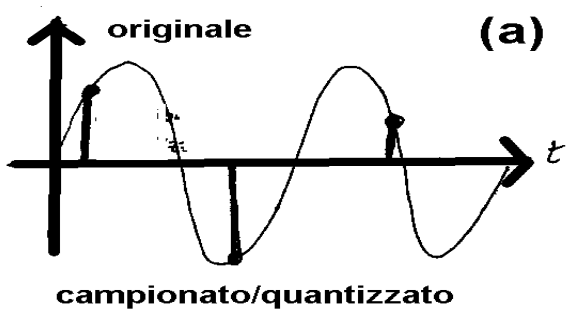
Improvement of √2 = 3dB = ½bit

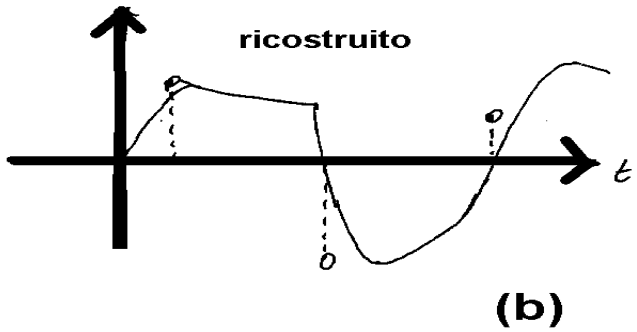
every doubling of f_S (OS) !

Oversampling

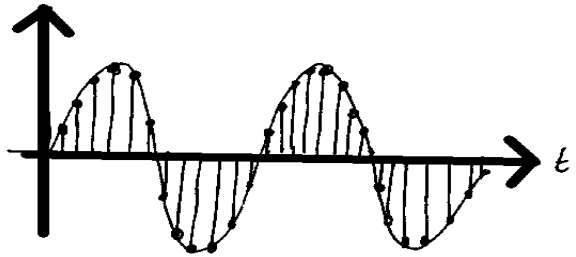
Qualitative description:

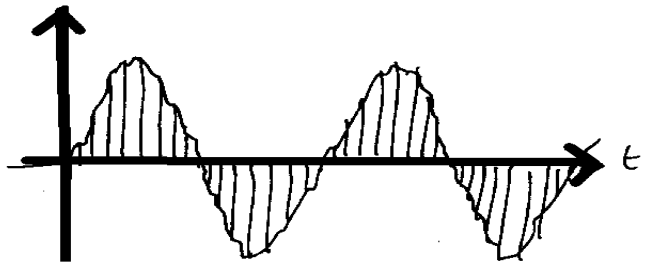
Nyquist sampling and reconstruction



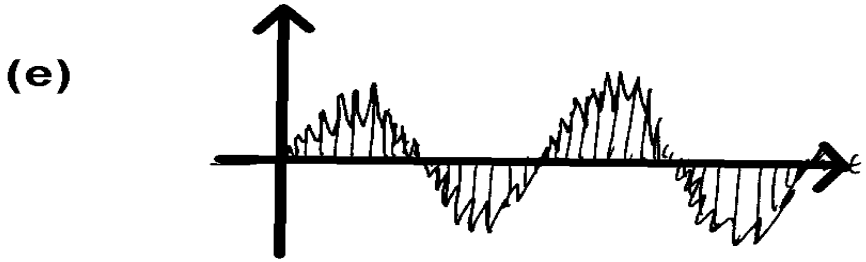


Oversampling and SMART reconstruction (filtering at f_0)





Oversampling and SILLY reconstruction (filtering at $f_S/2$)



Decimation

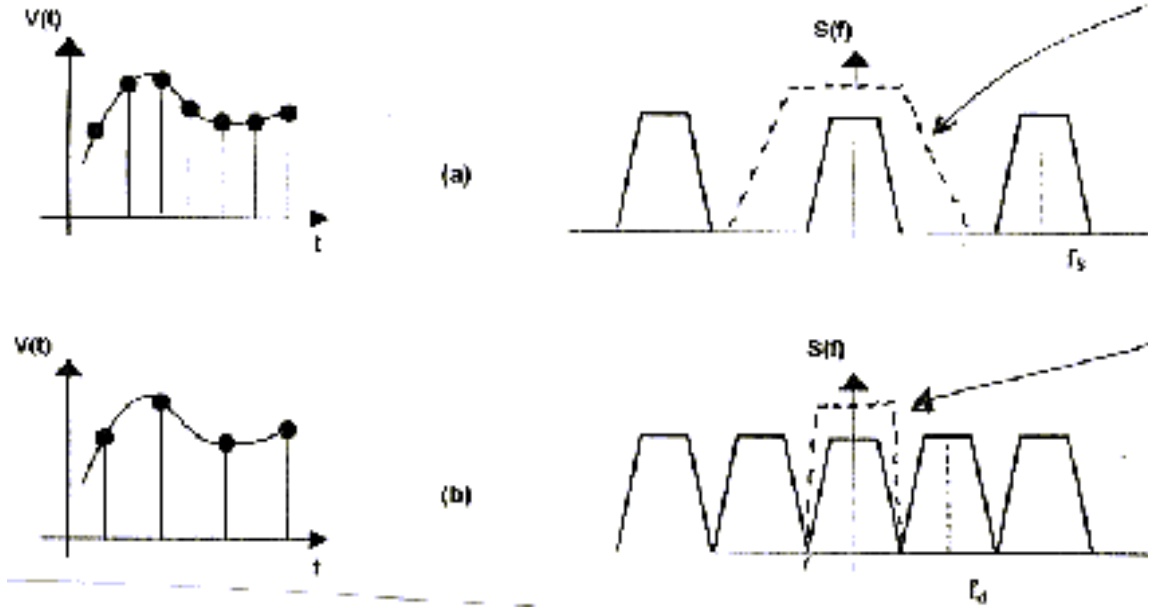
The bit stream has too high a frequency !

Example: f_0=20kHz OS=256 f_S=10.24 Msps

In fact, even if the through-put of the input samples is $f_S >> f_{max}$

at the output it is indeed enough to provide a throughput of $2\ f_{max}$

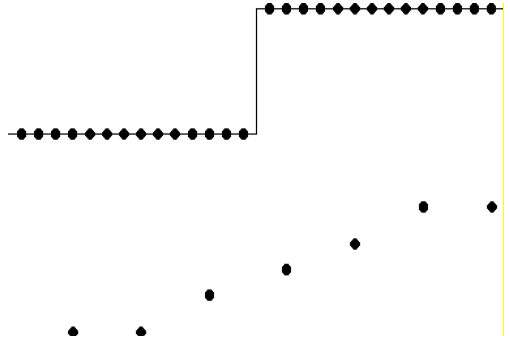
It is possible to take “one-out-of-OS” samples, thus **DECIMATING** it



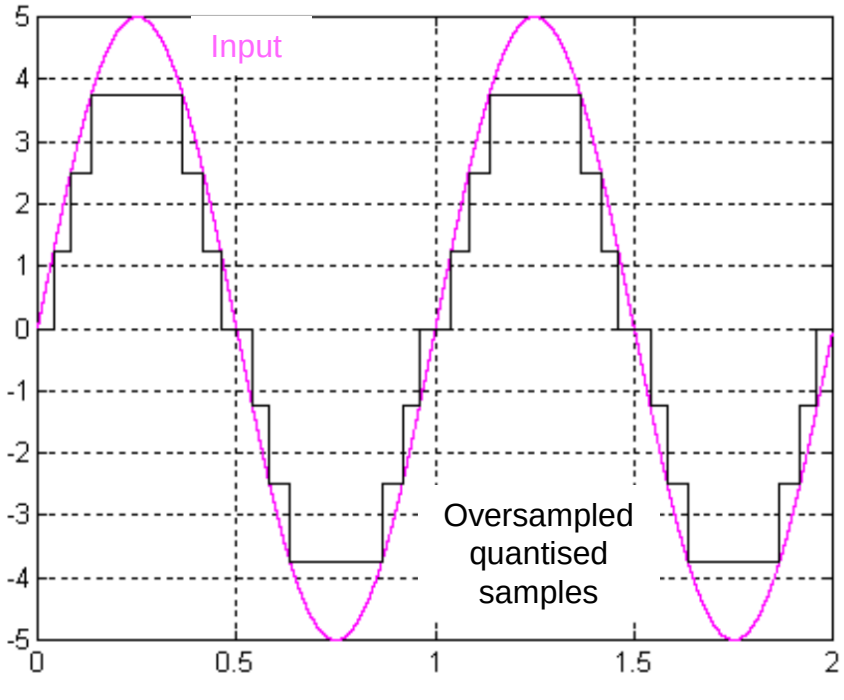
… or even better to **FILTER** and then to **DECIMATE** !

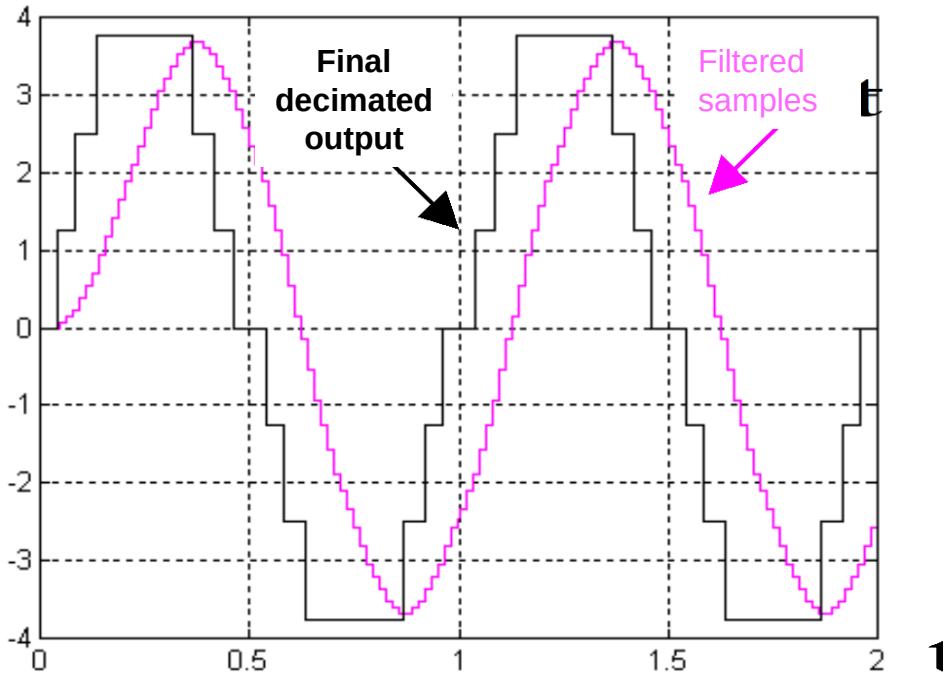
Digital filtering

Example, a simple moving average provides more quantized levels, i.e. it increases resolution

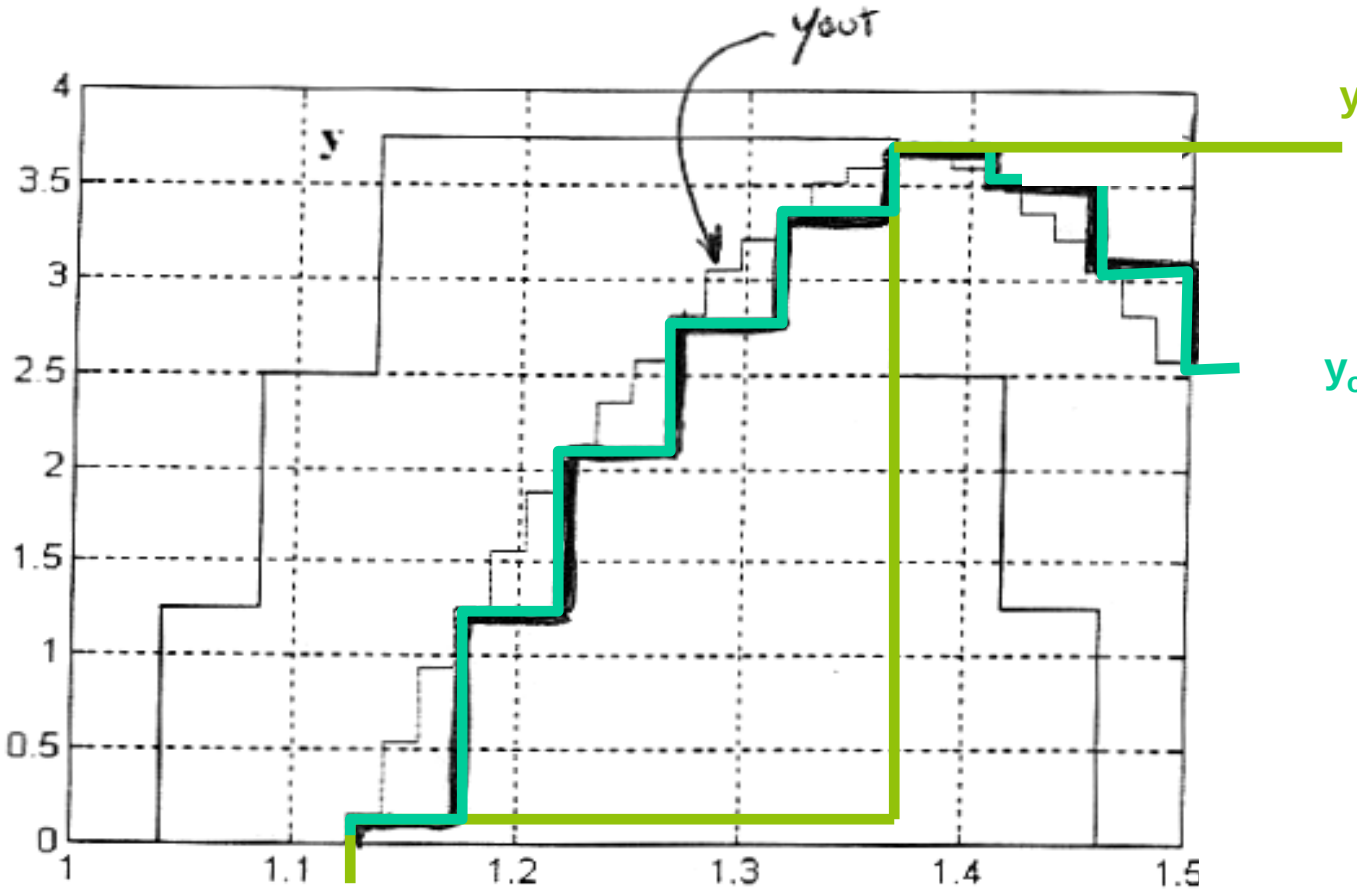


Example: f_0=1Hz OS=16 f_S= 32sps n=3bit





Digital filtering and Decimation

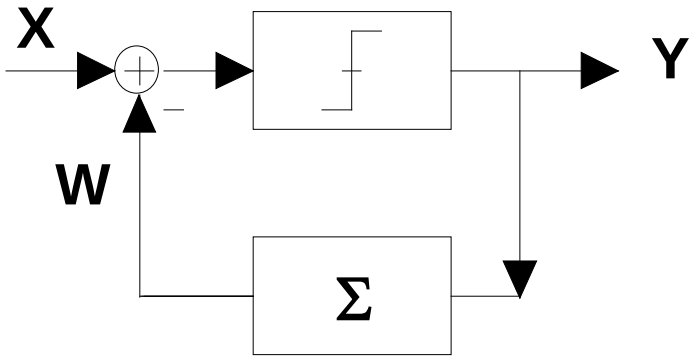


y_{out} after 1:16 decimation

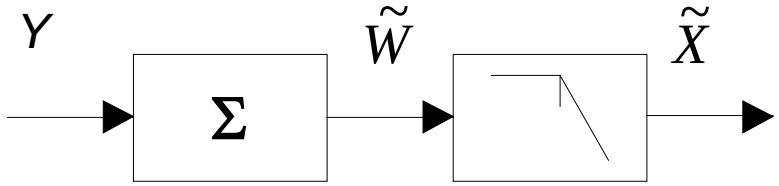
y_{out} after 1:3 decimation

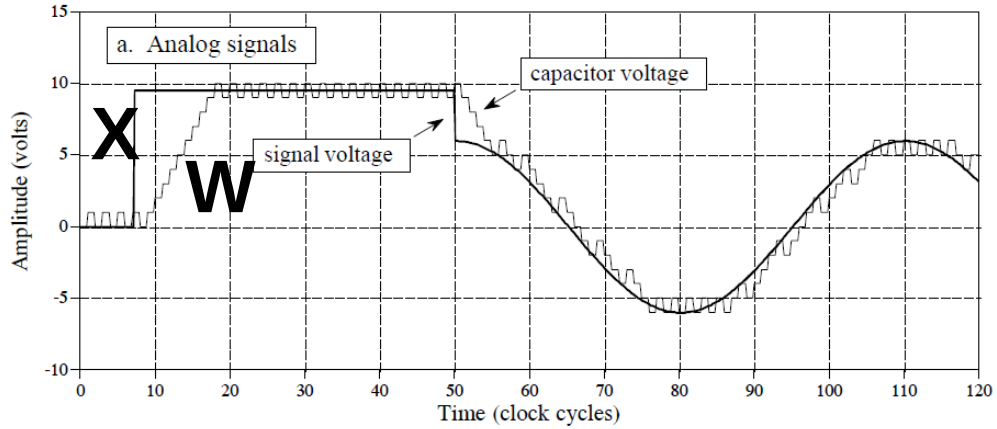
Delta Modulation

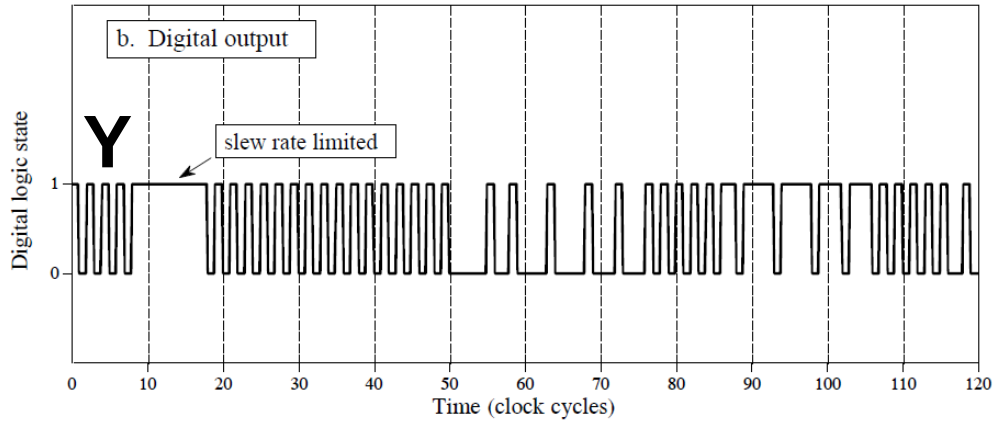
Delta Modulator



Delta Reconstructor



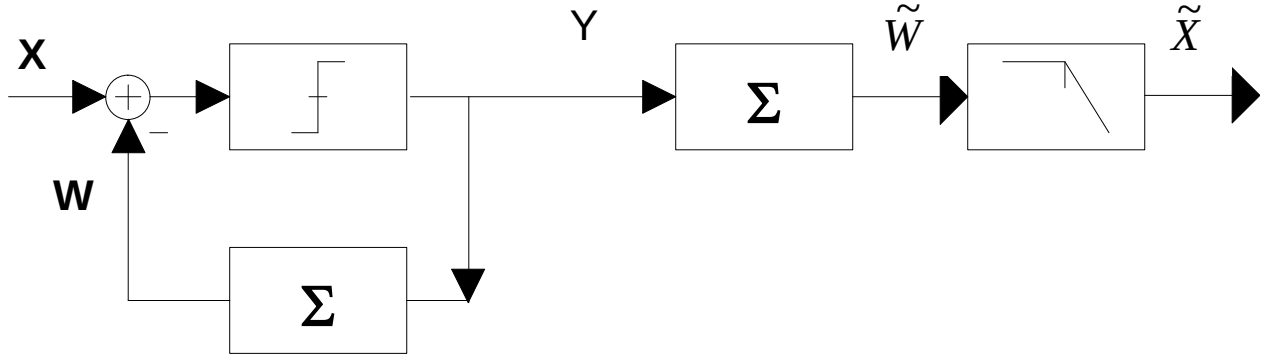


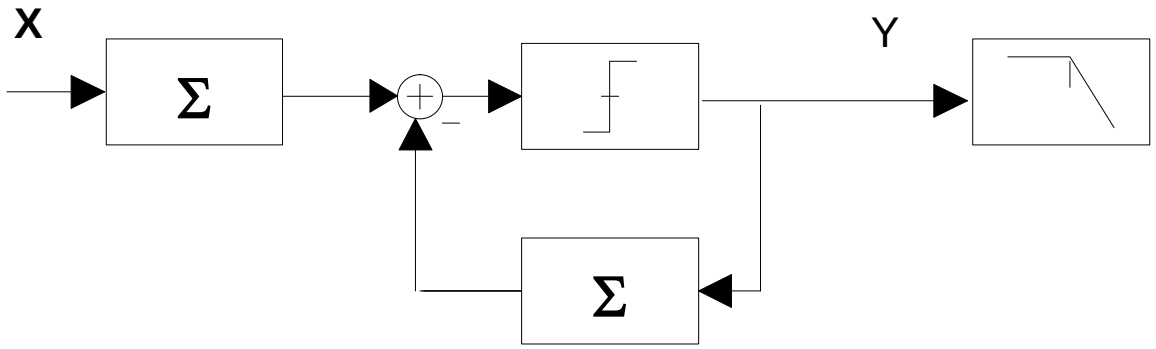


It is like the tracking ADC, but just 1bit output (up/down) instead of the whole byte

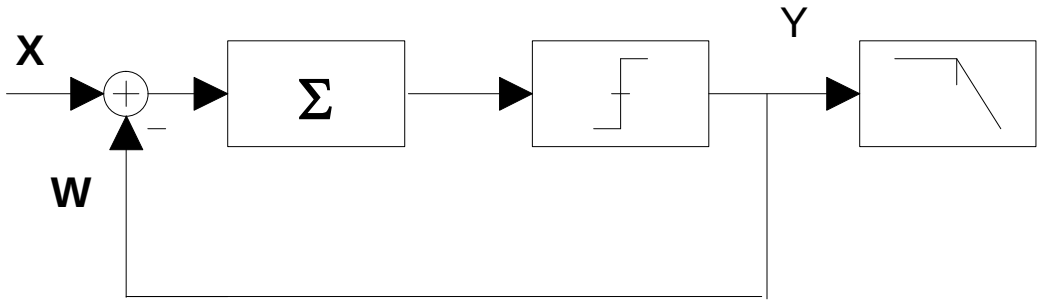
Sigma-Delta Modulation

Let's shuffle cards...



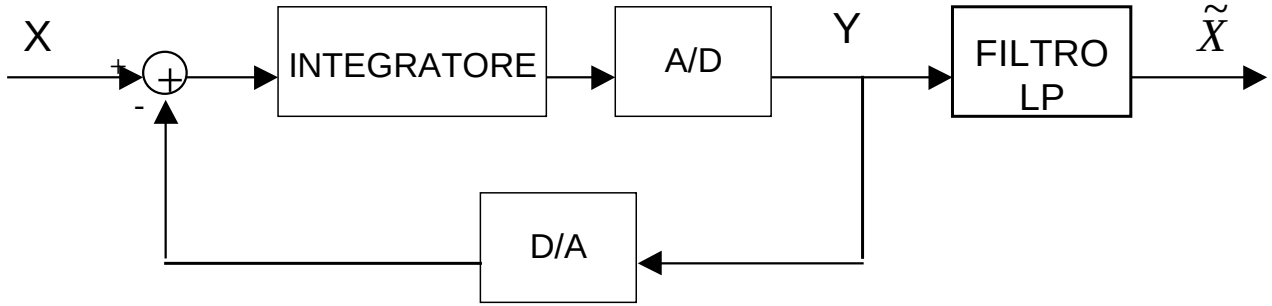


It is still the same in-out relationship,
but NOT for the QUANTIZATION error

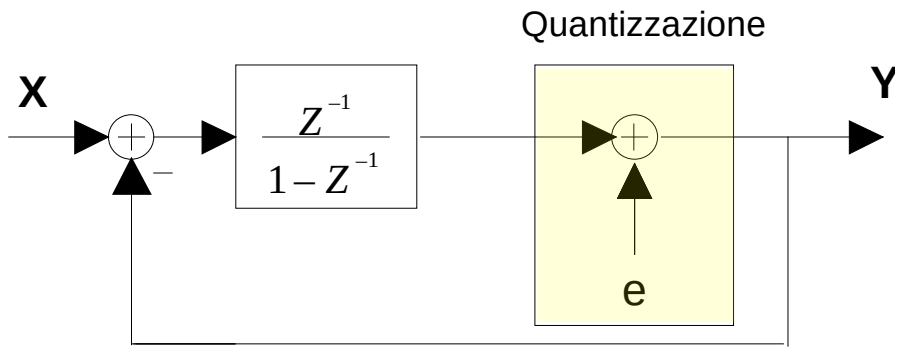


Sigma-Delta Modulation

Generalized architecture:



Linear modelling:

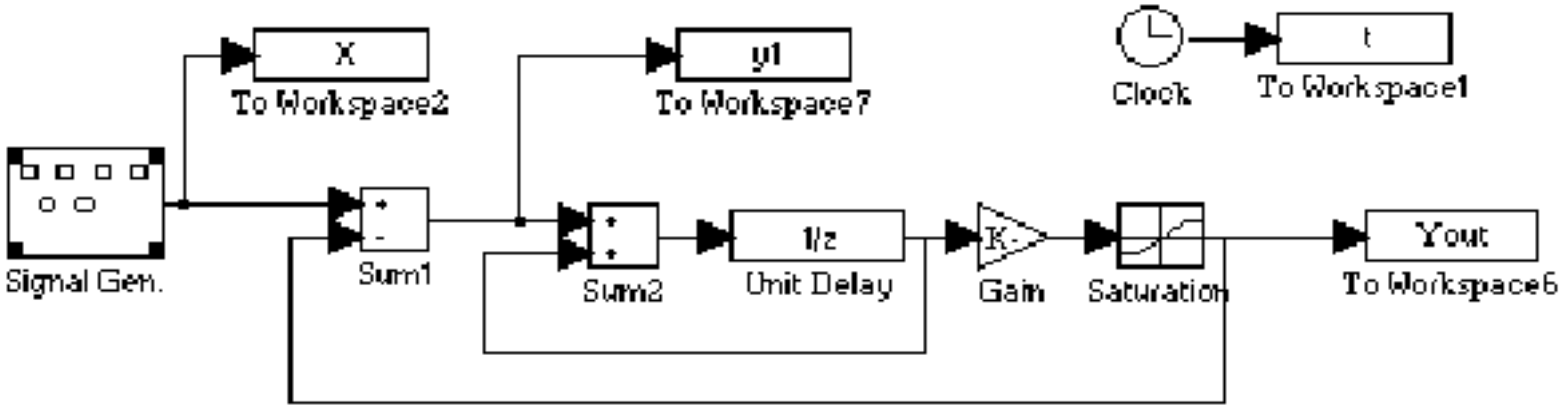


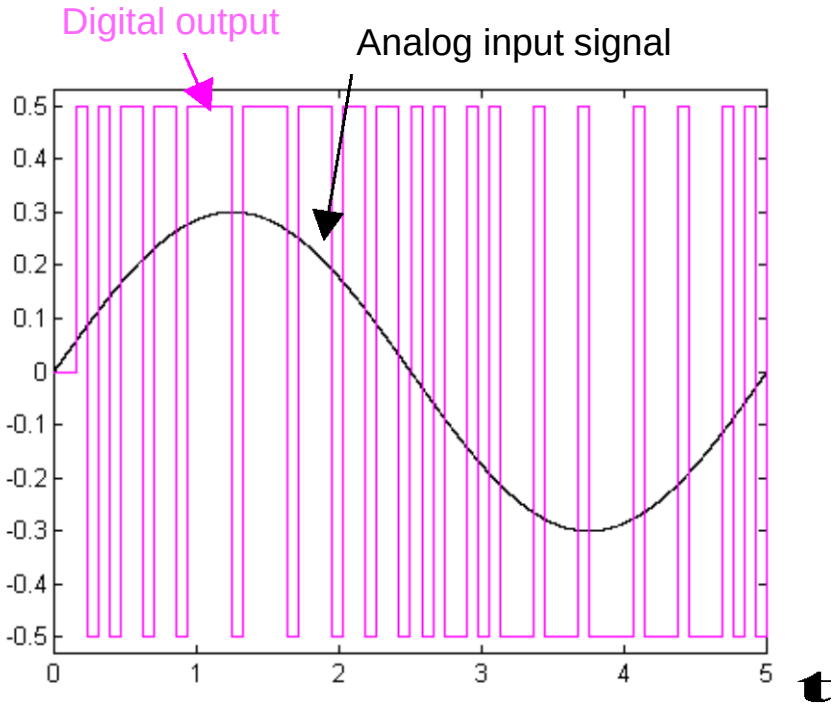
The average value of the output tracks the average value of the input signal

$$Y(z) = X(z)\frac{1}{1+\frac{1-z^{-1}}{z^{-1}}} + e(z)\frac{1-z^{-1}}{1+\frac{1-z^{-1}}{z^{-1}}} = X(z)\cdot z^{-1} + e(z)\cdot\left(1-z^{-1}\right)$$

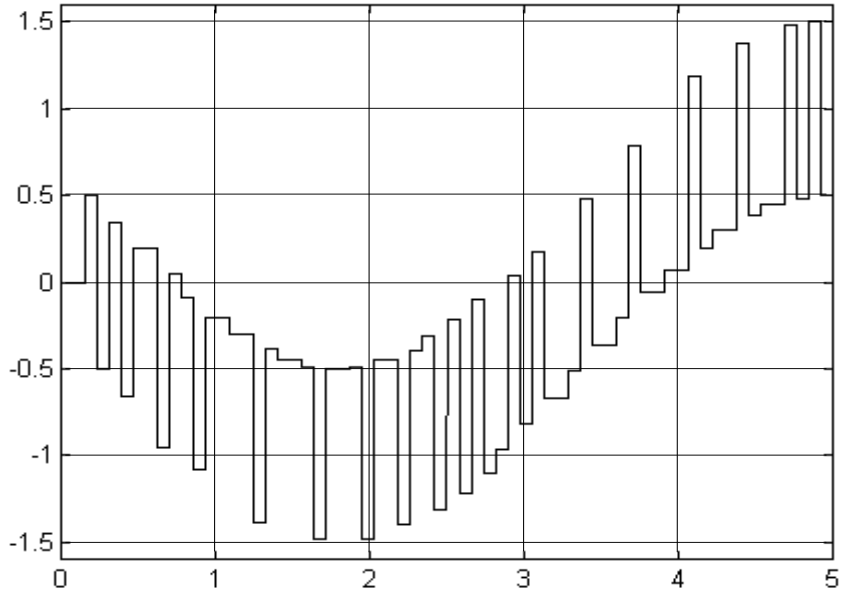
Quantization error is still present, but it is differentiated

Simulation of a Sigma-Delta modulator



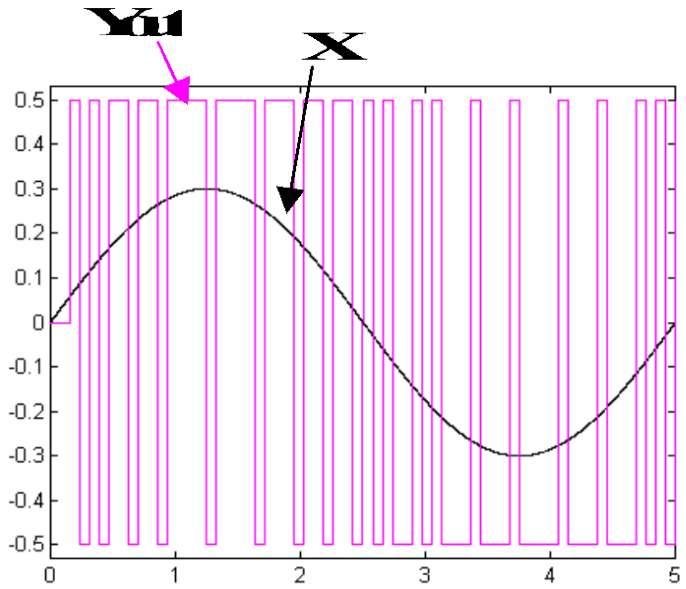


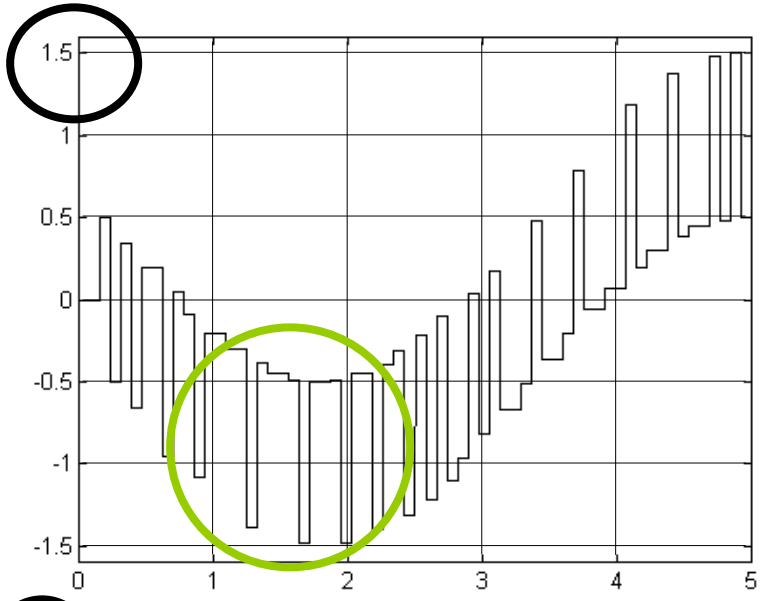
Error y_{out}-X



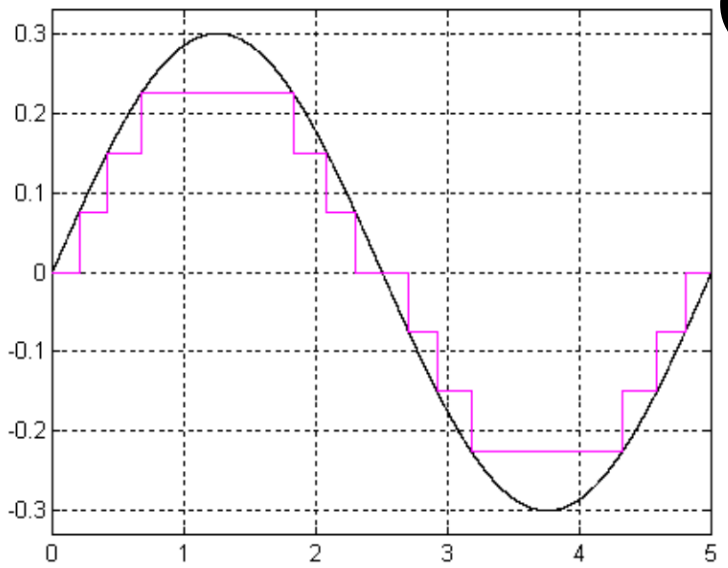
Sigma-Delta Modulation

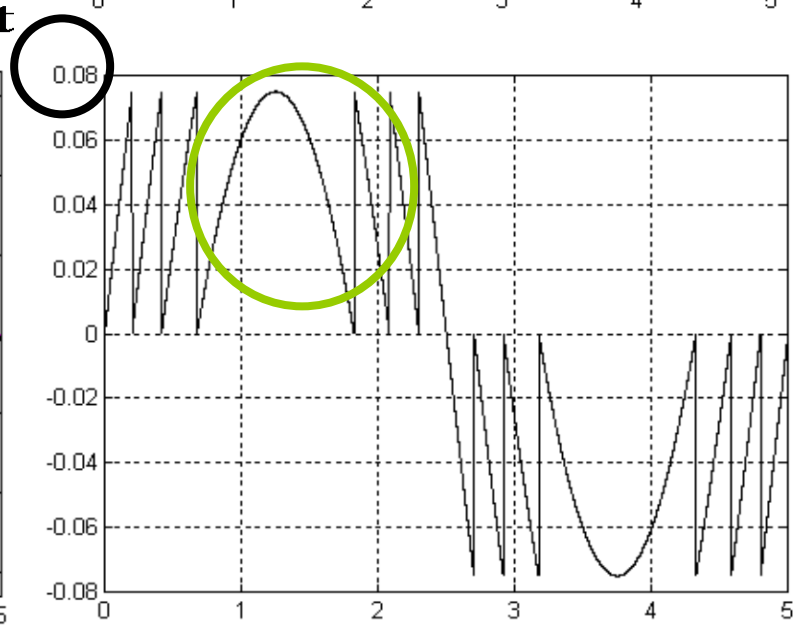
Sigma-Delta:
1bit





Classic ADC:
3bit



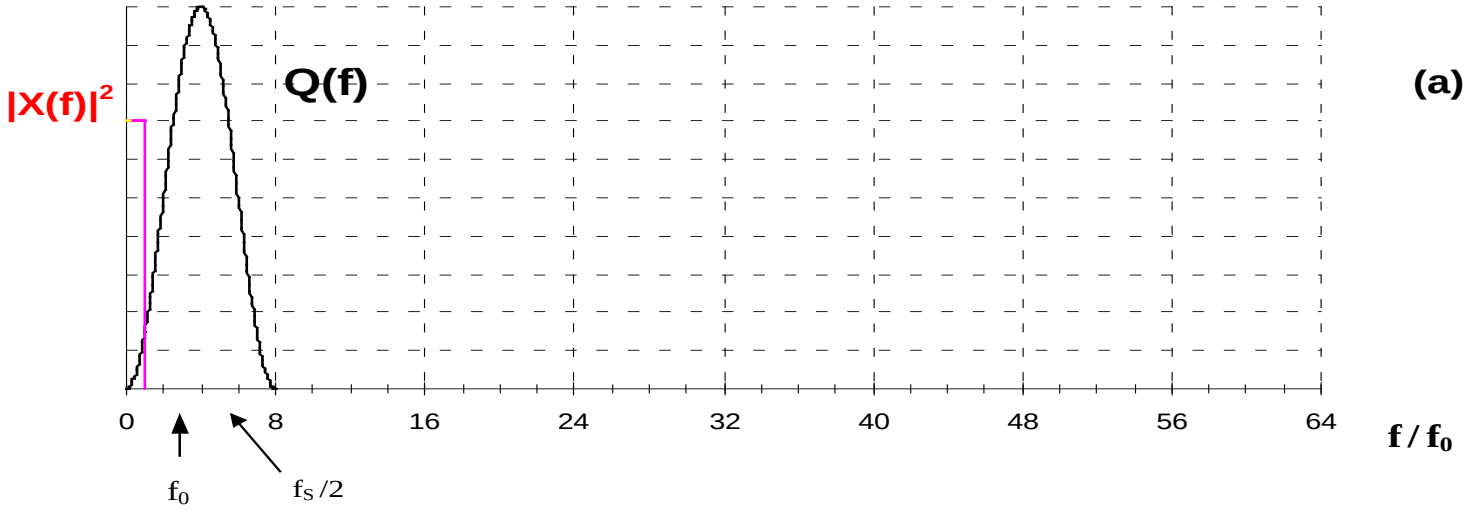


Noise shaping

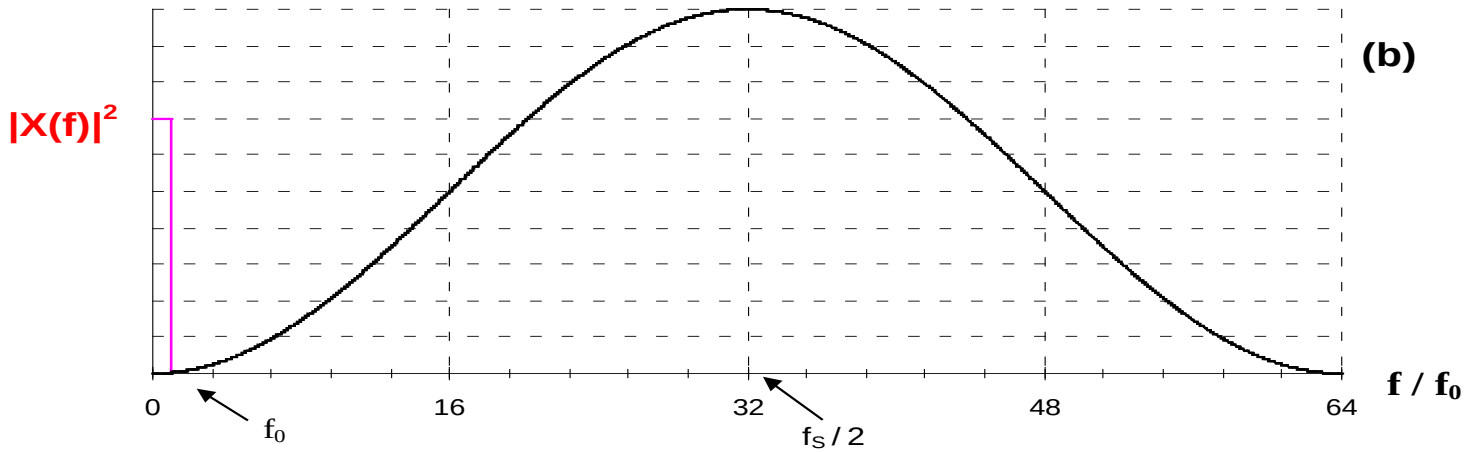
$$Y(z) = X(z) \cdot z^{-1} + e(z) \cdot (1 - z^{-1})$$

$$Q(f) = Q_0 \left| 1 - e^{j 2\pi f T} \right|^2 = 4 Q_0 \sin^2(\pi f T)$$

OS=4

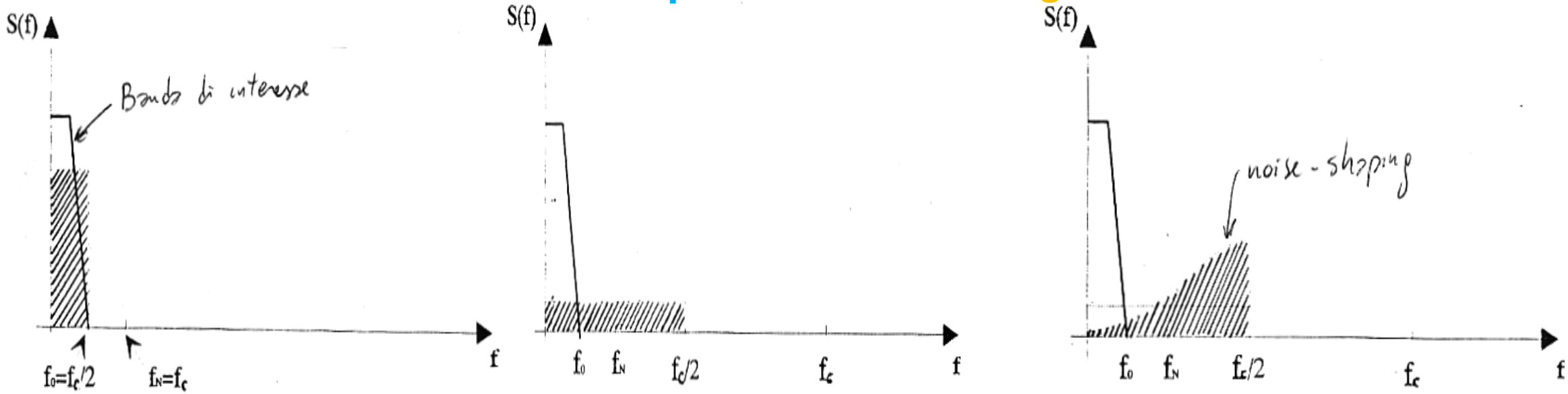


OS=32



Advantages of Sigma-Delta modulators

Classic ADC **Oversampled ADC** **Sigma-Delta modulator**



With a smart filtering of the output (at f_{max} and not at $f_S/2$):

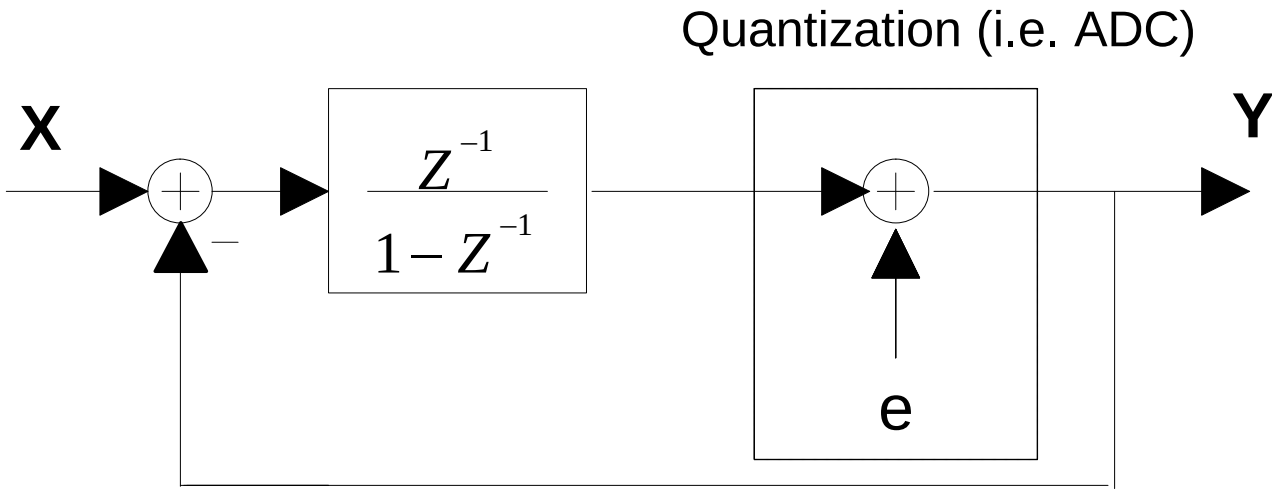
$$q^2 = \int_0^{f_0} Q(f)\,df = \int_0^{f_0} \frac{\Delta^2}{12}\frac{8}{f_s}\sin^2(\pi f T)\,df \approx \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{1}{OS^3}$$

$$SNR_{out} = SNR_{in} \cdot \frac{3}{\pi^2} \cdot OS^3$$

Improvement of 2^3 = 9dB = 1.5bit

Every doubling of the sampling frequency f_S (i.e. doubling OS) !

Sigma-Delta modulator: linearized modelling



$$Y(z) = X(z)\frac{1}{1+\frac{1-z^{-1}}{z^{-1}}} + e(z)\frac{1-z^{-1}}{1+\frac{1-z^{-1}}{z^{-1}}} = X(z)\cdot z^{-1} + e(z)\cdot\left(1-z^{-1}\right)$$

"On the average" the output is equal to the input (apart a delay)...

... of course the quantization noise is added, but **first it is differentiated**!

Sigma-Delta modulator: resolution

A Sigma-Delta with *c* bit and with $OS=2^L$:

$$SNR_{dB} = 6.02(c+1.5L) - 3.41$$

For every added bit the SNR increases of 6dB

Instead for every doubling of f_S (increment of L) the SNR increases of 9dB

What about a Sigma-Delta with more than *c* bit at the output ?

… can the SNR be better than *6.02·n+1.76* ?

There is an maximum "equivalent" number of bit after digital filtering:

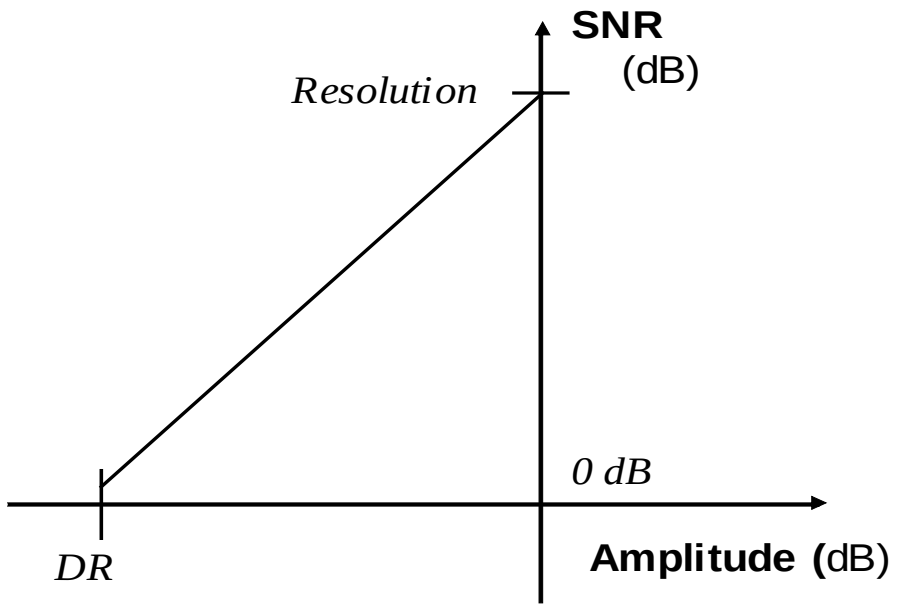
$$b = \frac{SNR + 3,41}{6,02}$$

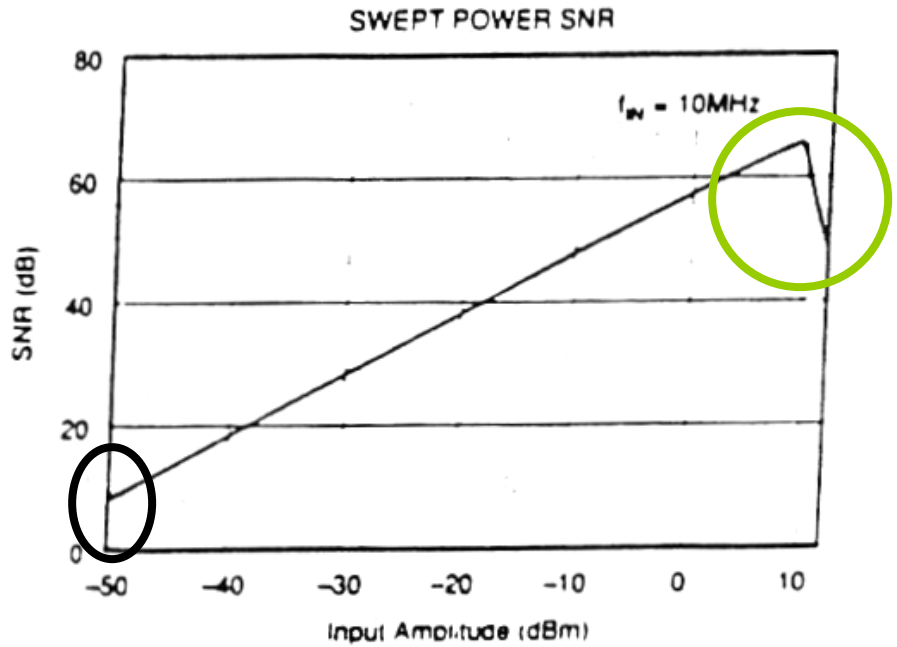
Any filtering/processing that provides a number of bits higher than b is useless, since the extra-bits are redundant, since they simply describe the quantization error !

Sigma-Delta modulator: dynamic range

SNR and Dynamic Range:

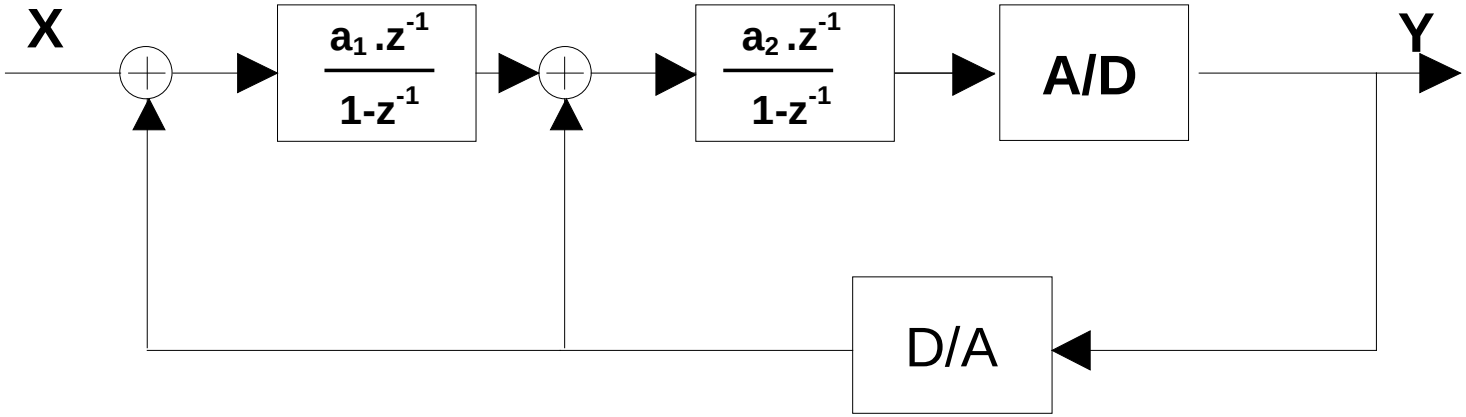
$$SNR = \frac{Vin/2}{\frac{V_{fs}}{2^c}\frac{\pi}{(OS)^{3/2}\cdot\sqrt{36}}} = Vin\cdot\frac{\sqrt{36}}{\pi}\cdot\frac{(OS)^{3/2}\cdot 2^{c-1}}{V_{fs}}$$





Sigma-Delta modulator: I and II order

Second-Order ΣΔ modulators:



$$Y(z) = X(z)\cdot z^{-2} + e(z)\cdot\left(1 - z^{-1}\right)^2$$

Noise shaping:

$$Q(f) = 16Q_0 \sin^4(\pi fT)$$

In bandwidth noise power:

$$q^2 = \int_0^{f_0} Q(f)df \approx \frac{\Delta^2}{12}\frac{\pi^4}{5}\frac{1}{OS^5}$$

Improvement:

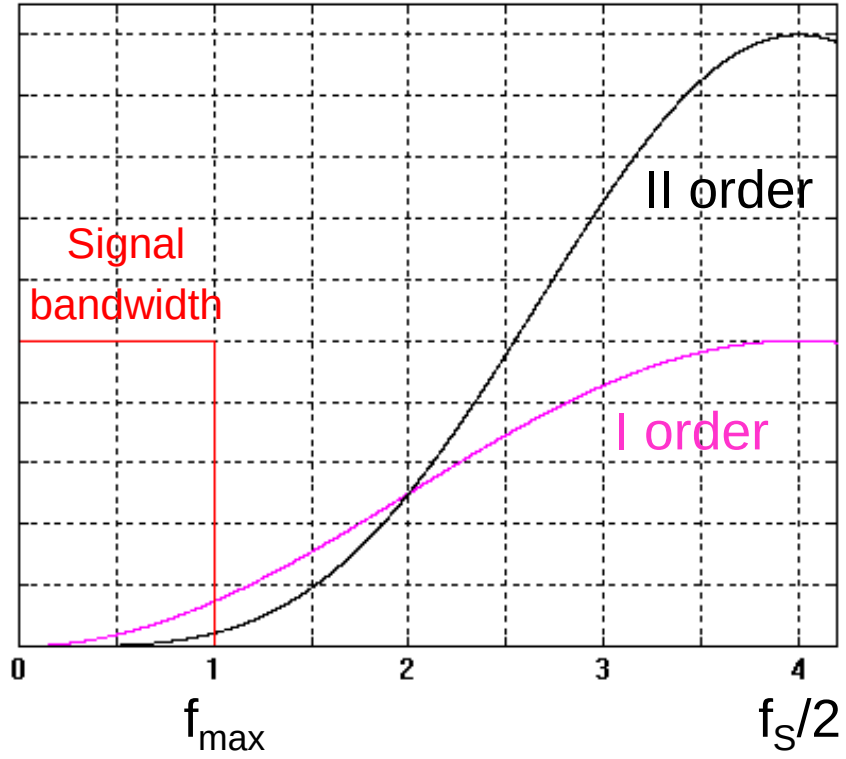
$$SNR_{dB} = 6.02\left(c + 2.5L\right) - 11.14$$

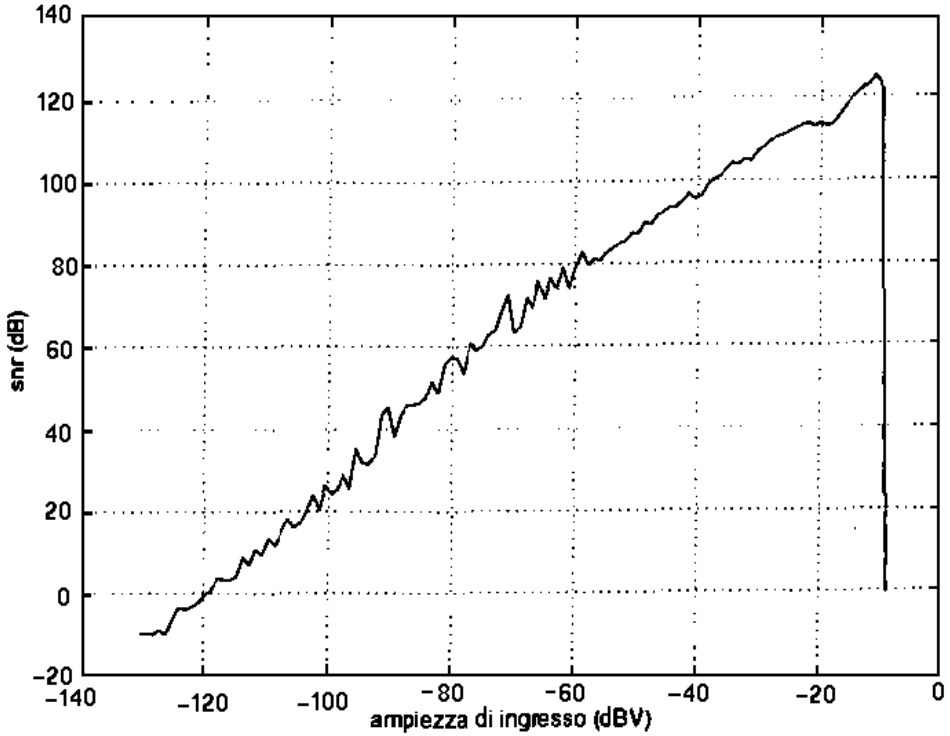
"Equivalent" bits:

$$b = \frac{SNR + 11.14}{6.02}$$

Sigma-Delta modulator: noise shaping

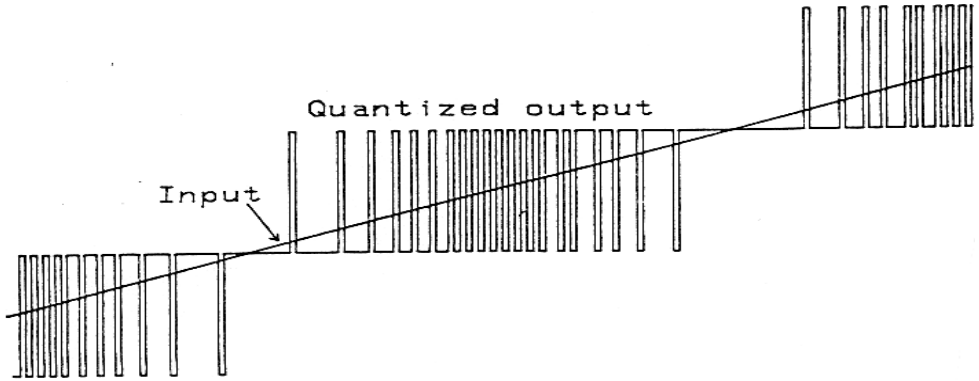
Noise shaping and Dynamic-Range of I- and II-order Sigma-Delta modulators:



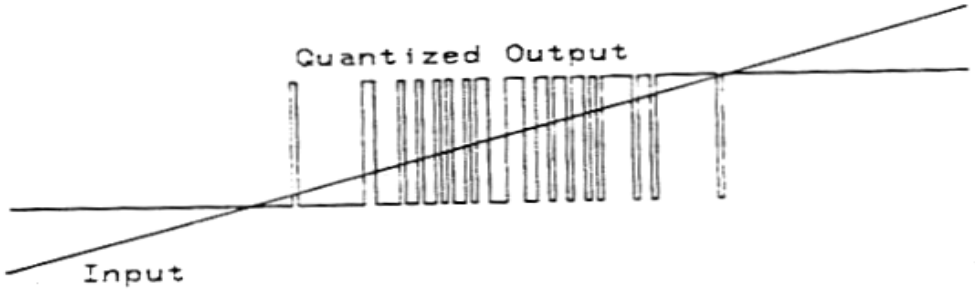


Sigma-Delta modulator: comparisons

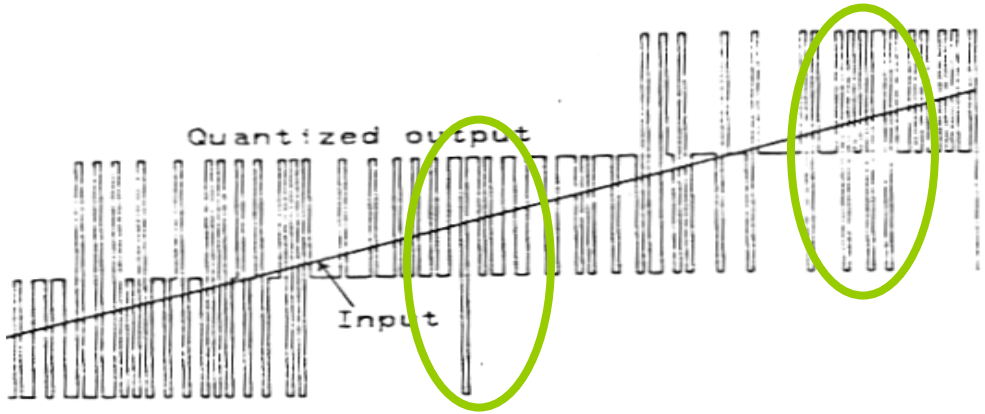
I order 2bit:



II order 1bit:



II order 2bit:



Vin=1.3V

0 2 1 2 1 1 2 1 1 2 0 2 2 0 2 2 0 2 1 2
1 1 1 2 1 1 2 0 3 0 2 1 1 2 1 1 2 1 1 1
2 1 2 0 2 2 0 2 1 2 0 3 0 2 1 1 1 2 2 0
2 1 1 2 1 1 2 1 1 1 2 1 2 0 2 1 2 1 1 2
0 2 2 0 2 2 0 2 1 2 1 1 1 2 1 1 2 1 1 1
2 1 1 2 1 1 2 1 1 1 2 1 2 0 2 2 0 2 1 2
1 1 1 2 1 1 1 2 2 0 2 1 1 2 1 1 2 1 1 1
2 1 2 0 2 2 0 2 1 2 0 2 2 1 1 1 1 2 1 2
1 1 1 2 1 1 2 1 1 1 2 1 1 2 1 1 2 1 1 1
2 1 2 0 2 2 0 2 1 2 1 1 1 2 1 1 2 0 3 0

Recap

Oversampled ADC

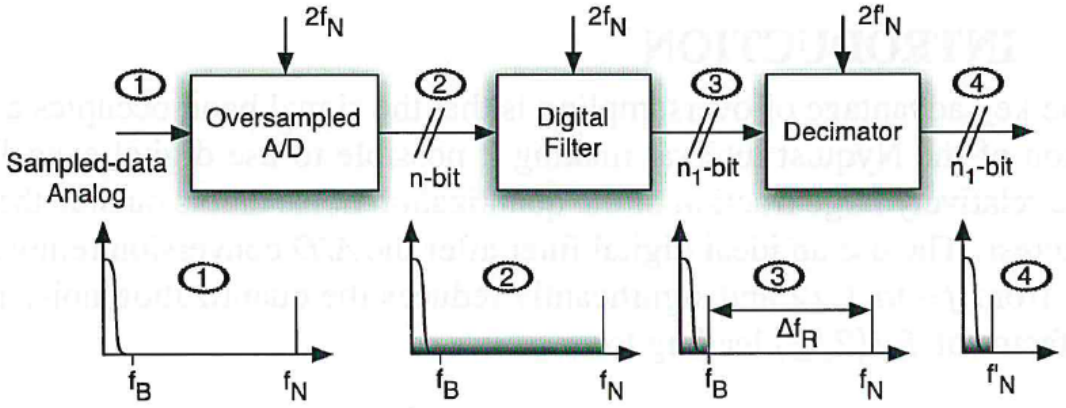


Figure 6.1. Out-of-band noise rejection and decimation of an over-sampled signal.

Sigma-Delta modulator

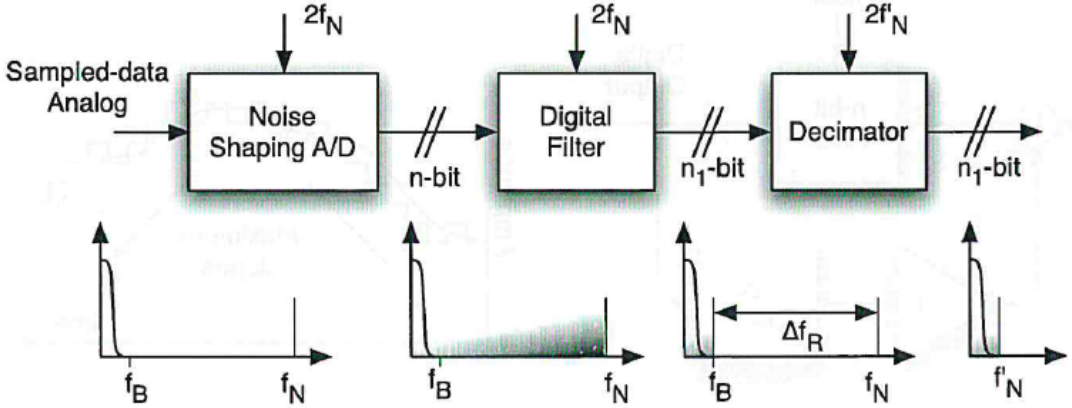


Figure 6.4. Out-of-band noise rejection and decimation of a noise shaped signal.

Detailed discussion:

"*Chapter 2 - Oversampling and low-order ΣΔ modulators*"

"**Data Converters**", prof. Franco Maloberti

Modelling and Simulations

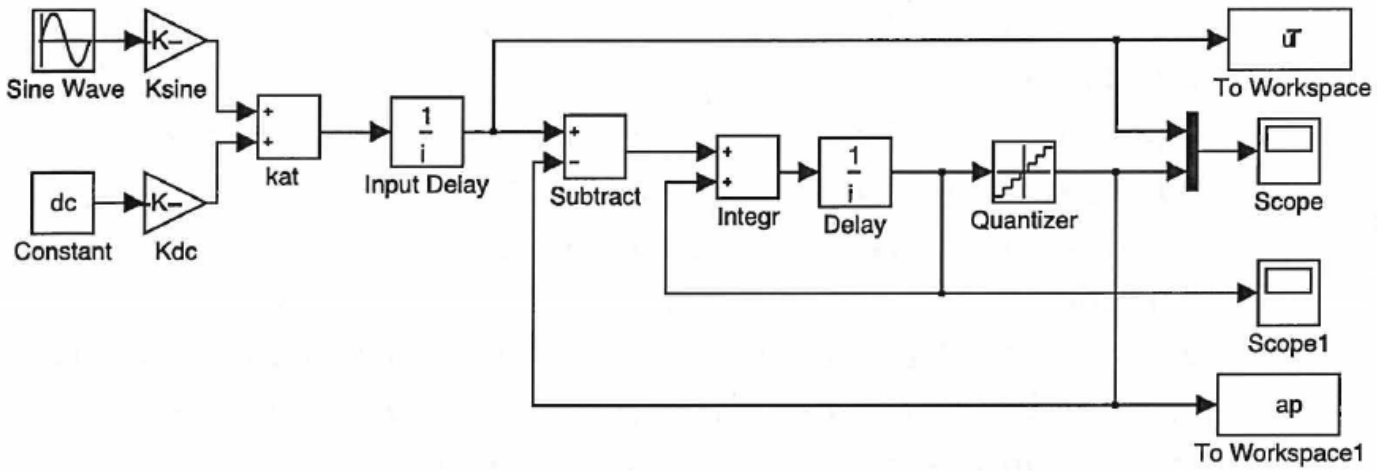


Figure 6.7. Behavioral scheme of the first order sigma-delta modulator.

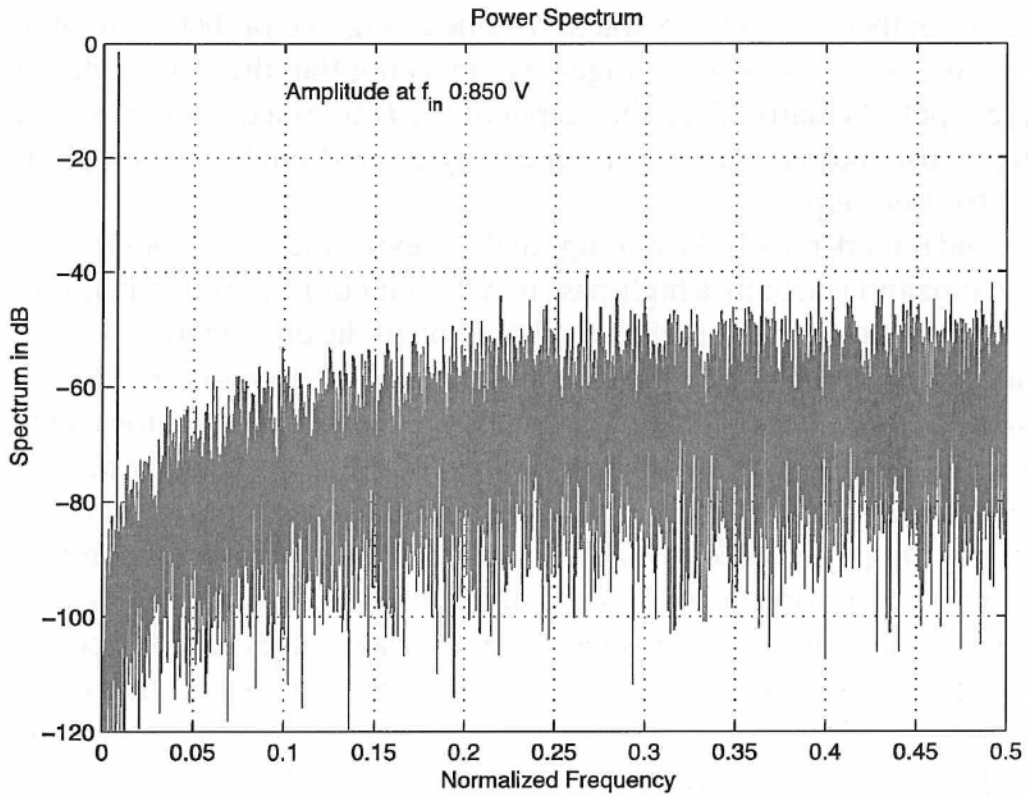
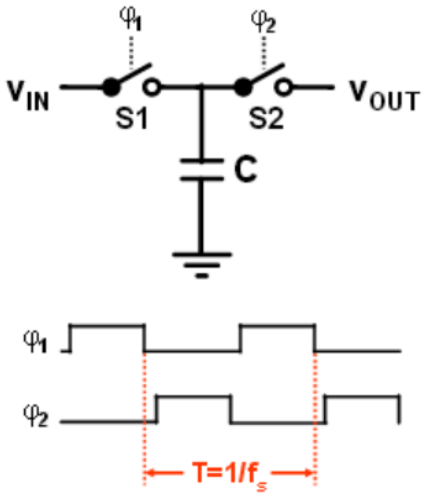


Figure 6.8. FFT of a 16384 sequence of the output bit-stream made by 131 sine waves periods.

"*Oversampling and low-order ΣΔ modulators*"
"Data Converters", prof. Franco Maloberti

How to design a R in a time-discrete world: Switched-Capacitor



In time-discrete operation, charge transfer from V_{IN} to V_{OUT} during each clock cycle is:

$$Q = C \cdot (V_{IN} - V_{OUT})$$

Hence, the "average" current is:

$$I = \frac{Q}{T} = f_S \cdot C \cdot (V_{IN} - V_{OUT})$$

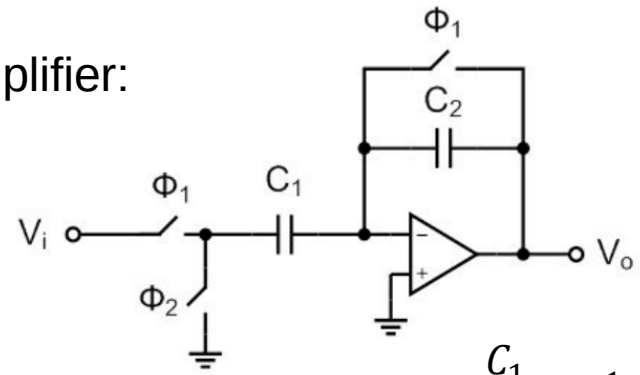
Instead, in time-continous operation, a Resistor would provide:

$$I = \frac{(V_{IN} - V_{OUT})}{R}$$

Therefore, we may say that:

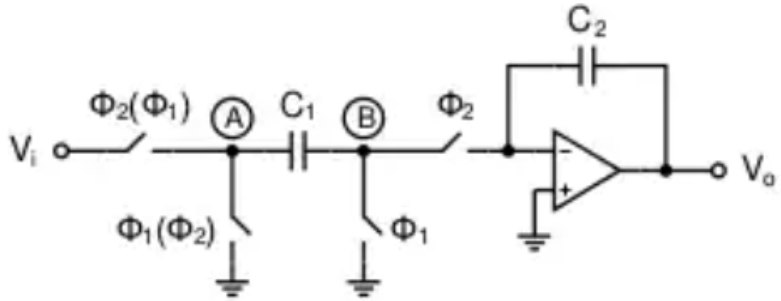
$$R = \frac{1}{f_S \cdot C}$$

Examples of SC amplifier:



$$G(z) = +\frac{C_1}{C_2} \cdot z^{-1}$$

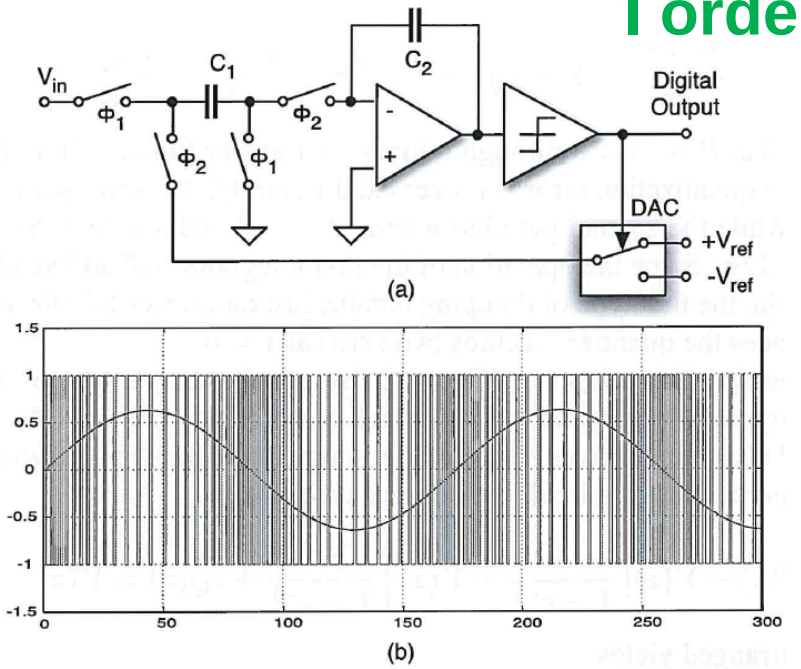
It is possible to play with many different SC configurations and clock schemes, to invert gain and/or in-out delay (z^{-1})



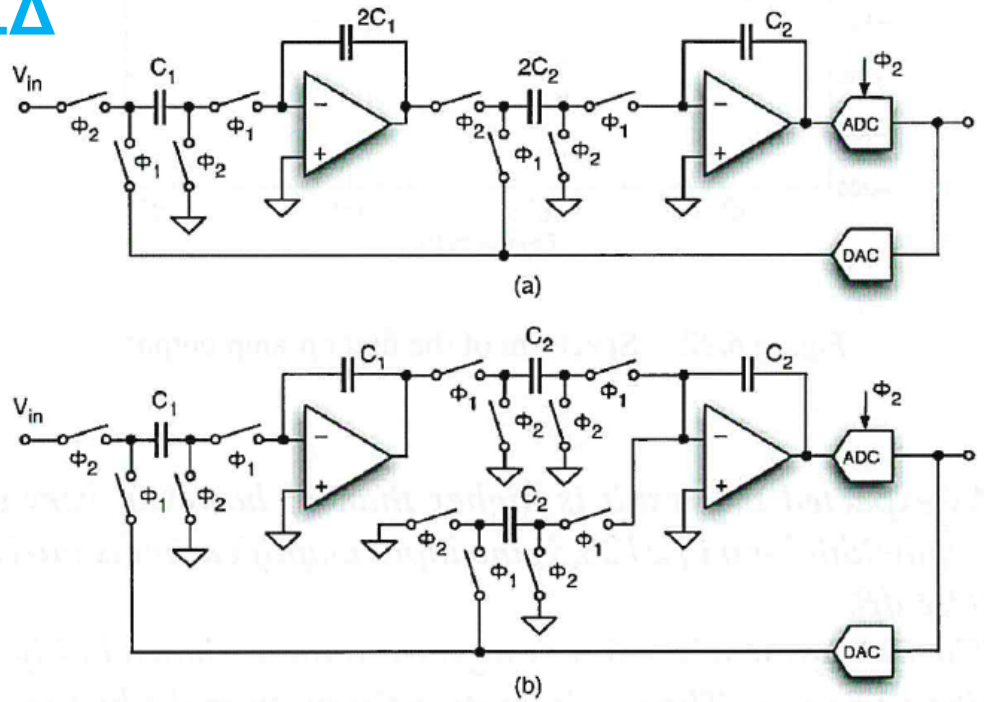
$$G(z) = -\frac{C_1}{C_2} \cdot \frac{1}{1 - z^{-1}} \qquad \left(G(z) = +\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}\right)$$

Switched-Capacitor implementations

I order ΣΔ

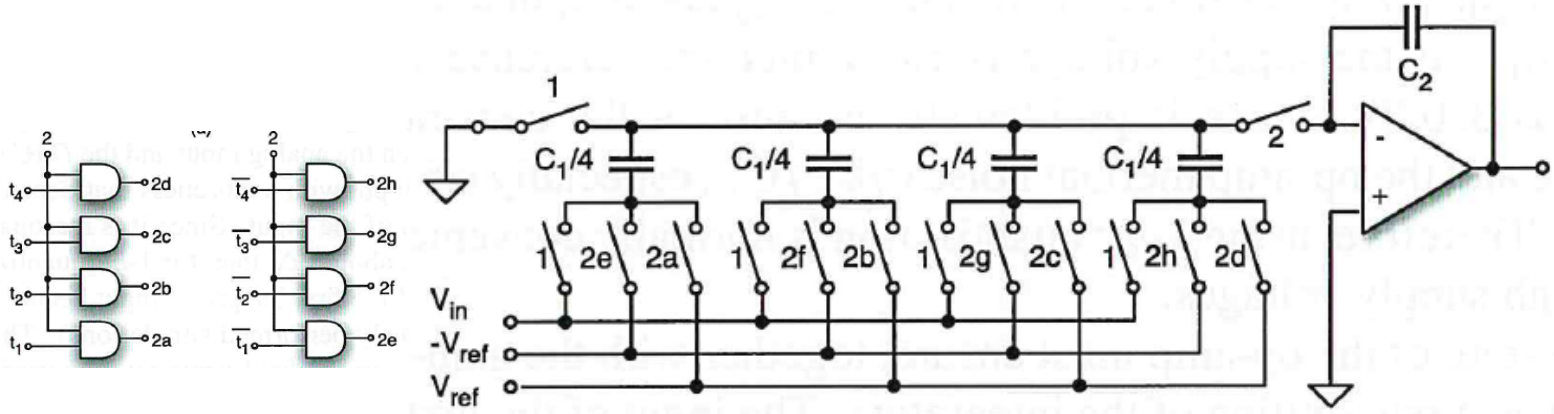


II order ΣΔ



Multi-Bit integrator

(from a 2bit thermometric code)



"*Oversampling and low-order ΣΔ modulators*"

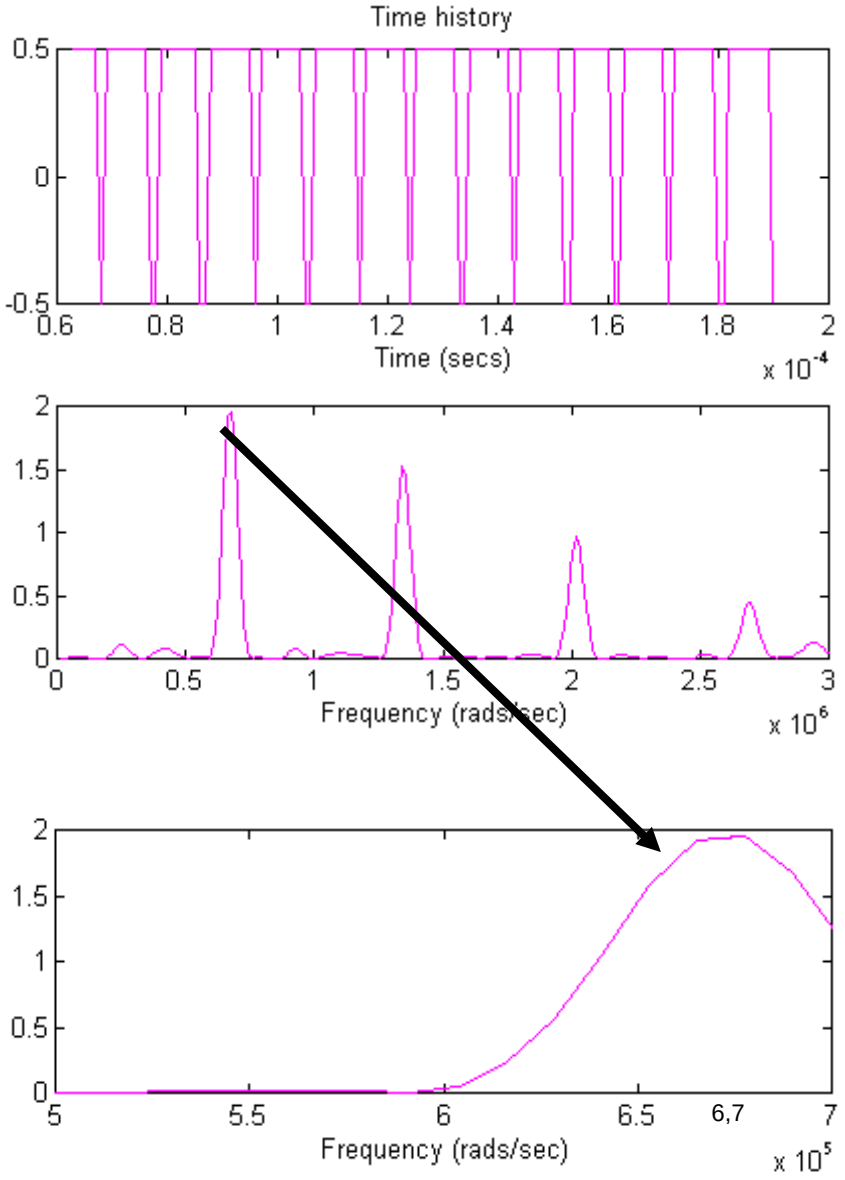
"Data Converters", prof. Franco Maloberti

New issue: "*Pattern Noise*"

Example:

f_0=20kHz f_S=320kHz OS=8

with a constant input v_{in}=0.33V the output becomes periodic:



Hence there is a tone at 106kHz, luckily out of band...

... but with other values the main tone may lower below the filter bandwidth f_{max}

For example with v_{in}=1/16 FSR we get a tone at 1/16·f_S=20kHz

Pattern Noise

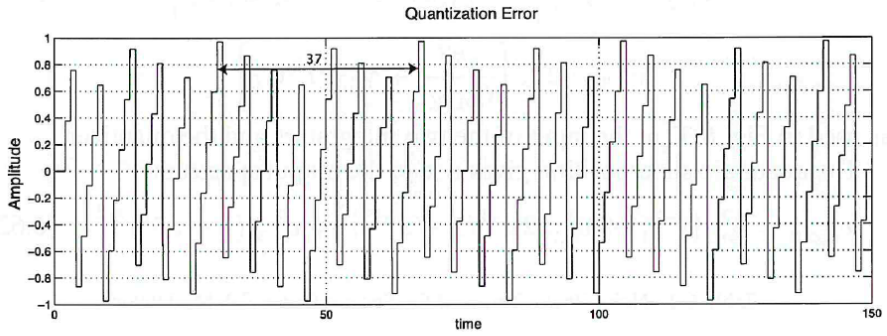
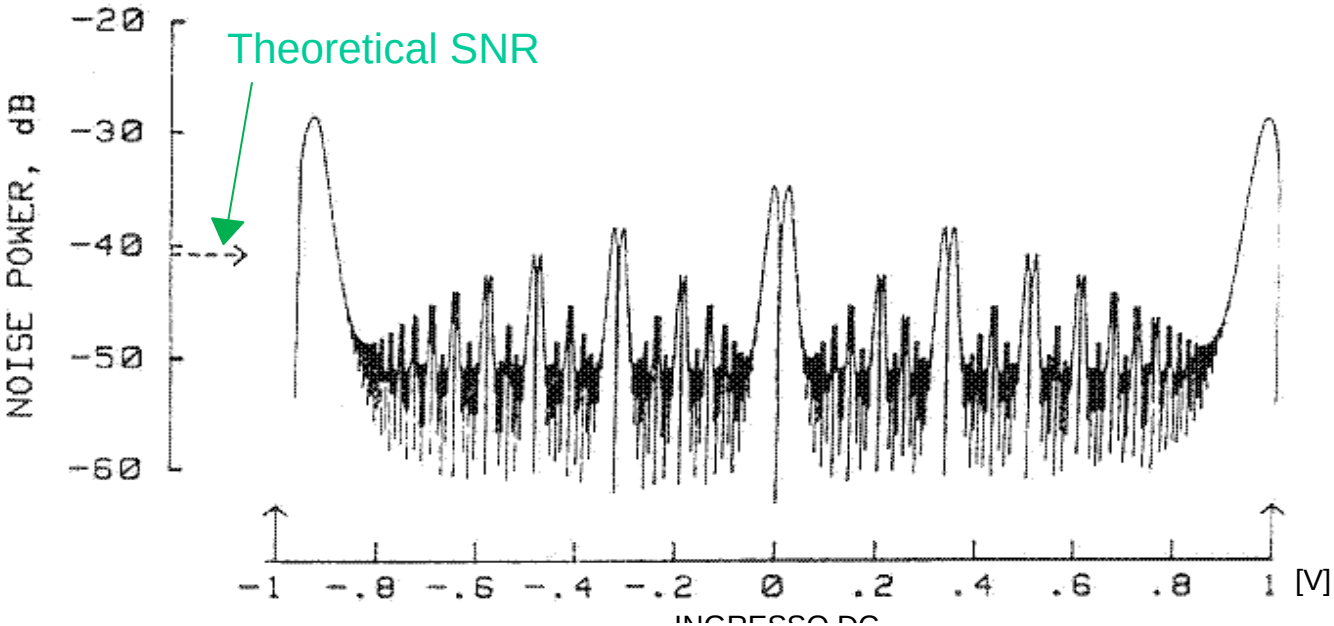
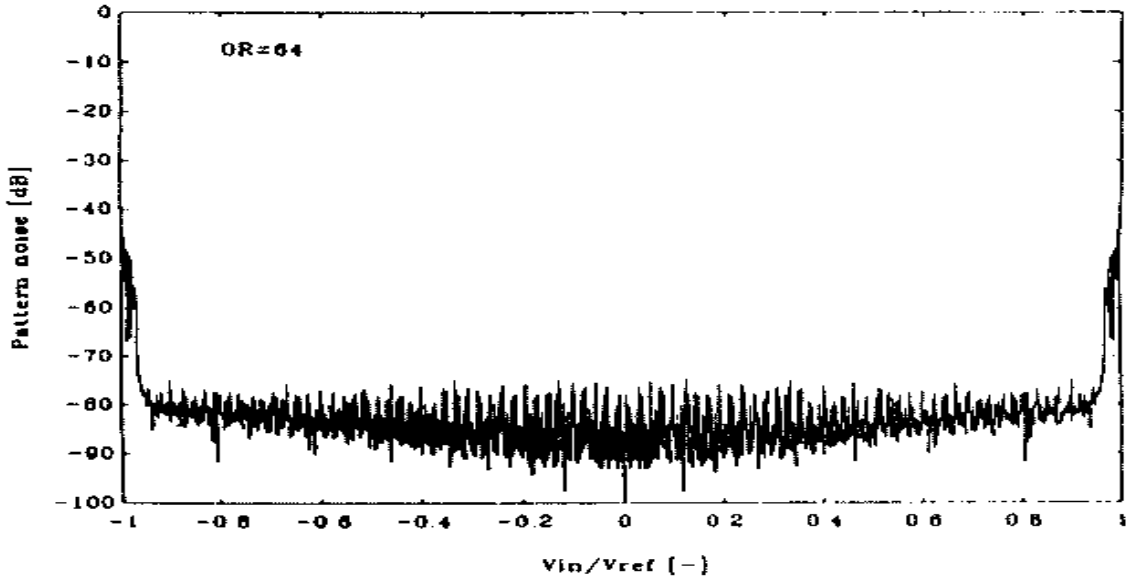


Figure 6.33. Quantization error of a first order ΣΔ with $V_{in} = 23/37$ and $V_{ref} = \pm 1$.

I order:

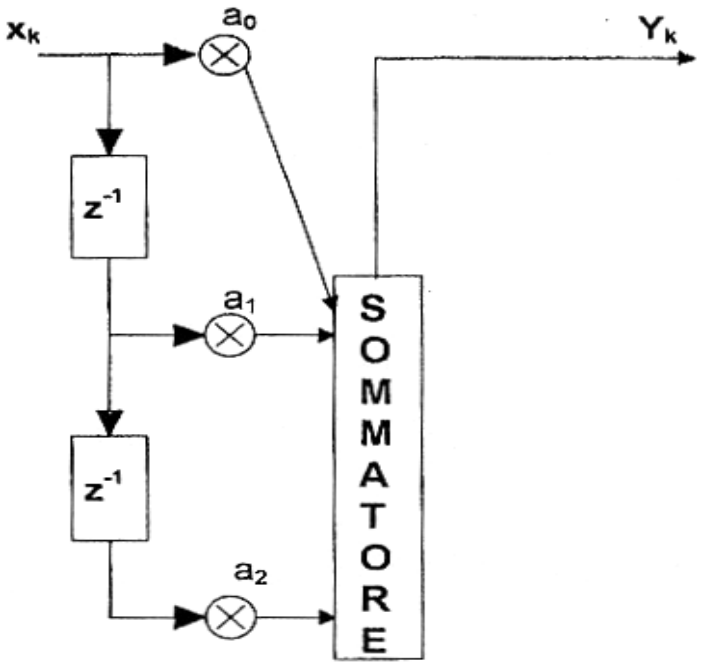


II order:



Digital Filtering: possible implementations

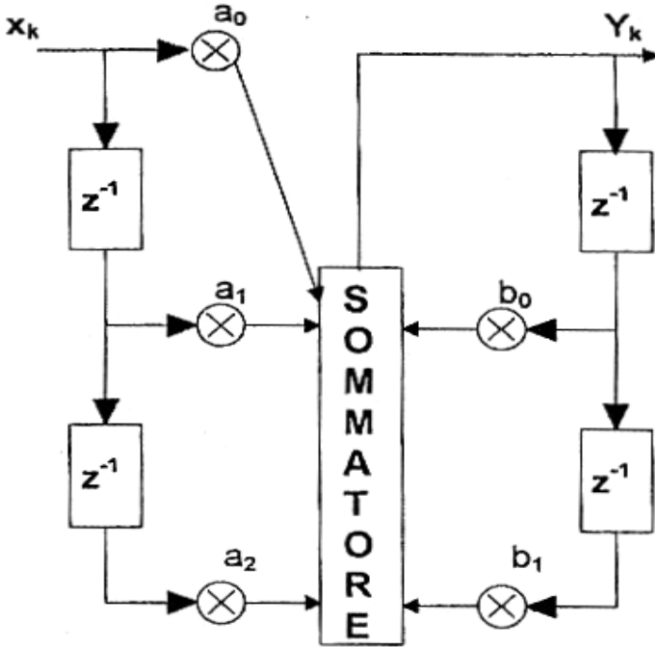
FIR: Finite Impulse Response



$$y_K = \sum_{i=0}^{N} a_i \cdot x_{k-i}$$

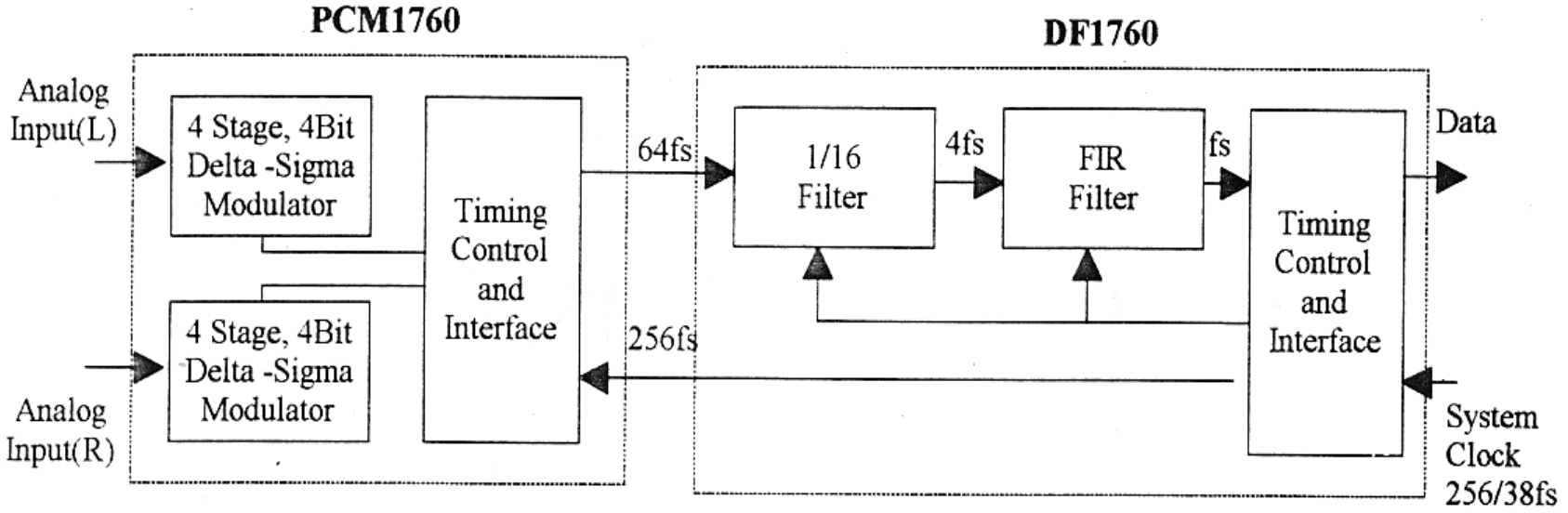
- It processes a finite number of samples
- its time response in limited in time
- it provides only **ZEROES**
- it is **always STABLE**

IIR: Infinite Impulse Response



$$y_K = \sum_{i=0}^{N} a_i \cdot x_{k-i} - \sum_{j=0}^{M} b_i \cdot y_{k-j}$$

- It process all infinite past samples
- its time response lasts to infinite time
- it provides **both POLES and ZEROES**
- It **can be UNSTABLE**



- IV order 4bit ΣΔ modulators
- 64-fold oversampling
- two stage FIR digital filter (first decimation 16, second decimation 4)
- overall resolution is 20bit

PARAMETER	CONDITIONS	PCM1760/DF1760 MIN	TYP	MAX	UNITS
ACCURACY					
Gain Error			±0.5	±1.0	dB
Gain Mismatch				±0.5	dB
Bipolar Zero Error	V_{IN} = 0 at 20s Afeter Power-On			±0.4	%FSR(2)
Gain Drift	0°C to +70°C		±100		ppm/°C
Bipolar Zero Drift	0°C to +70°C		±20		ppm/°C

NOTES: (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR=5V.

PARAMETER	CONDITION	TEMP	ADS801U MIN	TYP	MAX	UNITS
ACCURACY(2)						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.0	±2.5	%
Gain Tempco				±85		ppm/°C
Power Supply Rejection Gain	Delta +V_s=±5%	+25°C		0.03	0.15	%FSR%
Input Offset Error		+25°C		±2.0	±2.5	%
		Full		±2.1	±3.0	%FSR%
Power Supply Rejection Offset	Delta +V_s=±5%	+25°C		00.5	0.15	%FSR%

NOTE: (2) Percentage accuracies are referred to the internal A/D Full Scale Range of 4Vp-p.

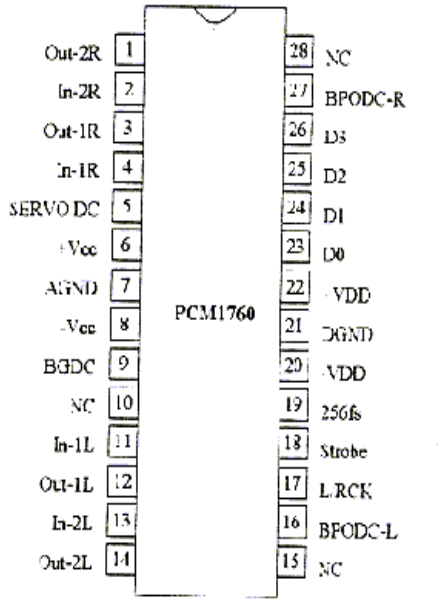
Data-sheet

PARAMETER		CONDITIONS	PCM1760/DF1760 MIN	TYP	MAX	UNITS
DYNIMIC CHARACTERISTICS(4)						
TDH+N/(0dBFS)	P,U	f_{IN} =1kHz		-92	-90	dB
	P-L, U-L			-90	-88	dB
TDH+N/(-20dBFS)	P,U	f_{IN} =1kHz		-76	-70	dB
	P-L, U-L			-76	-70	dB
TDH+N/(-60dBFS)	P,U	f_{IN} =1kHz		-44	-42	dB
	P-L,U-L			-44	-42	dB
Dynamic Range	P,U	f_{IN} =1kHz, V_{IN} =-60dBFS	104	108		dB
	P-L,U-L		104	108		dB
SNR	P,U	V_{IN} =-0. A Filter	108	110		dB
	P-L,U-L		106	110		dB
Frequency response		f_{IN} =20kHz		±0.1		dB
Channel Separation		f_{IN} =1kHz, A Filter	94	98		dB

NOTES: (4) Average response using a 20-bit reconstruction DAC with 20 kHz low-pass filter and 400 Hz high-pass filter.

PIN ASSIGNEMENT PCM1760

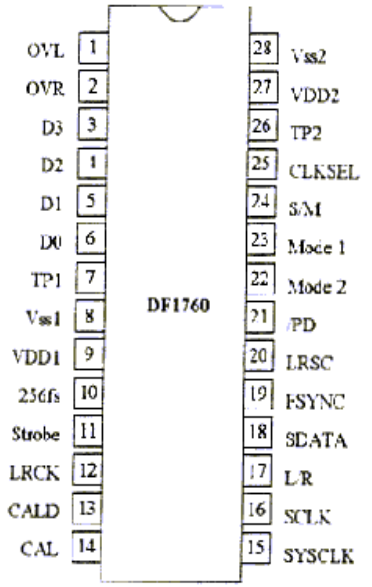
TOP VIEW SOIC/D



PIN	NAME	DESCRIPTION
1	Out-2R	Right Channel Second Integrator Output
2	In-2R	Right Channel Second Integrator Input
3	Out-1R	Right Channel First Integrator Output
4	In-1R	Right Channel First Integrator Input
5	SERVO DC	Servo Amp Decoupling Capacitor
6	+Vcc	+5V Analog Supply Voltage
7	AGND	Analog Common
8	-Vcc	-5V Analog Supply Voltage
9	BGDC	Band Gap Reference Decoupling Capacitor
10	NC	No Connection
11	In-1L	Left Channel First Integrator Input
12	Out-1L	Left Channel First Integrator Output
13	In-2L	Left Channel Second Integrator Input
14	Out-2L	Left Channel Second Integrator Output
15	NC	No Connection
16	BPODC-L	Left Channel Bipolar Offset Decoupling Capacitor
17	LRCK	LR Clock Output (64fs)
18	Strobe	Data Strobe Output (128fs)
19	256fs	256fs Clock Input
20	$-V_{DD}$	-5V Digital Supply Voltage
21	DGND	Digital Common
22	$-V_{DD}$	+5V Digital Supply Voltage
23	D0	D0 Data Output (LSB)
24	D1	D1 Data Output
25	D2	D2 Data Output
26	D3	D3 Data Output (MSB)
27	BPODC-R	Right Channel Bipolar Offset Decoupling Capacitor
28	NC	No Connection

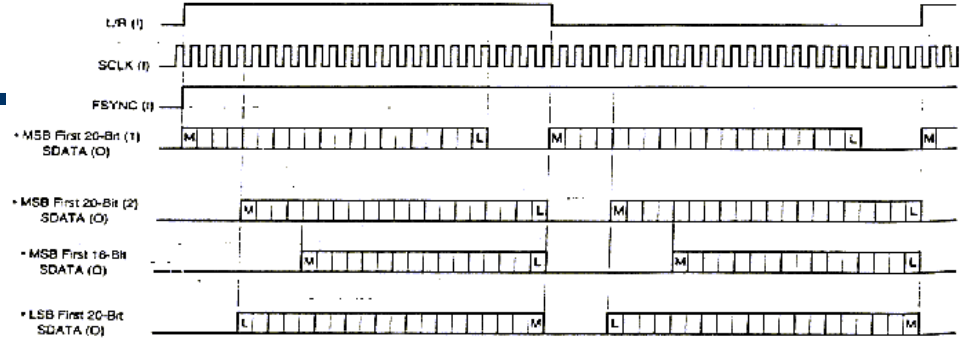
PIN ASSIGNEMENT DF1760

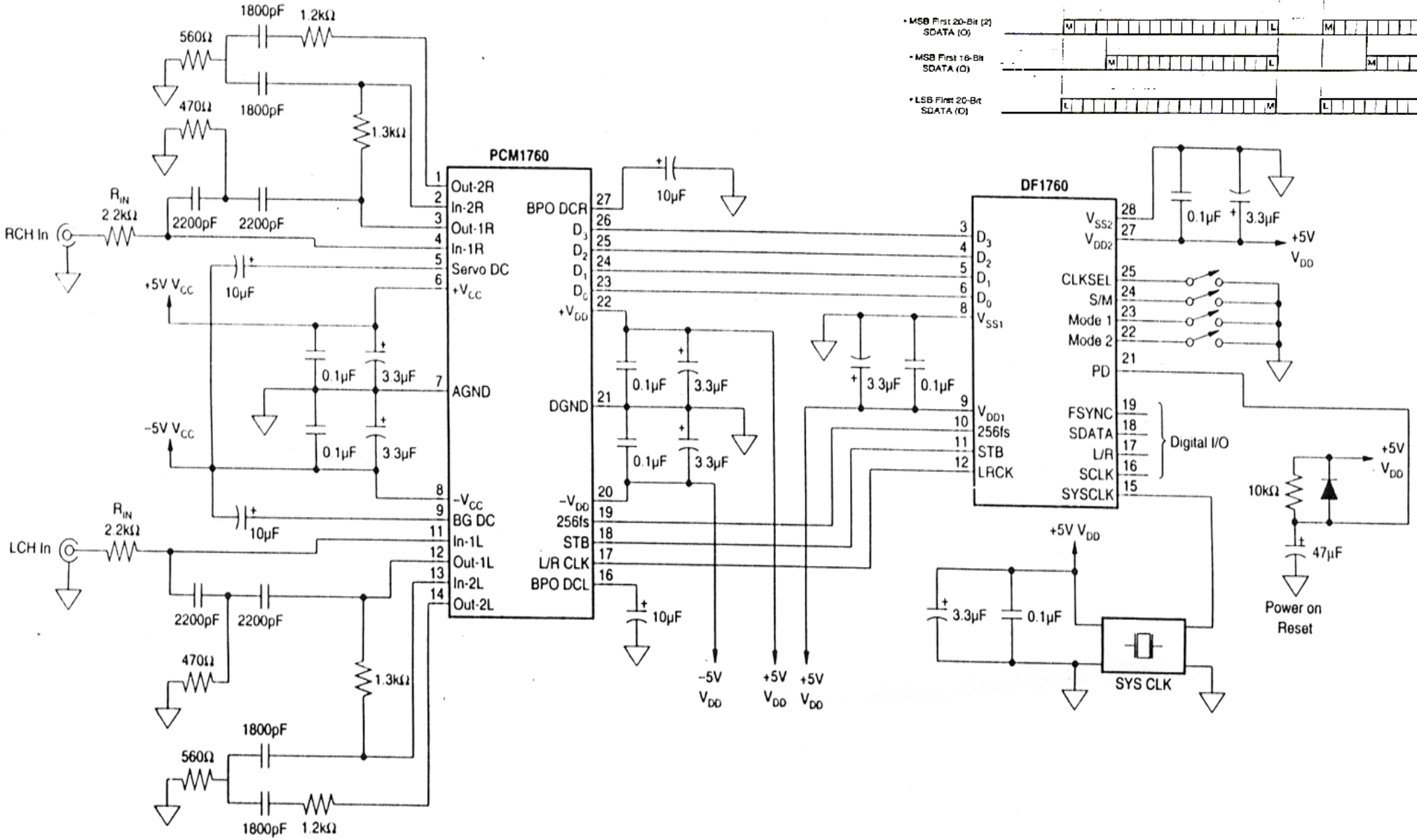
TOP VIEW SOIC/D

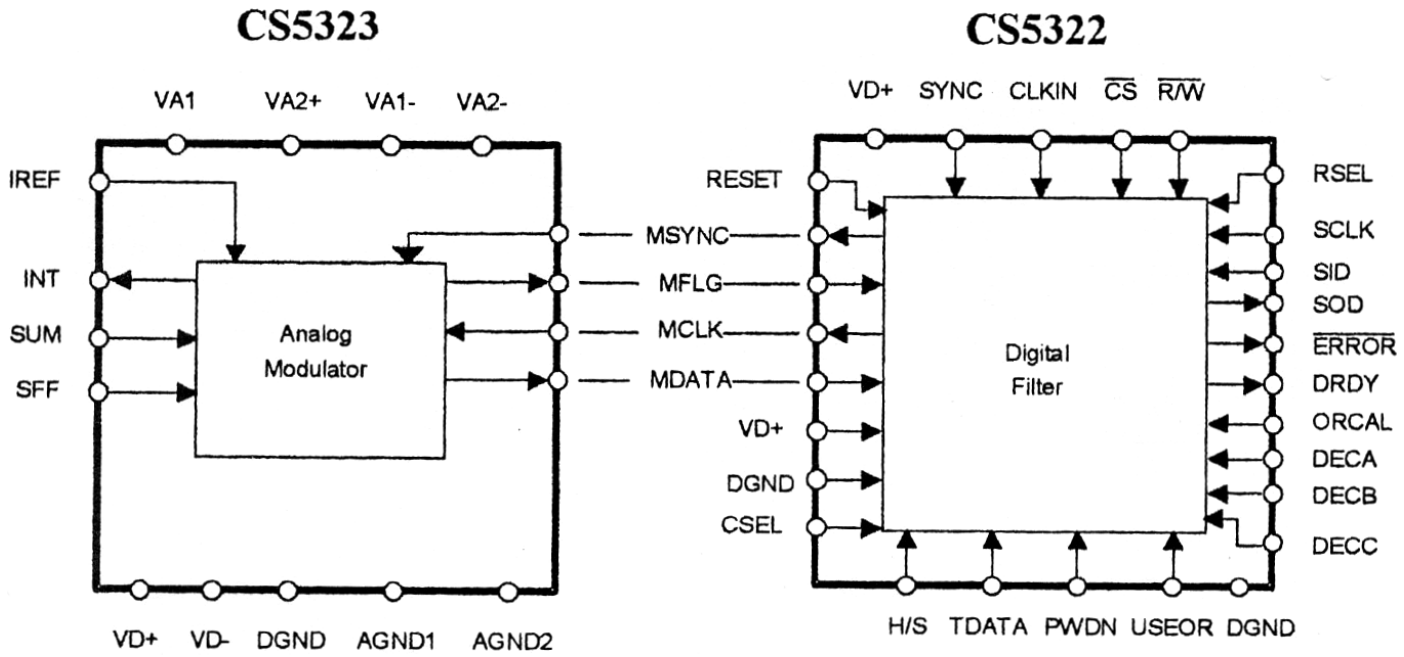


PIN	NAME	DESCRIPTION
1	OVL	Left Channel Overflow Output (Active High)
2	OVR	Right Channel Overflow Output (Active High)
3	D3	D3 Data Input (MSB)
4	D2	D2 Data Input
5	D1	D1 Data Input
6	D0	D0 Data Input (LSB)
7	TP1	Test Pin (No Connection)
8	V_{SS1}	Common Channel 1
9	V_{DD1}	+5V Channel 1
10	256fs	256fs Clock Output
11	Strobe	Data Strobe Clock Input (128fs)
12	LRCK	LR Clock Input
13	CALD	Calibration Function Enable (Active Low)
14	CAL	Calibration Output (High During Calibration)
15	SYSCLK	System Clock Input (256fs or 348fs)
16	SCLK	Data Clock
17	L/R	LR Channel Phase Clock
18	SDATA	Serial Data Output (1fs)
19	FSYNC	Frame Clock (2fs)
20	LRSC	Phase Control or LR Channel Phase Clock
21	/PD	Power Down Mode Enable Input (Active low)
22	Mode 2	Output Format Selection Input 2
23	Mode 1	Output Format Selection Input 1
24	S/M	Slave/Master Mode Selection Input (High Makes Slave Mode
25	CLKSEL	System Clock Selection Input (High Makes 256fs)
26	TP2	Test Pin (No Connection)
27	V_{DD2}	+5V Channel 2
28	V_{SS2}	Common Channel 2

Data-sheet

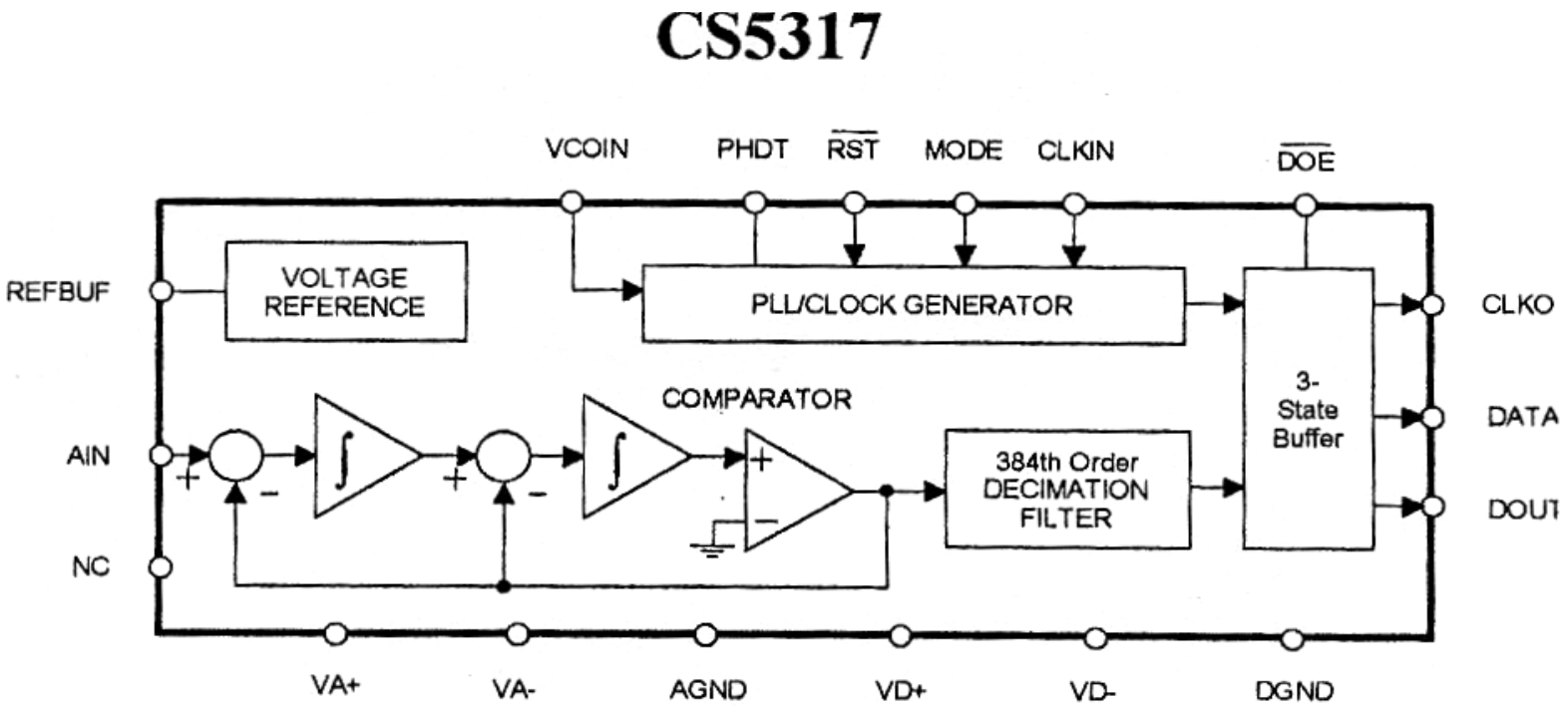

L/R (I)
SCLK (I)
FSYNC (I)
• MSB First 20-Bit (1) SDATA (O)
• MSB First 20-Bit (2) SDATA (O)
• MSB First 16-Bit SDATA (O)
• LSB First 20-Bit SDATA (O)
M
L


PCM1760
DF1760
RCH In
LCH In
R_{IN} 2.2kΩ
1800pF
1.2kΩ
560Ω
470Ω
1.3kΩ
2200pF
10µF
0.1µF
3.3µF
+5V V_{CC}
-5V V_{CC}
Out-2R
In-2R
Out-1R
In-1R
Servo DC
+V_{CC}
AGND
-V_{CC}
BG DC
In-1L
Out-1L
In-2L
Out-2L
BPO DCR
D_3
D_2
D_1
D_0
+V_{DD}
DGND
-V_{DD}
256fs
STB
L/R CLK
BPO DCL
V_{SS2}
V_{DD2}
CLKSEL
S/M
Mode 1
Mode 2
PD
V_{SS1}
V_{DD1}
LRCK
FSYNC
SDATA
L/R
SCLK
SYSCLK
Digital I/O
+5V V_{DD}
-5V V_{DD}
10kΩ
47µF
Power on Reset
SYS CLK



- III order ΣΔ modulator
- filtering with two FIR stages
- variable oversampling between 64 to 4096
- 24bit output

POLITECNICO MILANO 1863



- one-chip with both modulator and digital filter
- II order ΣΔ modulator
- FIR filtering with *sinc* response
- 128-fold oversampling
- 16bit output

Example of an application

- CS5516 at 16bit and 60sps (CS5520 at 20bit)
- both modulator, digital filter, INA with 25x gain, PGA, 4bit DAC (offset comp), ref. voltage generator…

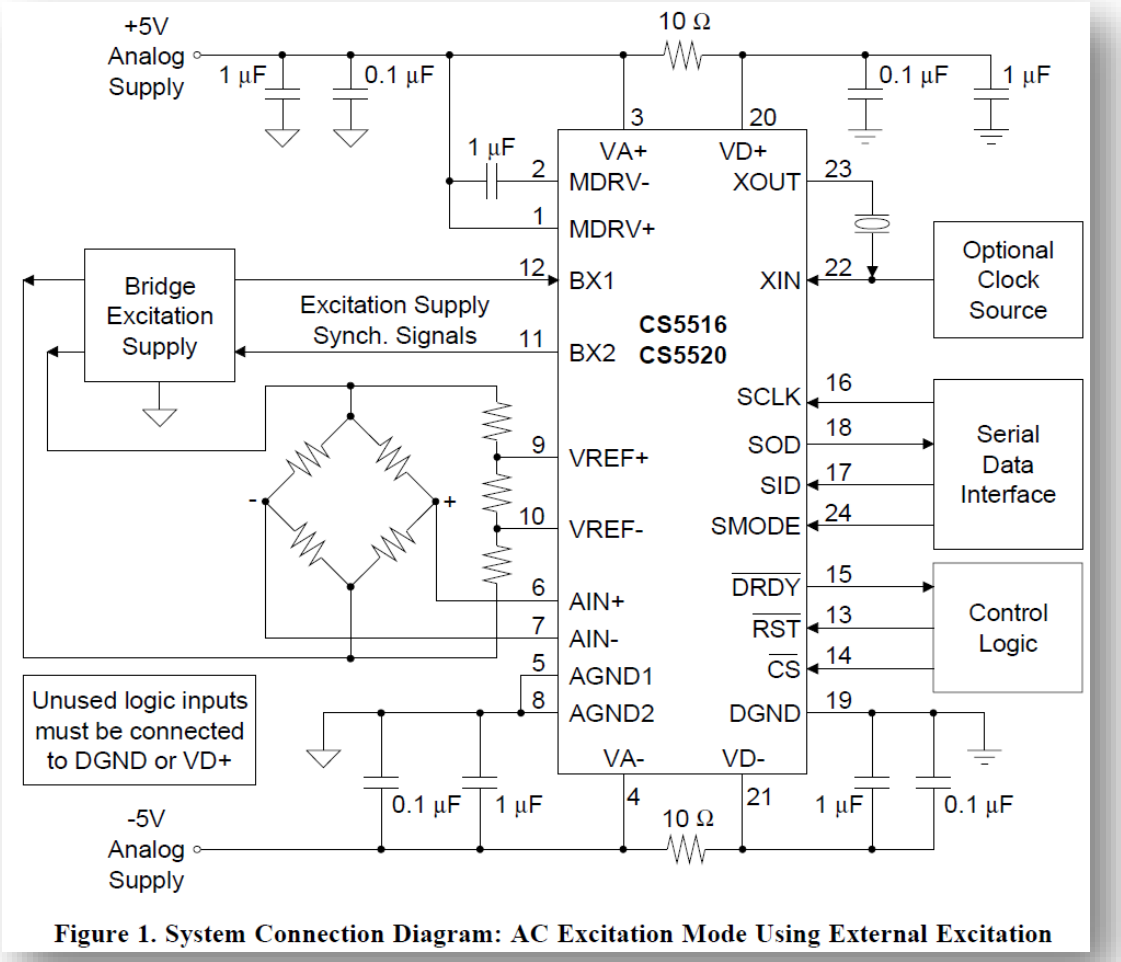


Figure 1. System Connection Diagram: AC Excitation Mode Using External Excitation

CIRRUS LOGIC

CS5516
CS5520

16-bit & 20-bit Bridge Transducer A/D Converters

Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error: ±0.0015% FS
  - 20-bit, No Missing Codes
- CMRR at 50/60 Hz > 200 dB
- System Calibration Capability with calibration read/write option
- 3-, 4-, or 5-wire Serial Communications Port
- Low Power Consumption: 40 mW
  - 10 µW Standby Mode for Portable applications

Description

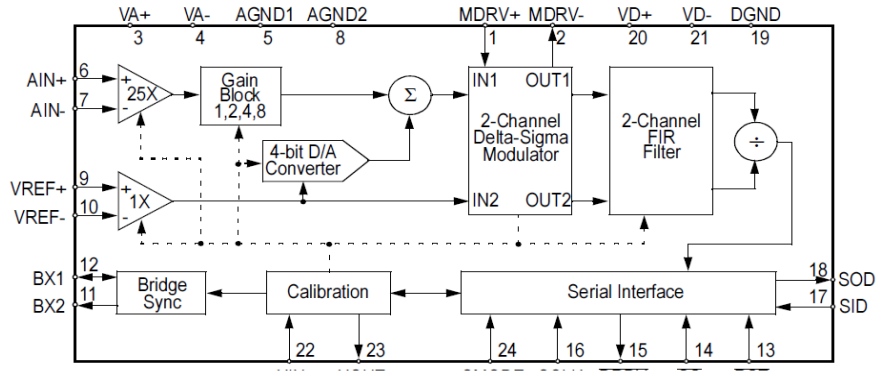
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60 Sps. The CS5520 achieves 20-bit resolution at output word rates up to 60 Sps.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12 Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

ORDERING INFORMATION
See page 29.



Conclusions

ADC should not be always the classic-way!!!

ΣΔ is a very brilliant example of

- Analog & Digital processing
- Resolution vs. speed trade-off

Next lesson: **none, just the exam!**