



POLITECNICO
MILANO 1863



ELECTRONIC SYSTEMS

2021-22 academic year
prof. Franco ZAPPA



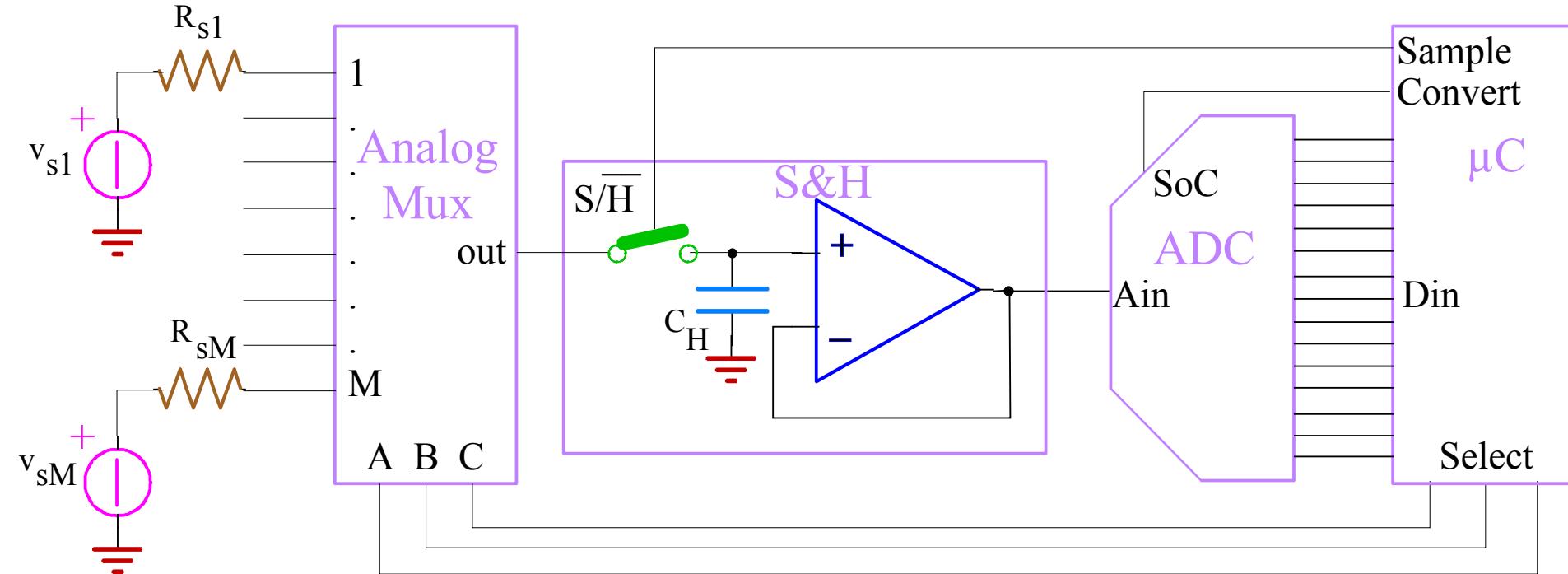
- Analog multiplexers
- ... again errors
- Digital potentiometers

they complete the acquisition front-end

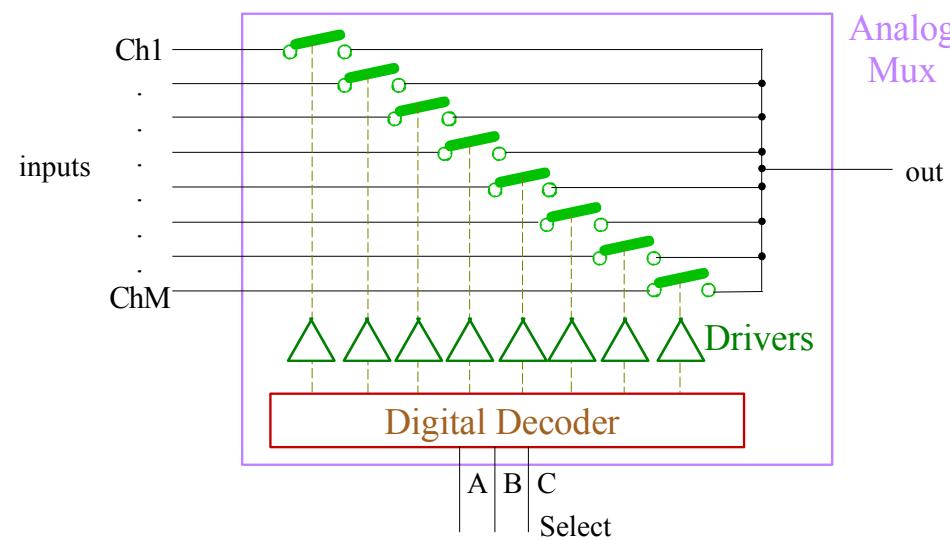


Analog Multiplexer

Example of application:



Internal architecture:

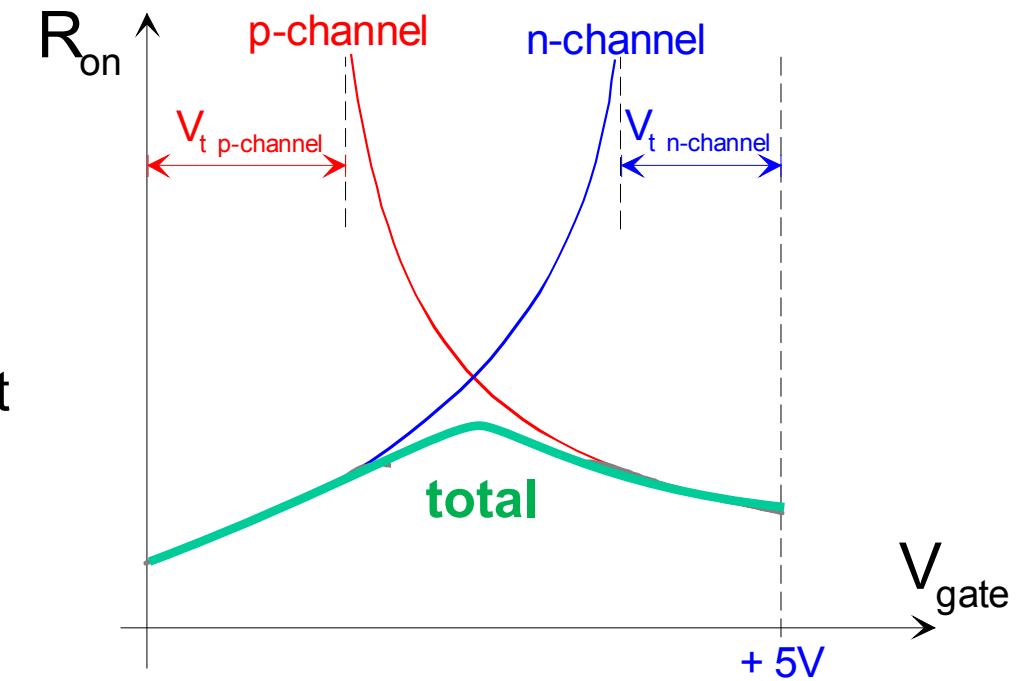
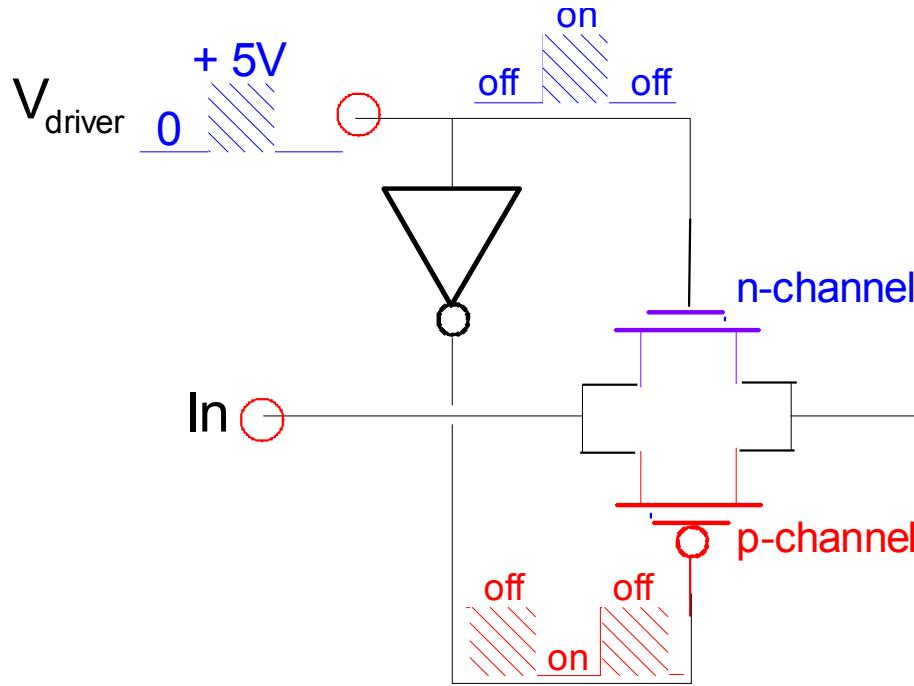




Analog Multiplexer

POLITECNICO
MILANO 1863

Analog switch implementation:



Also useful to compensate charge injection!



Datasheet

POLITECNICO
MILANO 1863

19-0396; Rev. 0; 5/95

MAXIM

Low-Voltage, 8-Channel/Dual 4-Channel Multiplexers with Latchable Inputs

MAX382/MAX384

1

General Description

The MAX382/MAX384 are low-voltage, CMOS, 1-of-8 and dual 4-channel muxes with latchable digital inputs. They feature low-voltage operation from a +2.7V to +16.5V single supply and from $\pm 3V$ to $\pm 8V$ dual supplies. Pin compatible with the DG428/DG429, these muxes offer low on-resistance (100Ω max) matched to within 4Ω max between channels. Additional features include off leakage less than $2.5nA$ at $+85^\circ C$ and guaranteed low charge injection ($10pC$ max). ESD protection is greater than 2000V per Method 3015.7.

Features

- ◆ Pin-Compatible with Industry-Standard DG428/DG429, DG528/DG529, MAX368/MAX369
- ◆ Single-Supply Operation (+2.7V to +16.5V)
Bipolar Supply Operation ($\pm 3V$ to $\pm 8V$)
- ◆ Low Power Consumption (<300 μW)
- ◆ Low On-Resistance, 100Ω max
- ◆ Guaranteed On-Resistance Match Between Channels, 4Ω max
- ◆ Low Leakage, $2.5nA$ at $+85^\circ C$
- ◆ TTL/CMOS-Logic Compatible

Applications

Battery-Operated Systems
Audio Signal Routing
Low-Voltage Data-Acquisition Systems
Sample-and-Hold Circuits
Automatic Test Equipment

Ordering Information

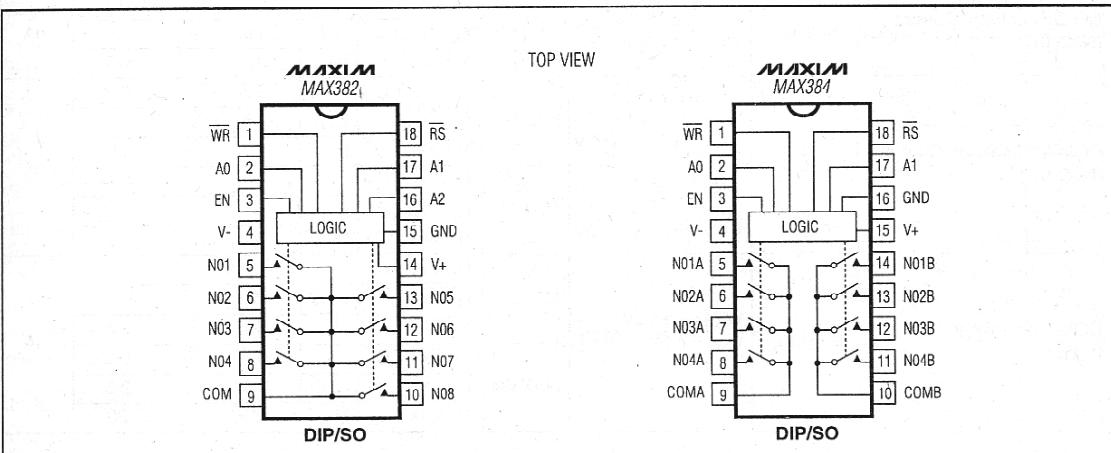
PART	TEMP. RANGE	PIN-PACKAGE
MAX382CPN	$0^\circ C$ to $+70^\circ C$	18 Plastic DIP
MAX382CWN	$0^\circ C$ to $+70^\circ C$	18 Wide SO
MAX382C/D	$0^\circ C$ to $+70^\circ C$	Dice*
MAX382EPN	$-40^\circ C$ to $+85^\circ C$	18 Plastic DIP
MAX382EWN	$-40^\circ C$ to $+85^\circ C$	18 Wide SO
MAX382EJN	$-40^\circ C$ to $+85^\circ C$	18 CERDIP**
MAX382MJN	$-55^\circ C$ to $+125^\circ C$	18 CERDIP**

Ordering Information continued on last page.

* Contact factory for dice specifications.

** Contact factory for package availability.

Pin Configurations





Analog Multiplexer's errors

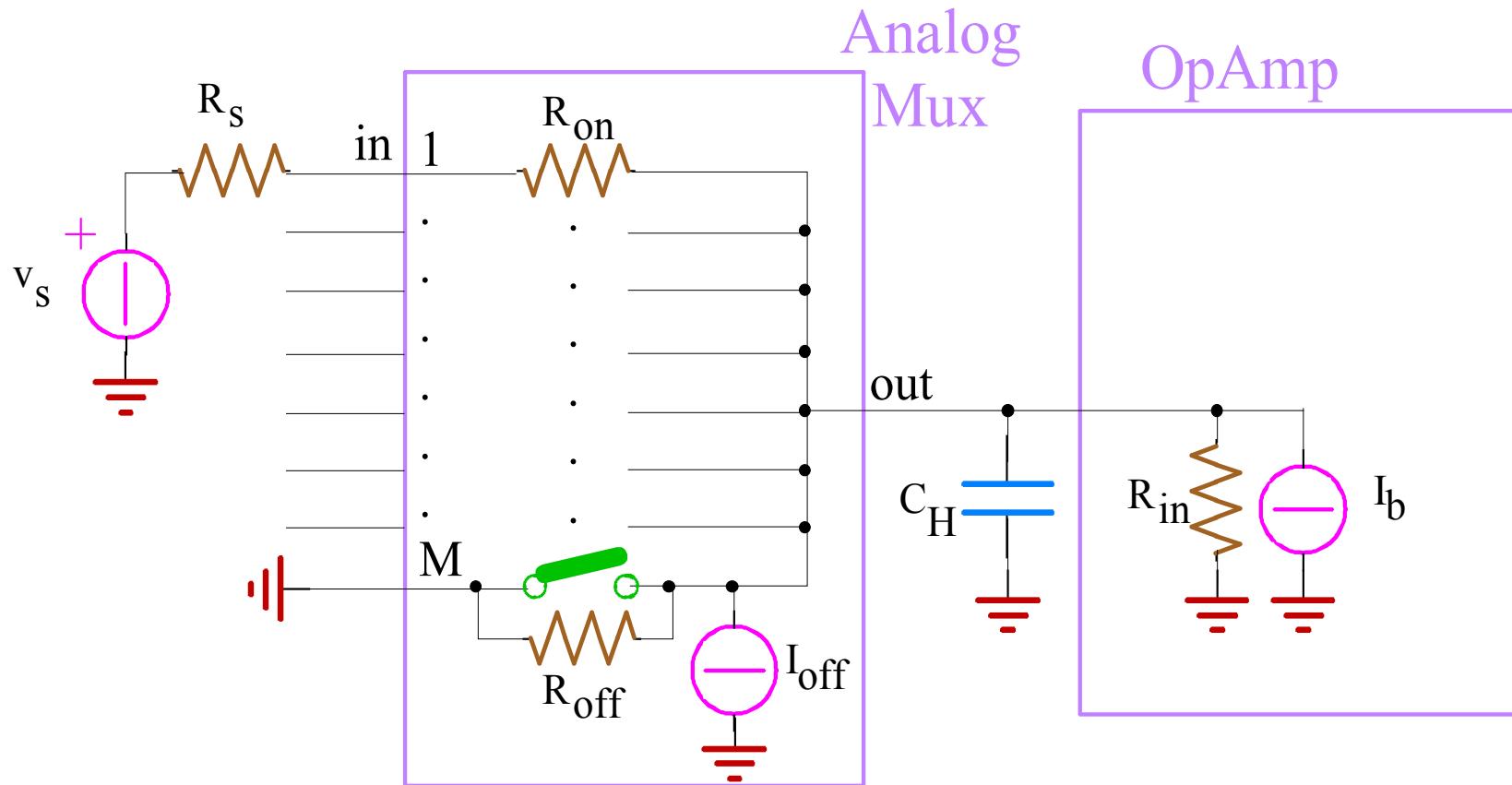
Sources of errors:

R_{on} $10\Omega \div 10k\Omega$

R_{off} $>10M\Omega$

I_{off} $<100nA$

T_{on} $T_{off} < 100ns$



$$\Delta V = \pm v_s \cdot \frac{R_s + R_{on}}{R_s + R_{on} + \left\{ R_{in} \parallel \left[\frac{R_{off}}{(M-1)} \right] \right\}} \pm (I_{off} \cdot (M+1) + I_B) \cdot \left\{ (R_s + R_{on}) \parallel R_{in} \parallel \left[\frac{R_{off}}{(M-1)} \right] \right\}$$



Example: ADG508A mux, Analog Devices

M=8 channels $R_{on}=400\Omega$ $R_{off}=10M\Omega$ $I_{off}=100nA$ (@ 125°C)

$v_s=\pm 15V$ $R_s=1k\Omega$

OpAmp $R_{in}=500k\Omega$ $I_b=0.5\mu A$

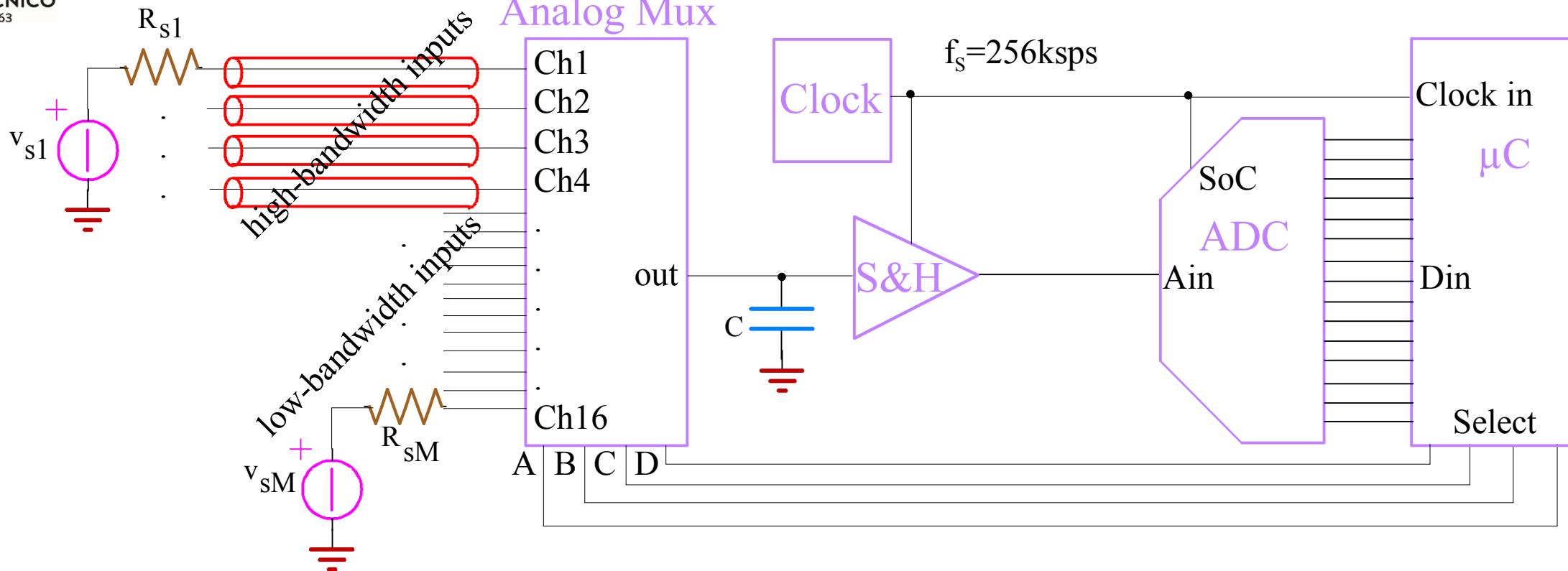
we get a maximum error of $\Delta V=\pm 56mV \pm 0.98mV \pm 0.7mV$

the first term is equal to $\frac{1}{2}LSB$ for a 10bit ADC

the sum of the other two contributions is equal to $\frac{1}{2}LSB$ for a 15bit ADC



Timings



Example:

ADC with $f_s = 256\text{ksps}$

every channel scanned at 16ksps ($1/f_s = 3.9\mu\text{s}$ and not $1/16\text{ksps}!$)

therefore the maximum admitted bandwidth of each channel is less than 8kHz

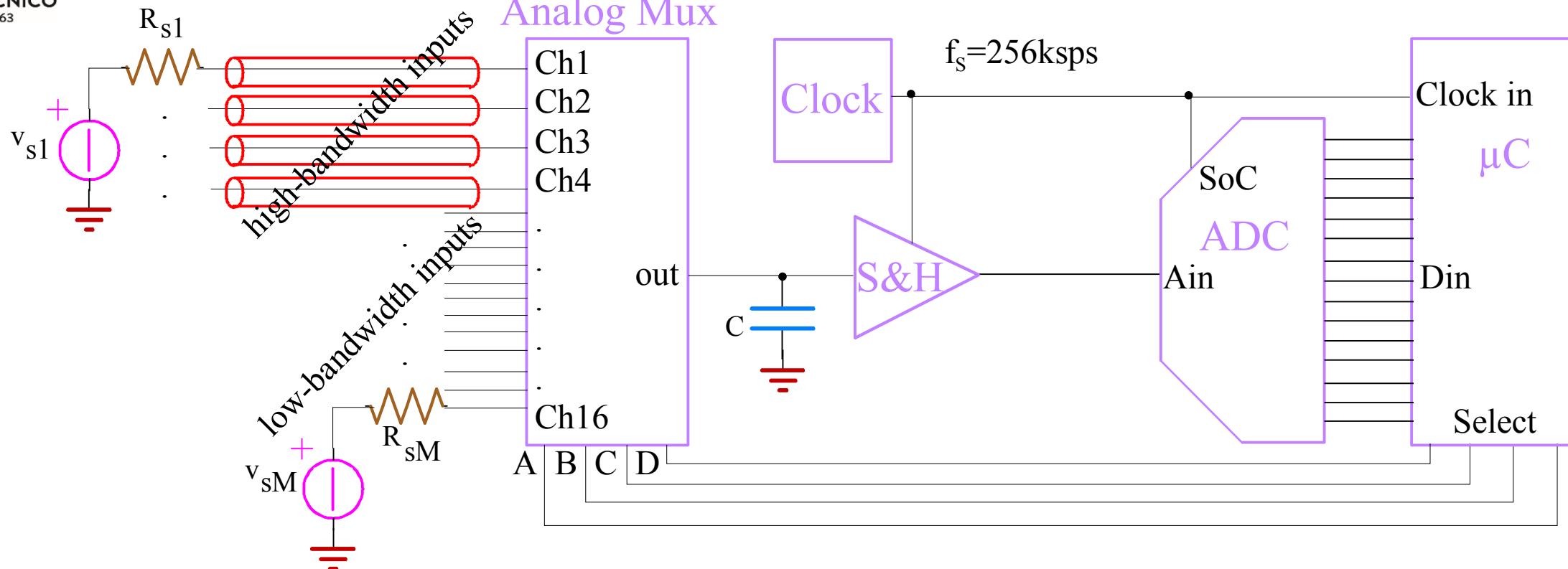
What about if $M=16$, but only the first four channels with a 20kHz bandwidth? Here is the solution:

Ch1, Ch2, Ch3, Ch4, Ch5, Ch1, Ch2, Ch3, Ch4, Ch6, Ch1, Ch2, Ch3, Ch4, Ch7...

for the first 4 channels, the sampling becomes $f_s/5 = 51.2\text{ksps}$, while the other 12 have $f_s/60 = 4.2\text{ksps}$



Timings



Example:

12bit ADC, requested accuracy better than $\frac{1}{2}\text{LSB}$

Acquisition time lower than:

$$\tau \leq \frac{T}{\ln \frac{FSR}{0.5 \cdot \text{LSB}}} = \frac{T}{\ln(2 \cdot 2^n)}$$

$$\tau < 3.9\mu\text{s}/9 = 434\text{ns}$$

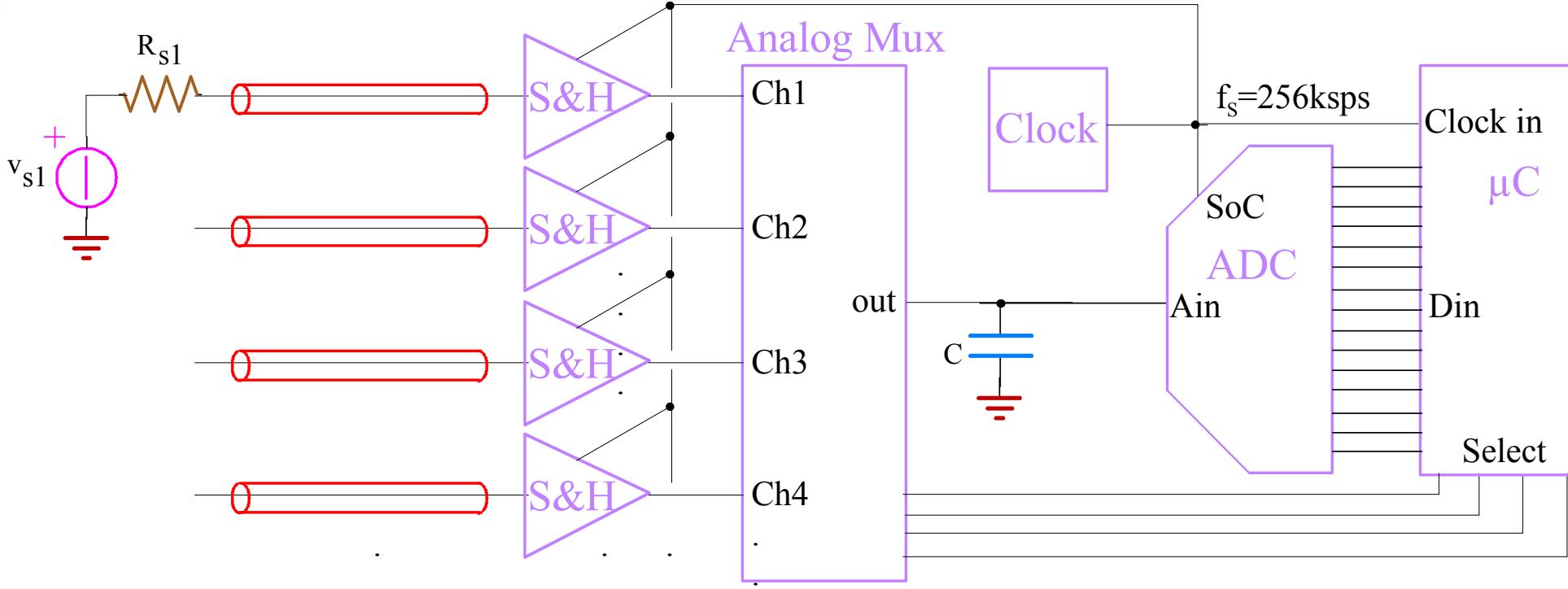
with $C_H=40\text{pF}$

we get

$$R_s + R_{on} < 11\text{k}\Omega$$



Synchronous coherent acquisition



Example:
ADC with $f_s=256\text{ksps}$
4 "fast" and 12 "slow" input channels

With just one S&H after the mux, each "fast" channel should have available a time of $5/f_s=19.5\mu\text{s}$

With one S&H at each channel input, each channel should have $16/f_s=62.5\mu\text{s}$



Data-sheet

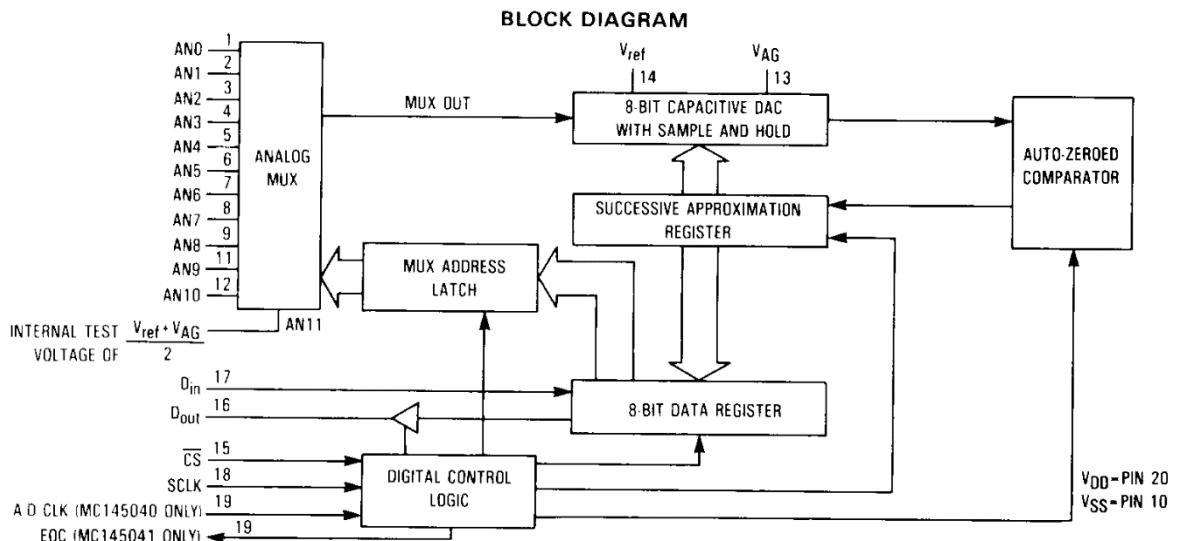
POLITECNICO
MILANO 1863

8-Bit A/D Converters With Serial Interface CMOS

The MC145040 and MC145041 are low-cost 8-bit A/D Converters with serial interface ports to provide communication with microprocessors and microcomputers. The converters operate from a single power supply with a maximum nonlinearity of $\pm \frac{1}{2}$ LSB with a 5 V reference and ± 1 LSB with a 2.5 V reference. No external trimming is required.

The MC145040 allows an external clock input (A/D CLK) to operate the dynamic A/D conversion sequence. The MC145041 has an internal clock and an end-of-conversion signal (EOC) is provided.

- Operating Supply Voltage Range: $V_{DD} = 4.5$ to 5.5 Volts
- Successive Approximation Conversion Time:
 - MC145040— $10\ \mu s$ (with 2 MHz A/D CLK)
 - MC145041— $20\ \mu s$ Maximum (Internal Clock)
- 11 Analog Input Channels with Internal Sample and Hold
- 0- to 5-Volt Analog Input Range with Single 5-Volt Supply
- Ratiometric Conversion
- Separate V_{ref} and V_{AG} Pins for Noise Immunity
- Monotonic Over Voltage and Temperature
- No External Trimming Required
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- TTL/NMOS-Compatible Inputs May Be Driven with CMOS
- Outputs are CMOS, NMOS, or TTL Compatible
- Very Low Reference Current Requirement
- Low Power Consumption: 11 mW
- Internal Test Mode for Self Test



**MC145040
MC145041**



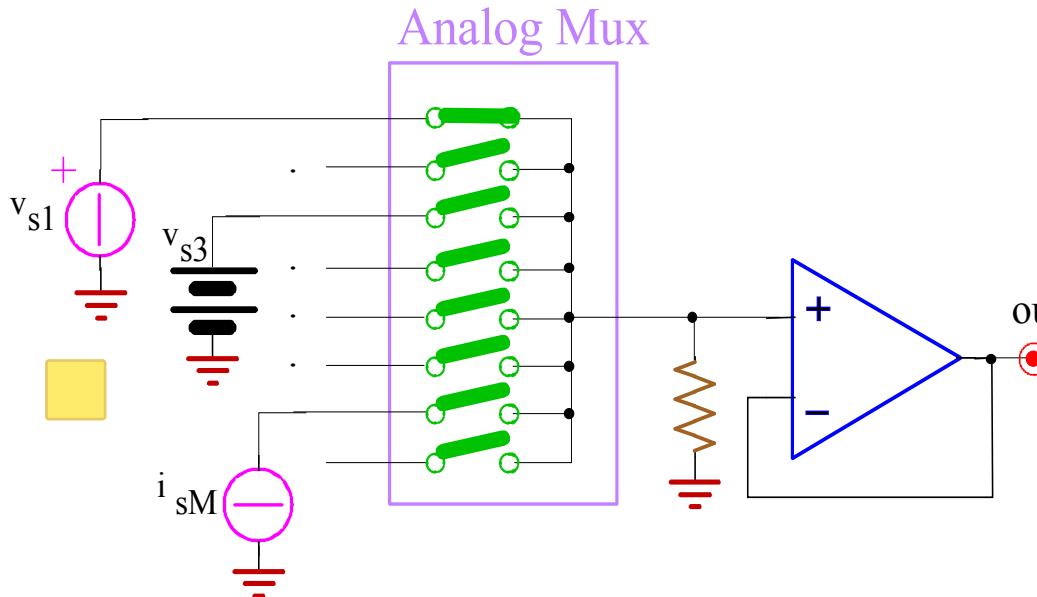
ORDERING INFORMATION

MC14XXXX	↓
Suffix	
1	-40 to 125°C
2	-40 to 85°C
P	Plastic DIP
DW	SOG
FN	PLCC

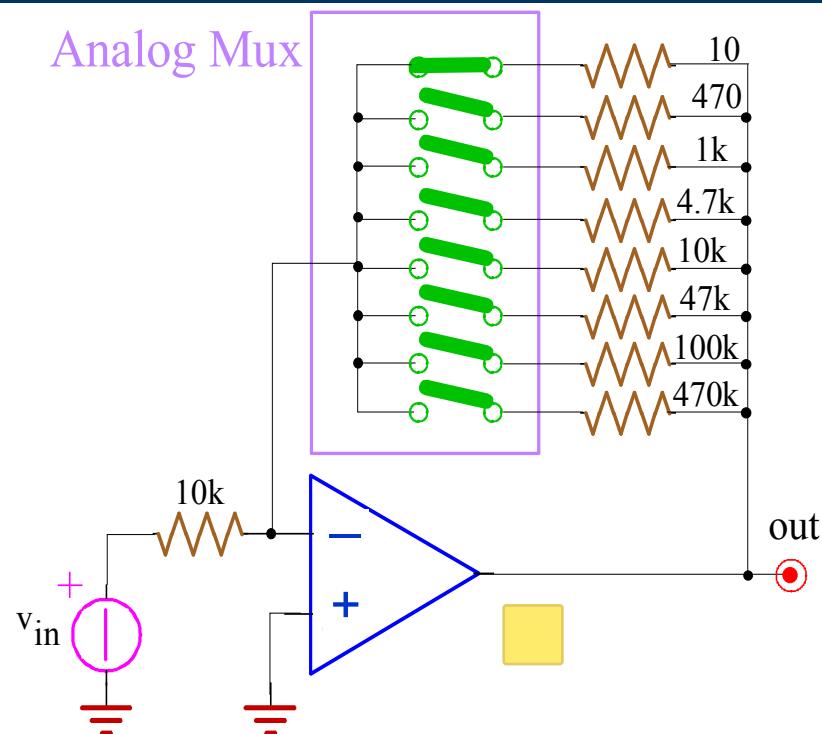


Improvements

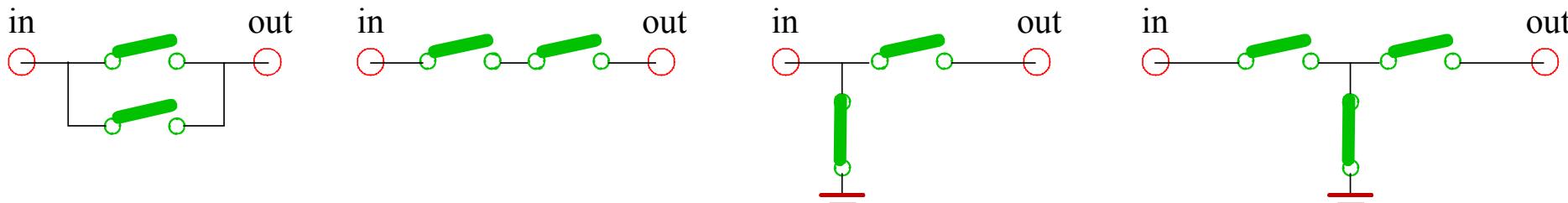
POLITECNICO
MILANO 1863



ALD4201 (**Break before Make**)



ALD4202 (**Make before Break**)



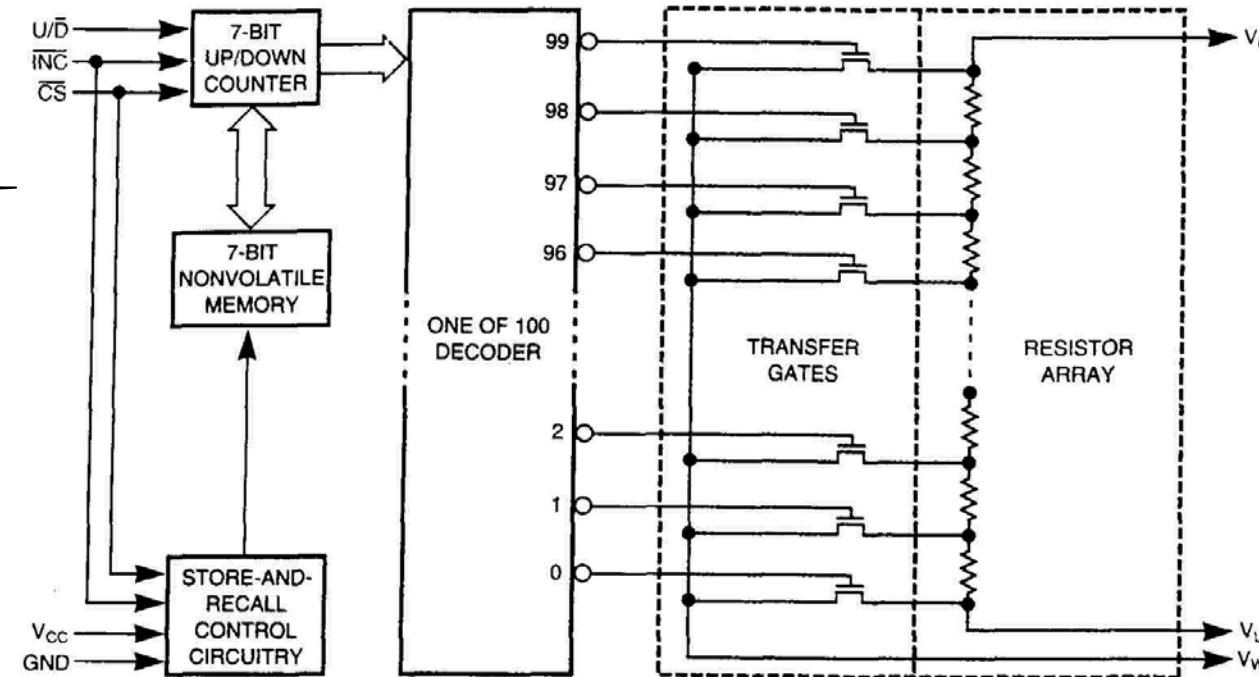


Digital potentiometers (DigPOT)

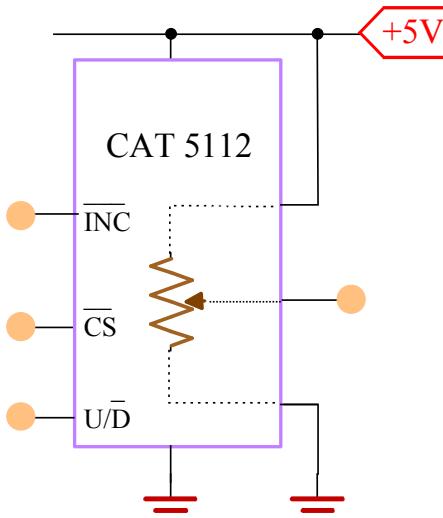
POLITECNICO
MILANO 1863

Block diagram:

Praticamente è un potenziometro digitale
comandato da un contatore



Example:

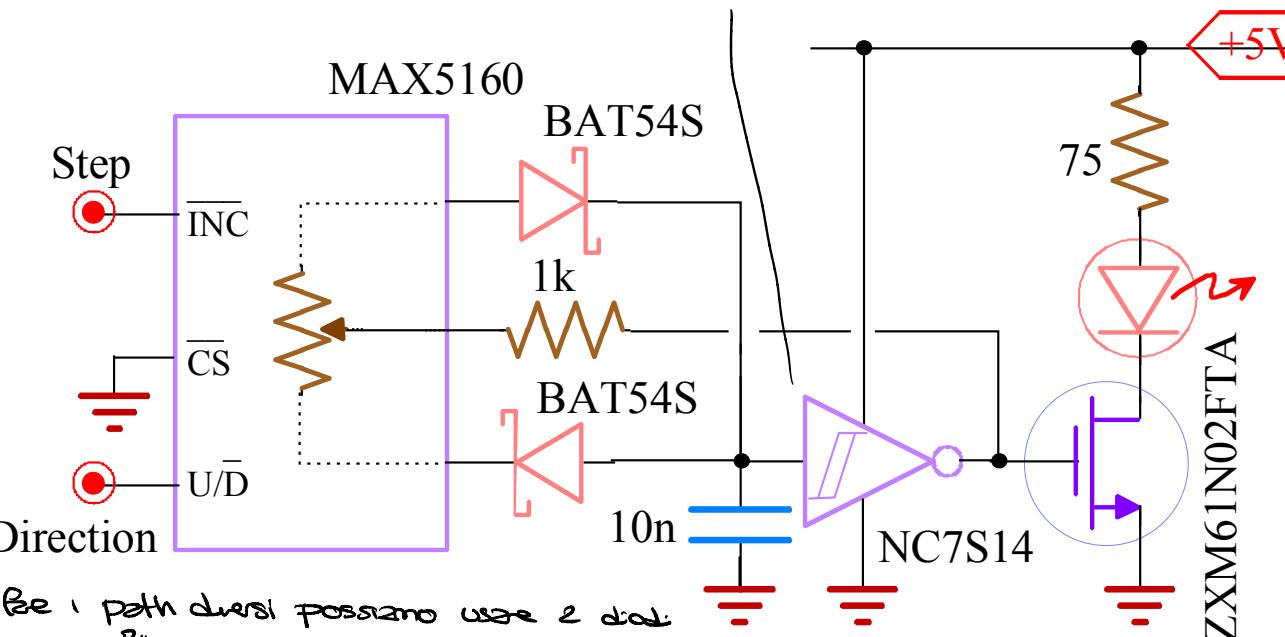


Model	Steps	Resistance (kΩ)	Configur- ation	Non- volatile	Packages	Interface	Operating power	Features	Price (1000)
AD8402	256	10, 50, 100	Dual	No	DIP-14, SO-14	Three-wire	2.7 to 5.5V, 5 μA	Full ac specs, nA shutdown current	\$1.66
AD8403	256	10, 50, 100	Quad	No	SOT-24	Three-wire	2.7 to 5.5V, 5 μA	Full ac specs, nA shutdown current	\$2.51
DS1267	256	10, 50, 100	Dual	No	DIP-14 SO-16, TSSOP-20	Three-wire	5 or ±5V, 650 μA	Stackable wipers for 512-step resolution	\$2.45
DS1867	256	10, 50, 100	Dual	Yes	DIP-14, SO-16, TSSOP-20	Three-wire	5 or ±5V, 650 μA	Nonvolatile ver- sion of DS1267	\$3.14
DS1802	64	50	Dual	No	DIP-20, SO-20, TSSOP-20	Three-wire and pushbutton	3 or 5V, 2 mA	Log taper, mute, audio specs	\$2.56



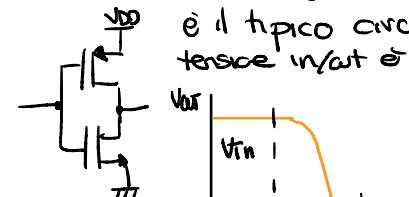
Digital potentiometers (DigPOT): examples of applications

POLITECNICO
MILANO 1863

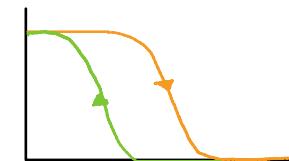


è un inverter con trigger d' Smith.

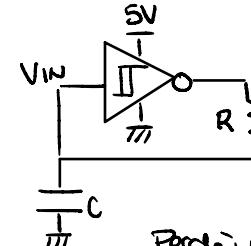
il mos può essere ON o OFF dipendentemente dalla tensione sul suo gate (che può essere 0, 5V o 5V)



Nel nostro caso però abbiamo che



Ci può servire un circuito così perché abbiamo rumore/debouncing. Questi inverter con trigger sono usati per creare degli oscillatori.



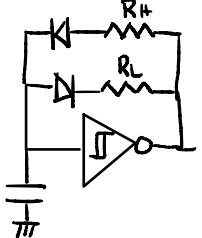
Perché noi aumentiamo la canca del veloce V_{THz} e diminuiamo fino a V_{TH1} . Con questa topologia c'è invece che $V_{TH} = V_{TH1}$ e $T = RC$ se volessimo T_H e T_L diversi dobbiamo usare 2 path diversi per canca e scanca.

Calcoliamo T_{av} e T_{off} . Sappiamo che non deve cambiare esponenti, perché a regime

$$T_H = T \cdot \ln\left(\frac{\Delta}{E}\right)$$

$$\text{dove } \Delta = 5V - V_{THz} \text{ e } E = 5V - V_{TH1}$$

Per fare i path diversi possiamo usare 2 diazi:



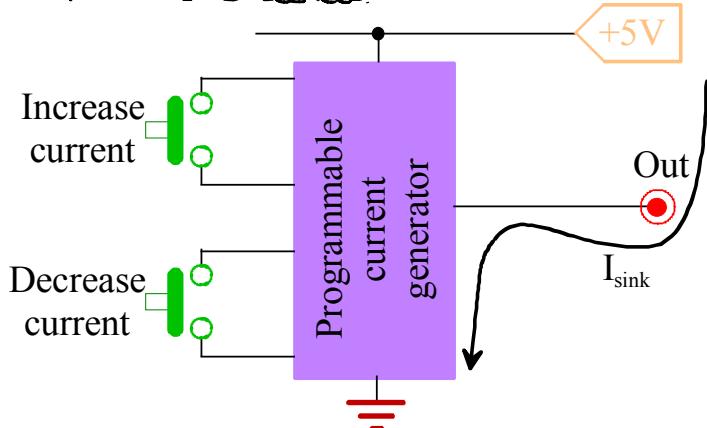
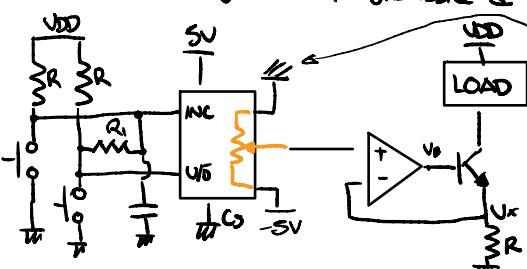
che è sostanzialmente quello fatto sopra solo che questo usa diazi: lui ha messo poi un potenziometro così posso cambiare T_H e T_L e il potenziometro è collegato così in modo che la frequenza sia la stessa. Sostanzialmente al posto di un potenziometro analogico ne usiamo uno digitale così top.

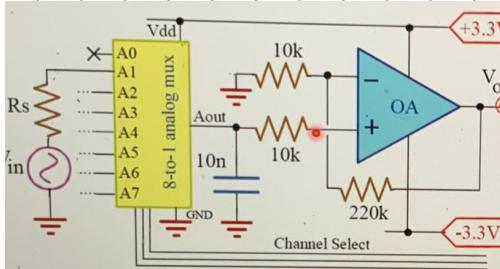
Per comandare il pot con 2 pulsanti posso fare

In pratica se premo D destra se cala V_{DD} down e poi con U salvo se salvo. Sembra la rete RC serie per fare un Delay così non debba tenere premuto D per stare in Down.

Se volessi fare un generatore programmabile di corrente posso fare una rete così con il POT.

Qui è collegato così perché il BJT in uscita da molte limitazioni. Se aussi messo +5V e GND allora la max V_A sarebbe stata tipo $V_B = 0.6$ ma ci sono piccole e quindi poco corrente in uscita anche.





Seven inputs with $R_s=100\Omega-1k\Omega$. OpAmp with sourcing $I_B=1nA$ and $V_{OS}=0.2mV$. Mux with $R_{on}=5-50\Omega$, $R_{off}=2M\Omega-20M\Omega$ and $I_{leak}=5nA$.

- Compute **sampling** and **hold** times for 12 bit resolution and $V_{in,max}=\pm 50mV$ and specify if they are max or min values.
- Compute all static errors and properly add them to compute the total output error in LSBs.

Abbiamo un MUX con un solo canale utilizzato. Il primo canale è usato per l'hold. L'output del MUX va al condensatore e poi va all'OPAMP.

So che il guadagno dell'OPAMP è $G = 1 + R_2/R_1$, perciò se V_{in} varia di $50mV$ allora l'uscita dell'OPAMP è $50mV \cdot G$

Per 12bit uno ADC ce ne ha un FSR di $5V$, allora il $LSB = \frac{5V}{2^{12-1}} = 2.4mV$ (11 è non 12 parziali in bit e di segno)
Allora abbiamo zero un errore $E < \frac{1}{2} LSB \leq 1.2mV$

1) Sampling time : $t_{sampling} \geq t_{acquisition} = T \ln \frac{\Delta}{E}$ dobbiamo considerare il caso peggiore cioè quando T e Δ sono massimi e E_{min} .

Perciò $t_{acq,min} = (R_{Smax} + R_{on,max}) C_H \cdot \ln \left(\frac{100mV}{\frac{1}{2} 2.4mV} \right) \simeq 75\mu s$

*Non ho capito perché MIN, ma è
contatto*

Questo perché $\Delta = 150mV \rightarrow 100mV$ e poi questo lo devo dividere all'uscita del mux quindi l'errore minimo da zero dopo l'opamp devo dividerlo per il guadagno.

Allora posso prendere un $t_{sampling} \simeq 100\mu s$.

2) Calcolare il tempo completo.

$$\frac{dV}{dt} = \frac{I_{leakage,tot}}{C_H} \quad \text{la Ileakage di quando siamo in Hold è data da}$$

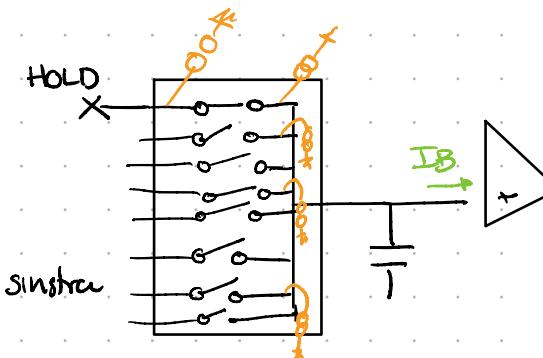
Abbiamo già già calcolato il canale del MUX al tempo massimo (8 dei bit + quello a sinistra di HOLD perché l'interruttore è chiuso) + I_B dell'OPAMP

$$\frac{dV}{dt} = \frac{95nA + 1nA}{C_H} \quad \text{(me lo sono perso)}$$

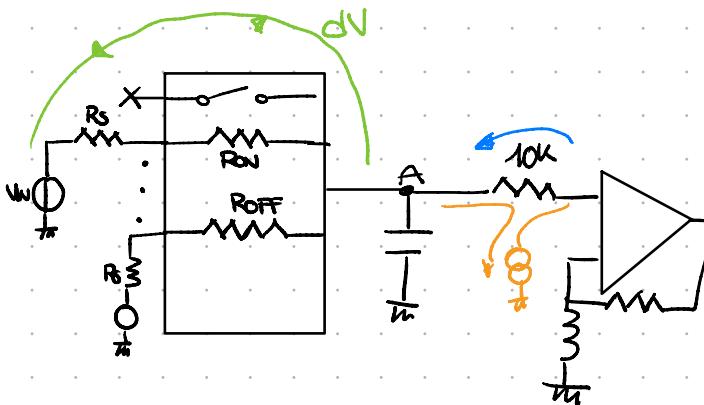
$$\text{Allora } t_{hold} \leq \frac{E}{\frac{dV/dt}_{\text{hold}}} = \frac{52\mu V}{4.6 \text{ V/s}} = 11.3 \mu s$$

e dunque per il guadagno

$$\text{Perciò } T_S = t_{sampling} + t_{hold} \simeq 90\mu s. \quad \text{Perciò } f_{Smax} \leq \frac{1}{90\mu s} = 11 \text{ Ksps} \quad \text{quindi } f_{max} \leq 5 \text{ kHz}$$



Calcoliamo gli errori della configurazione.



$$dV = V_{IN MAX} \cdot \frac{R_{S MAX} + R_{ON MAX}}{R_S + R_{ON} + \left(\frac{R_{OFF} + R_S}{6} \right)} = \pm 50mV \cdot \frac{1050}{105 + \frac{2M}{6}} \approx \pm 0.16mV$$

In più un altro errore dato da leakaggi di corrente di tutti i canali + quello dell'OPAMP

$$dV = \underbrace{(9 \cdot I_{leakage} + I_B)}_{max} \cdot \underbrace{(R_S + R_{ON}) / \left(\frac{R_{OFF} + R_S}{6} \right)}_{max} = \pm 66nA \cdot 1050 / 3M \approx 47nV$$

Resistenza vista al
nodo A

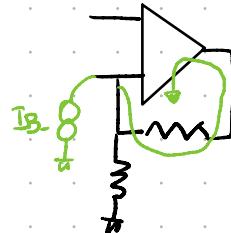
Allora per $dV = V_{OS} \cdot G = \pm 92mV \cdot 2.3 = \pm 4.6mV$ (calcolata all'output)

e anche $dV = I_B \cdot 10k\Omega = \pm 10\mu V \rightarrow$ è la ceduta data da I_B , sulla resistenza per uscire al nodo A.

E allora anche il gancio corrente del pin - parciò la leakaggi porta

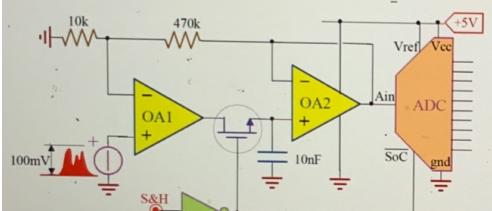
$$dV = I_B \cdot 220k = \pm 220\mu V$$

(calcolato all'output)

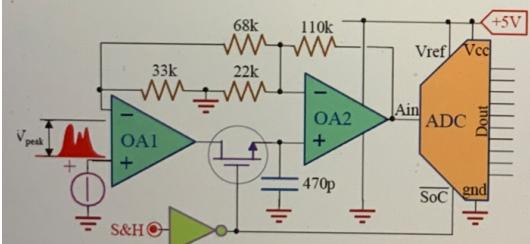


Perciò

$$\mathcal{E} = (\pm 0.16mV \pm 4.6\mu V \pm 10\mu V) \cdot G \approx \pm 4.6mV + 220\mu V \approx$$



OpAmps: $A_0=100\text{dB}$, $\text{GBWP}=100\text{MHz}$.
MOS: $R_{on}<100\Omega$, $V_T=0.8\text{V}$. ADC: 12bit.
a) Compute the acquisition time.
b) Compute static error on A_{in} in LSB, due to $I_B=5\text{nA}$ (sink) and $V_{os}=5\text{mV}$.



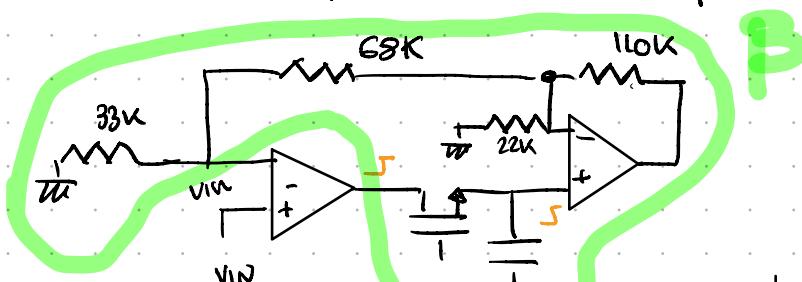
OpAmps: $A_0=100\text{dB}$, $\text{GBWP}=50\text{MHz}$.
ADC: 10bit, $T_{conv}=1\mu\text{s}$. MOSFET: $V_T=0.8\text{V}$, $R_{on}<80\Omega$, $C_{GS}=C_{GD}=C_{DS}<1\text{pF}$. CMOS NOT.
a) Compute the **ideal** gain of the S&H during Sampling and its **bandwidth**.
b) Compute the maximum allowable V_{peak} and the corresponding charge ignition.

Allora $I = \frac{V_{IN}}{33k}$ e quindi $V^* = I(33k + 68k)$

posso calcolare l'altra corrente $\hat{I} = \frac{V^*}{22k}$ perciò $I_{TOT} = I + \hat{I} = V_{IN} \left(\frac{1}{33k} + \frac{3}{22k} \right) = \frac{V_{IN}}{6000}$

Allora $V_{out} = V^* + \Delta V = V^* + \frac{V_{IN}}{6k} \cdot 110k \approx V_{IN} / (3 + 37) \approx V_{IN} \cdot 0.06$ perciò $G_{VD} \approx 60$

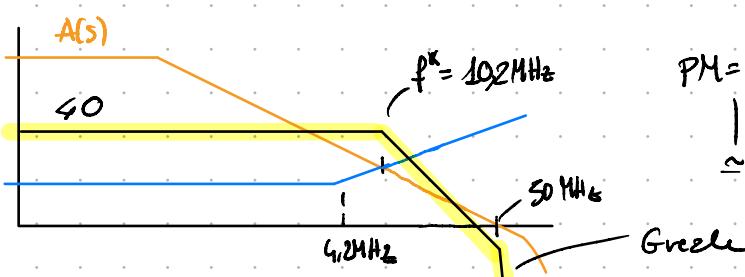
Studiamo il comportamento reale prendendo il circuito. Supponiamo il primo OPAMP come $A(s)$ e il resto $B(s)$



Se metto una tensione sul + ho lo stesso valore sul meno. Se suppongo il 2° opamp ideale

$$B(s) = \text{pole } 1 \cdot \frac{33k}{68k}$$

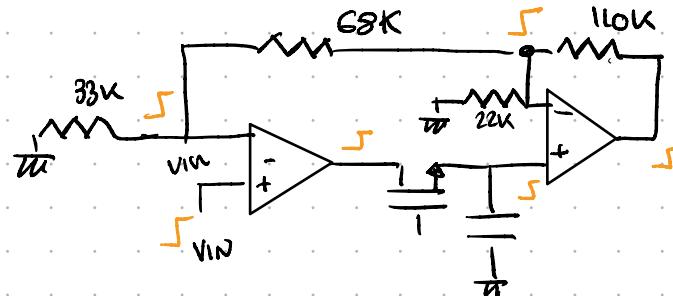
$$\text{pole} = \frac{1}{2\pi R_{ON} C_{in}} = 4.24 \text{Hz}$$



$$\text{PM} = 180^\circ - 90^\circ - \text{atan}\left(\frac{f^*}{4.24}\right) - \text{atan}\left(\frac{10.24}{50 \text{MHz}}\right) \approx 18^\circ$$

Il primo si parte considerando terra virtuale
allora il guadagno del S/H è $1 + R_2/R_1$
(ci ha detto di farlo da noi !!)

Facciamo l'esercizio 2.



ho quindi
una terra
virtuale



- What could we say... DO STUDY !

Next lesson: **12 - DAC**