Val Balaban

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SUMMARY for Machine Learning (ML) Engineer

- 7+ years of experience (industry + academia) building ML-training loops in Pytorch and C++.
- 2 ML papers – training strategies for improving both *robustness* and *fairness* of the trained model.
- Researched and developed ML and AI projects which placed second at Infineon's innovation conf.
- Founded *Race On*, an organization that taught 450+ students to code and race self-driving cars.

Keywords: *Pytorch, Tensorflow, scikit-learn, scikit-image, OpenCV, Python, Matlab, C++*

★ Highlights of ML experience

PhD in Electrical and Computer Engineering (Final Year) · University of Southern California *2016 – Present*

★ Devised ML training procedures for jointly optimizing individual and group fairness robust to changes in the data distribution – of paramount interest as sensitive groups are often underrepresented.[1]

★ Introduced *Distributional Variance Penalization* – an ML training strategy that improves generalization and robustness when the training data is limited and/or mislabeled.[2]

- Devised computer vision (CV) algorithms (OpenCV, C++) for detecting and tracking biological bodies. Investigated networking properties of neurons[3] and fractal self-organization properties of bacteria.[4]

★ Founded *Race On* – led a team of 11 PhD students who taught 450+ MS students how to code (CV and control) and race self-driving cars. The org. became financially independent within a year.

- Implemented an automated grading system (Python, GitHub) designed to provide transparency and granular feedback to combat learning limitations imposed by COVID, and evaluated assignments for 200+ grad students.
- Instructed (TAed) 1400+ undergrad and grad students for over 8 semesters teaching Embedded Systems, Network Programming, and Modern C++ (≥ 11) achieving an average student evaluation rating of 3.8/4.

Software and Hardware Engineer · Infineon Technologies *2014 – 2016*

★ Implemented an ML-based (SVM) automation strategy for simulation and lab experiments that reduced the validation time of integrated circuits (IC) from 120 hours to 8 hours (15-fold decrease).

★ Researched and built an AI-driven (PSO) power converter ($f_{switch} \leq 100kHz$) that compensates for load changes and component degradation, placed second at Inno Week (company's innovation conf).

- Devised system-level models (Matlab/Simulink) for validating the requirements of the next-gen IC modules.

Software and Hardware Engineer · D&D Technologies *2012 – 2014*

- Designed the electronics board (PCB), firmware (Embedded C), and server software (C++) for a distributed jackpot system currently deployed in casinos across 6 countries spanning 2 continents.
- Devised a secure network (CAN bus) that satisfies the real-time constraints (order of milliseconds) for coordinating the triggering moment of a distributed jackpot system across 128 slot machines.
- Created a custom Linux-based system (Yocto) optimized for minimum downtime and a reboot time < 2 seconds.

MS and BS in Electrical Engineering · University "Politehnica" of Bucharest, Romania *2009 – 2015*

[1] *Optimizing for Individual and Group Fairness using Variance Penalization.* Under Review
[2] *Improving Robustness: When and How to Minimize or Maximize the Loss Variance.* Presenting at ICMLA (2022)
[3] *Network science characteristics of brain-derived neuronal cultures deciphered from images.* Scientific Reports (2020)
[4] *Quantifying emergence and self-organisation of Enterobacter cloacae microbial communities.* Scientific Reports (2018)