```
1
2  --*************
3  -- Dylan Brown
4  -- ECE222 DP 2
5  -- Due 2/18
6  --*************
7
8  entity fulladd is
9    port(a, b, ci: IN  BIT;
10       s, co      : OUT BIT);
11 end fulladd;
12
13 architecture brown of fulladd is
14
15 begin
16   s<= a XOR b XOR ci;
17   co<= (a AND b) OR (a AND ci) or (b AND ci);
18 end brown;
```