```vhdl
1   --*************
2   -- Dylan Brown
3   -- ECE222 DP 2
4   -- Due 2/18
5   --*************
6
7   entity comb_mult4 is
8     port(m, q   : IN BIT_VECTOR(3 downto 0);
9          p      : OUT BIT_VECTOR(7 downto 0));
10  end comb_mult4;
11
12  architecture brown of comb_mult4 is
13
14    signal GND : BIT;
15    signal sig0, sig1, sig2, sig3, sig4, sig5, sig6, sig7, sig8, sig9, sig10, sig11, sig12, sig13, sig14, sig15 : BIT;
16    signal cout0, cout1, cout2, cout3, cout4, cout5, cout6, cout7, cout8, cout9, cout10, cout11, cout12, cout13, cout14, cout15 : BIT;
17    component fulladdmult is
18      port(a, x, y, ci: IN  BIT;
19           s, co      : OUT BIT);
20    end component;
21
22    begin
23      GND <= '0';
24      inst : fulladdmult port map(a=>'0', x=>m(0), y=>q(0), ci=>'0', s=>sig0, co=>cout0);
25      inst1 : fulladdmult port map(a=>'0', x=>m(1), y=>q(0), ci=>cout0, s=>sig1, co=>cout1);
26      inst2 : fulladdmult port map(a=>'0', x=>m(2), y=>q(0), ci=>cout1, s=>sig2, co=>cout2);
27      inst3 : fulladdmult port map(a=>'0', x=>m(3), y=>q(0), ci=>cout2, s=>sig3, co=>cout3);
28      inst4 : fulladdmult port map(a=>sig1, x=>m(0), y=>q(1), ci=>'0', s=>sig4, co=>cout4);
29      inst5 : fulladdmult port map(a=>sig2, x=>m(1), y=>q(1), ci=>cout4, s=>sig5, co=>cout5);
30      inst6 : fulladdmult port map(a=>sig3, x=>m(2), y=>q(1), ci=>cout5, s=>sig6, co=>cout6);
31      inst7 : fulladdmult port map(a=>cout3, x=>m(3), y=>q(1), ci=>cout6, s=>sig7, co=>cout7);
32      inst8 : fulladdmult port map(a=>sig5, x=>m(0), y=>q(2), ci=>'0', s=>sig8, co=>cout8);
33      inst9 : fulladdmult port map(a=>sig6, x=>m(1), y=>q(2), ci=>cout8, s=>sig9, co=>cout9);
34      inst10 : fulladdmult port map(a=>sig7, x=>m(2), y=>q(2), ci=>cout9, s=>sig10, co=>cout10);
35      inst11 : fulladdmult port map(a=>cout7, x=>m(3), y=>q(2), ci=>cout10, s=>sig11, co=>cout11);
36      inst12 : fulladdmult port map(a=>sig9, x=>m(0), y=>q(3), ci=>'0', s=>sig12, co=>cout12);
37      inst13 : fulladdmult port map(a=>sig10, x=>m(1), y=>q(3), ci=>cout12, s=>sig13, co=>cout13);
38      inst14 : fulladdmult port map(a=>sig11, x=>m(2), y=>q(3), ci=>cout13, s=>sig14, co=>cout14);
39      inst15 : fulladdmult port map(a=>cout11, x=>m(3), y=>q(3), ci=>cout14, s=>sig15, co=>cout15);
40      p(0)<=sig0;
41      p(1)<=sig4;
42      p(2)<=sig8;
43      p(3)<=sig12;
44      p(4)<=sig13;
45      p(5)<=sig14;
46      p(6)<=sig15;
47      p(7)<=cout15;
48  end brown;
```