Dylan Brown

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Khorbotly

ECE222

Design Project 2 Report

**Objective**

The objective of the design project was to learn how to write functional VHDL code. Moreover, this design project taught students how to use ModelSim, and only ModelSim, to simulate a design. Lastly, this project taught students both dataflow and structural VHDL.

**Procedure**

First, students had to launch ModelSim standalone. Then, students had to create a project in ModelSim. Then, students had to add a file named fulladd. Then, students had to write dataflow VHDL to implement a full-adder combinational circuit. Then, students had to compile, simulate, and verify their code. Next, students had to slightly modify their design in order to have one input be the ANDed output of two inputs X and Y. Then, students had to compile, simulate, and verify their code. Once students had this working, they had to create a new file named comb\_mult4. This file has an entity that use bit\_vector to take 2 inputs (of four bits) and an output (of eight bits). Students had to use their modified fulladd as a component. Students had to create instances of this component and implement a combinational multiplier. Lastly, students had to compile, simulate, and verify their design.

**Results**

I designed my paper sketch to use sixteen instances of fulladdmult. I connected the sum to the A of the next bit, and connected the multiplicand and multiplier to the X and Y inputs. My design is lined out in my paper sketch. When the design was written in VHDL, it simulated properly for all of the test cases. The work is shown on the waveform.

**Conclusion**

VHDL is a very powerful tool. VHDL allowed us to create a complex design in just under 50 lines. This project was beneficial in teaching us the language and showing us how to use ModelSim. This project overall was a massive success.