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ECE-222: Advanced Logic Design

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Design Project 4

**Objective**

The objective of this design project was to create a finite state machine for the controller of a Ford Thunderbird turn signal. The taillights work as described in the screenshot below. Moreover, this design project tested students on their ability to write FSMs in VHDL.



**Procedure**

First, students had to create a state diagram for their machine. Students were to use two inputs to indicate whether no action, left turn signal, right turn signal, or hazard lights were turned on. This would connect to a six-bit output of the whole taillight. After creating a state diagram, students had to then write a behavioral VHDL model. Then, students had to download the testbench file from blackboard. The testbench file had to be modified to fit your inputs/outputs. Students then had to run their simulation in ModelSim for 2000ns. Lastly, students had to verify their results.

**Results**

The design that I created for this project was successful. My state diagram and VHDL controller is attached to the back of this report. When simulated, the controller signaled the correct output for its respective input. This can also be seen on the last page of this report.

**Conclusion**

Overall, this project was really intuitive and it was a project that taught students how to properly write VHDL for FSMs. Moreover, this was a rea world application. Lastly, this project was a success, and I really learned a lot from it.