EE518 Analog IC-DESIGN LAB
Experiment 6

Design and analysis of a 2-stage op-amp

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September 2, 2024

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1 EXPERIMENTS

Design and analysis of a 2-stage op-amp

2 OBJECTIVE

- Design and analyze a 2-stage op-amp with the Design specification mentioned below.

3 Theory

The single stage op amp we can achieve the gain but it limits the output swing, By using the 2 stage opamp gin and the high swing can be achieved. in the 2 stage op amp the satge 1 will be the Differential amplifier and which provides the high gain and limits the swing, and the second stage is a common source stage that enhances the output swing. Let take the stage 1 differential amplifier with N-MOS input devices and P-MOS current source as a load. the outputs of the stage 1 differential amplifier circuit will be the inputs for the stage 2 common source

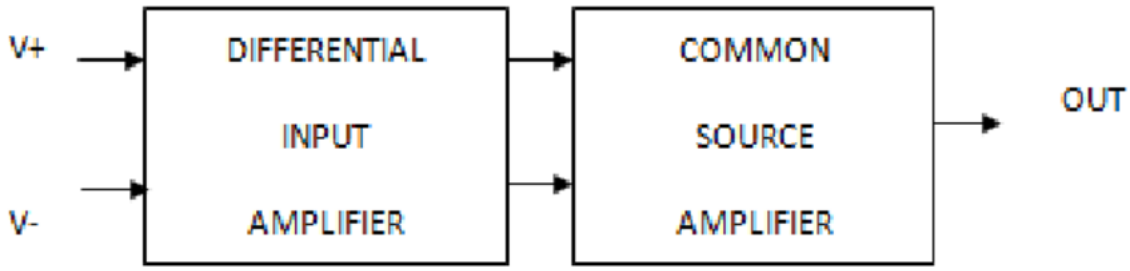

Figure 1: Block-diagram representation of two stage op-amp

3.1 Circuit

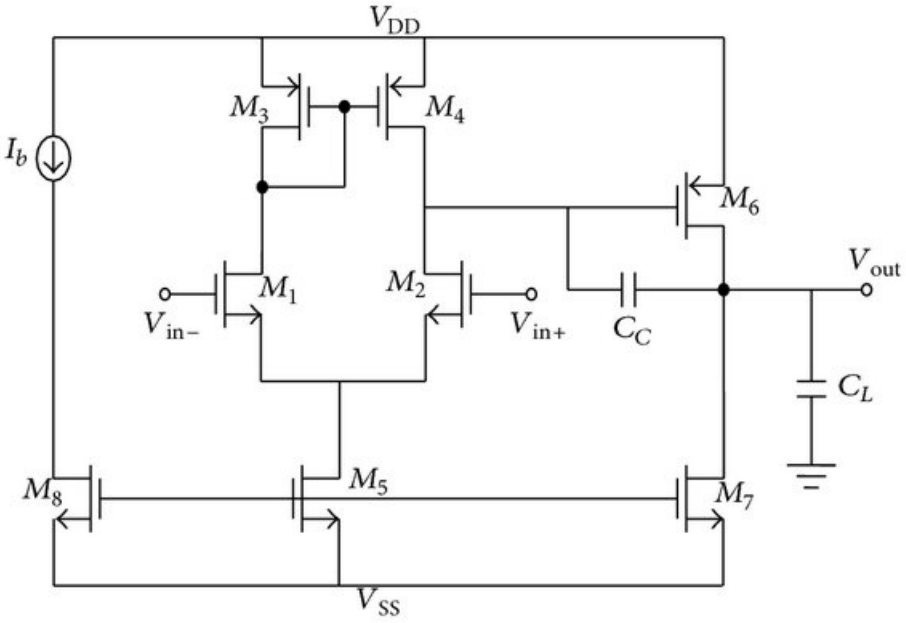

Figure 2: circuit of of two stage op-amp

3.2 Procedure

3.2.1 Step 1

If channel length modulation is considered, choose the smallest device length these will keep the channel length modulation (λ) constant

3.2.2 Step 2

Compensation capacitance Cc

- Cc (Miller compensation capacitance) connceted between gate and drain terminals of M6 transistor in the following circuit
- for a 60 degree phase margin, gain is almost flat, such that the Cc should choose as a minimum value to get the desired phase margin.
- For a 60 degree phase margin

$$Cc > 0.23CL \tag{1}$$

They given CL is 10 pF.so we got miller capacitance is

$$Cc > 2.3pF \tag{2}$$

3.3 step :3

Power calculations We have to design two stage OP AMP for low power they have given power should be less than or equal to 0.25milli watts and reference current current is 20µA.

3.3.1 Step 3

Finding Tail current Id5

- Since the given golden refernce current Iref is given as 40 uA, the current through M5 should be 40 uA
- Since based on slew rate requirement we will take the value for I5(tail current) Slew rate and tail current are dependent to each other

- Current flowing through the capacitor is

$$I = C.dv/dt \tag{3}$$

and the slew rate expression is

$$dv/dt = I/C(whichisthedefinationofSlewrate) \tag{4}$$

$$Id5 = Slewrate(SR) * Cc \tag{5}$$

Id5 is 40uA taken from the golden current source

$$Cc = 4PF \tag{6}$$

3.3.2 Step 4

Size of M3 PMOS transistor

- Current flowing through M1 and M3 transisitor are same,Since circuit is symmetric, current flowing from M1 and M3 are equal.
- Let M1 and M3 are in saturation
- Current flowing through M3 transistor is

$$Id3 = 1/2upCox(w/l)3(Vsg3 - |Vth3|)^2 \tag{7}$$

at saturation

- Since M3 is diode connected

$$Vsg3 = Vsd3 \tag{8}$$

The voltages at Vd3 and Vd1 are equal,

$$Id3 = 1/2upCox(w/l)3(Vs3 - Vg3 - |Vth3|)^2 \tag{9}$$

Voltage at source of M3 is Vdd and and vg3 = Vd3 =Vd1, such that

$$Id3 = 1/2upCox(w/l)3(Vdd3 - Vd1 - |Vth3|)^2 \tag{10}$$

- since M1 is in saturation

$$Vd1 = Vds1 = Vgs1 - vth1 \tag{11}$$

the above equation reprentsb the overdrive voltage of M1

- therefore Id3 will

$$Id3 = 1/2upCox(w/l)_3(Vdd3 - |Vth3| - (Vgs1 - Vth1))^2 \quad (12)$$

from the above equation (W/L)3 will be

$$(W/L)3 = 2 * Id3/upCox * (Vdd3 - |Vth3| - (Vgs1 - Vth1))^2 \quad (13)$$

- we know that Id3 =1/2 Id5

$$(W/L)3 = Id5/upCox * (Vdd3 - |Vth3| - (Vin(max) + Vth1))^2 \quad (14)$$

$(W/L)_3$ is determined using maximum ICMR (Vin (max)) Since Id5 =40 uA , by calculating these we will get

$$(W/L)_3 = 8$$

(15)

- M3 and M4 are forming a PMOS current mirror, so

$(W/L)_3 = (W/L)_4 = 8$ (16)

3.3.3 Step 5

Verify the poles and zeros

- Verify that poles and zeros due to C_{gs3} and C_{gs4} will not be dominant.
- Asuume that pole of M_3 is greater than 10 times od gain band width product, Such that
- Pole of M_3

$$PM_3 = gM_3/2C_{gs3} > 10 * GB \quad (17)$$

Where,

$$C_{gs3} = 2/3C_{ox}WL \quad (18)$$

and

$$gM_3 = 2Id/upC_{ox}(W/L)3(Vsg - |V_{th}|)^2 \quad (19)$$

3.3.4 Step 6

Size of M1 and M2 transistors

- M1 aand M2 are NMOS input transistors
- Select $(W/L)_1 = (W/L)_2$ to achieve desired GB

$$gM_1 = GBradiance * Cc \tag{20}$$

GB radiance GB (Hz) *2pi therefore

$$gM_1 = \sqrt{2unc_{\text{ox}}(W/L)Id_1}$$

(21)

- We know that Id1 = 1/2 Id5, Since it is a differential circuit so,

$$(W/L)_1 = {gM_1}^2/unC_{\text{ox}} * Id5 \tag{22}$$

- After calculating,

$$(W/L)_1 = 11 \tag{23}$$

- Since it is a Differential circuit the another half circuit will have the same current So,

$$(W/L)_1 = (W/L)_2 = 11 \tag{24}$$

3.3.5 Step 7

Size of M_5 transistor

- We will find the Size of M5 transistor by using the min ICMR equation

$$V_{\text{DS5(sat)}} = V_{\text{in(min)}} - V_{\text{ss}} - \sqrt{I_{\text{D5}}}/unC_{\text{ox}}(W/L)_1 - V_(th(max)) \tag{25}$$

- We know that I_{D5} = 40 uA, from the golden current source

- I_{D5} in saturation will be

$$I_{D5} = 1/2unC_{ox}(W/L)_5(V_{gs} - V_{th})^2 \tag{26}$$

- By using these current equation, We can find $(W/L)_5$

$$(W/L)_5 = 2I_{D5}/unCox(V_(DS5(sat)))^2 \tag{27}$$

- By Calculating, We will get the $(W/L)_5 = 11$
- Since M_5 and M_8 are a current mirror circuits

$$(W/L)_5 = (W/L)_8 = 11 \tag{28}$$

By these we will complete the 1 stage differential amplifier
Now,We will design the common source amplifier for stage 2

3.3.6 Step 8

Sizing of M_6 transistor

- For a resonable phase margin the following relation should be satisfied i.e.,

$$gM_6 = 2.2gM_4(C_L/C_(c)) \tag{29}$$

$$gM_6 >= 10gM_1 \tag{30}$$

- M_6 and M_4 have same voltages i.e.,

$$V_{sg6} = V_{sg4} \tag{31}$$

- Such that

$$(W/L)_6 = (W/L)_4(gm_6/gM_4) \tag{32}$$

- By calculating these we will get $(W/L)_6 = 144$

3.3.7 Step 9

Calculation for $I_{[}d6]$

- To find the sizing of M_7 we require Id_7, since I_{d7} =I_{d6}
- we can find the I_{D6} by using the obtained values of gm_6 and $(W/L)_6$.

$$gm6 = \sqrt{2upC_{ox}(W/L)_6}I_{D6} \tag{33}$$

– $I_{D6} = (gm_6)^2/2upC_{ox}(W/L)_6 By calculating, we will get I_{d6} = 360Id_6 = I_{D7}(34)$

3.3.8 Step 10

Sizing of M_7

- With the help of I_{D7} , we can calculate $(W/L)_7$

$$(W/L)7 = I_{D7}/I_{D5}(W/L)_5 \tag{35}$$

After calculating, we will get $(W/L)_7$ will be

$$(W/L)_7 = 99 \tag{36}$$

4 DC analysis

4.1 Schematic

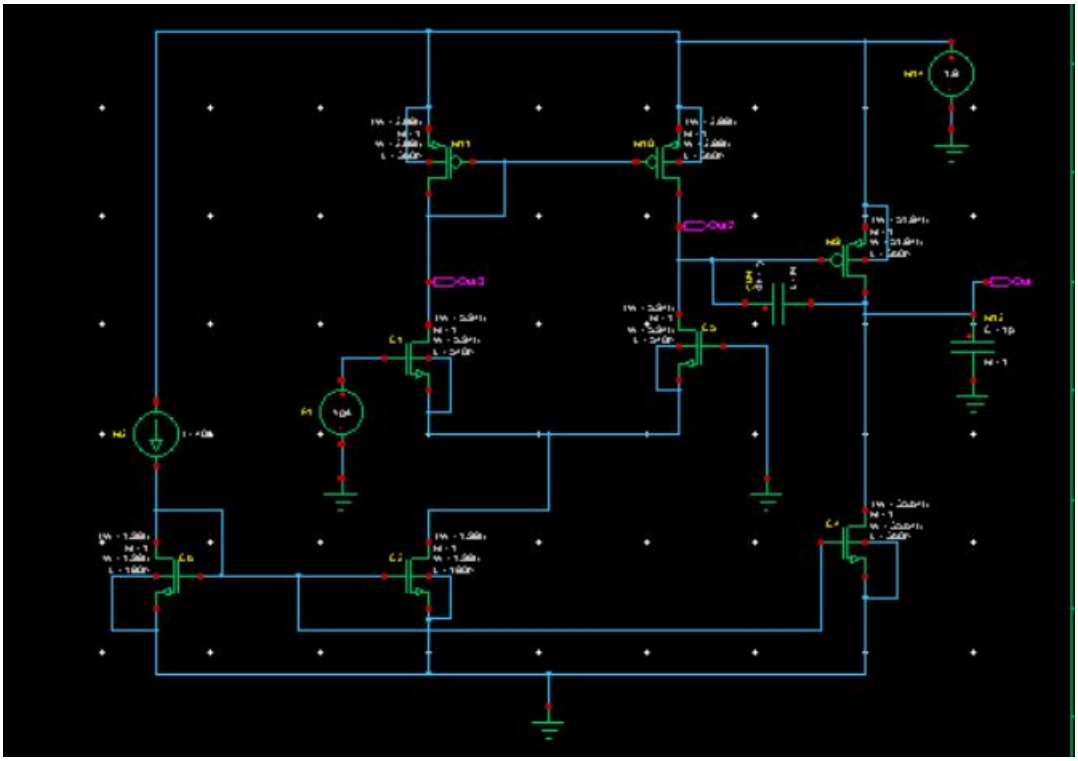

Figure 3: Block-diagram representation of two stage op-amp

4.2 Simulations and wave forms

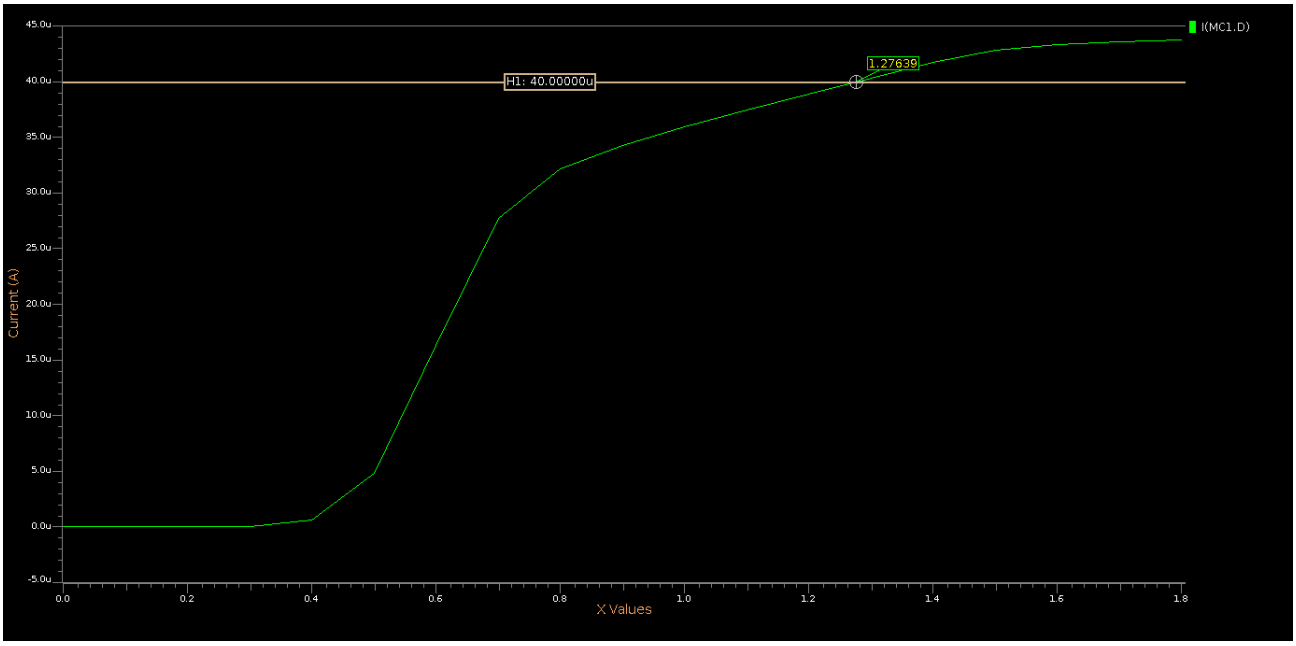

Figure 4: Block-diagram representation of two stage op-amp

5 AC analysis

5.1 Schematic

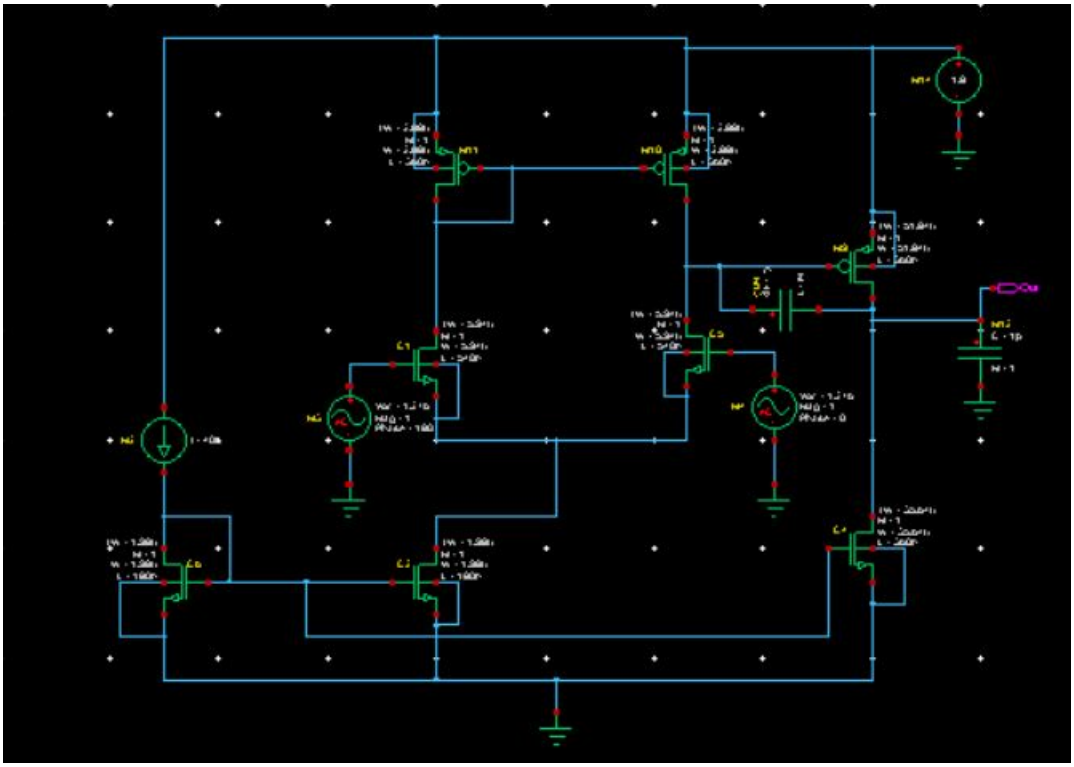

Figure 5: Block-diagram representation of two stage op-amp

5.2 Simulations and wave forms

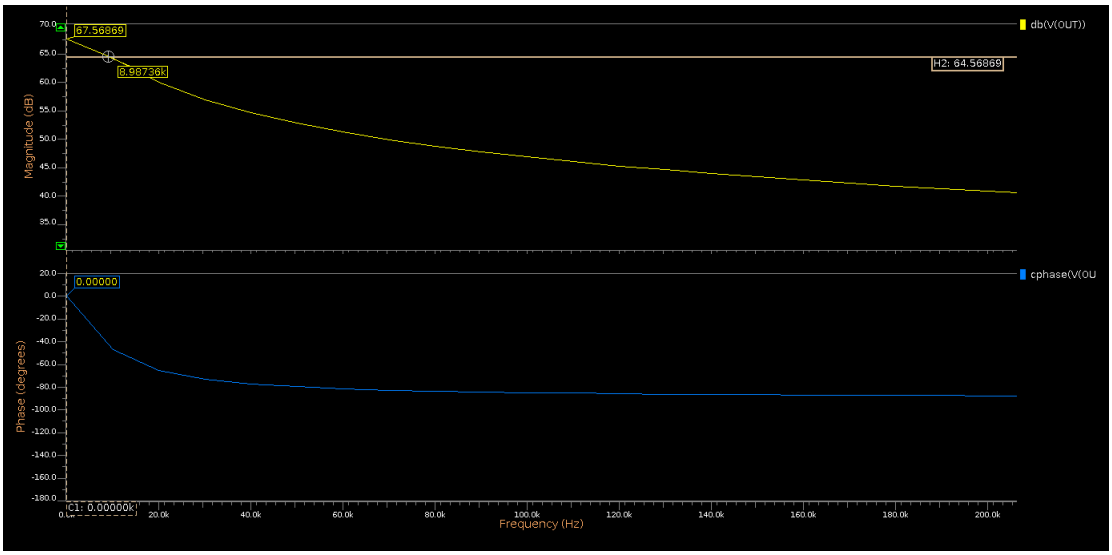

Figure 6: Block-diagram representation of two stage op-amp

6 Comparison tables

6.1 Design Specifications

Variable	Theoratical	Practical
gain	66.6 dB	67.8 dB
GBW	15 Mhz	19.12 Mhz

6.2 Capacitor Values

Capacitor	values (pF)
C_c	4
C_L	10

6.3 (W/L) ratios of all transistors

transistor	width(nm)	length(nm)
M1	5940	540
M2	5940	540
M3	2880	360
M4	2880	360
M5	1980	180
M6	360	5180
M7	360	5180
M8	1980	180

7 Conclusions:-

- All the results have been obtained practically and matching with the theoretical justification. The theoretical calculations have been done.
- Phase margin assumption and practical value that is 60 degrees satisfied.

- gain is high and good Gain bad width product got in 2 stage OP-AMP