EE518 Analog IC-DESIGN LAB
Experiment 7

Design and analysis of fully differential telescope OP - AMP circuits

Submitted by,
KOTAPATI VAMSHI KRISHNA
Roll No-234102412
Mtech in VLSI and Nanoelectronics
September 2, 2024

Contents

1 EXPERIMENTS

Analysis, and design of fully differential telescopic OP-AMP circuits.

2 OBJECTIVE

- To calculate parameters of the differential amplifiers for a specific gain such as length and width of each PMOS and NMOS used, transconductance and unity gain bandwidth.

2.1 Design Specification

- Target gain is ≥ 60
- The design should have a GBW $\geq$ 200 MHz.
- Power dissipation $\leq$ 10m W.
- Slew rate $\geq$ 50 V/ μ S

3 Theory

Voltage gain of 1 stage OP-AMP is very low, in order to increase the gain either R_0 or g_m should increase,Increasing gain by increasing R_0 will be achieved by using the cascoded structure in which R_0 is high

In the circuit, g_1=g_2=g_3=g_4=g_n and
g_5=g_6=g_7=g_8=g_p
Such that,
ro_1=ro_2=ro_3=ro_4=ro_n and ro_5=ro_6=ro_7=$r0_8$=g_p,
m3 and m4 are biased using Vb_1,
m5 and m6 are biased using Vb_2,
m7 and m8 are biased using Vb_3.
By half circuit concept, The gain of a telescopic OP-AMp is A_v = -$gm_n(gm_n ro_n^2 // gm_p ro_p^2)$

The drain resistor of the 2-mosfetsaa are also should be identical in such case the gain provided by both the amplifiers will be same and the 2 mosfets should be in saturation region,biasing is applied toboth the mosfets some common mode voltage(V_{cm}) input will be present at both inputs,Since mosfets are identical it will not effect the differential output

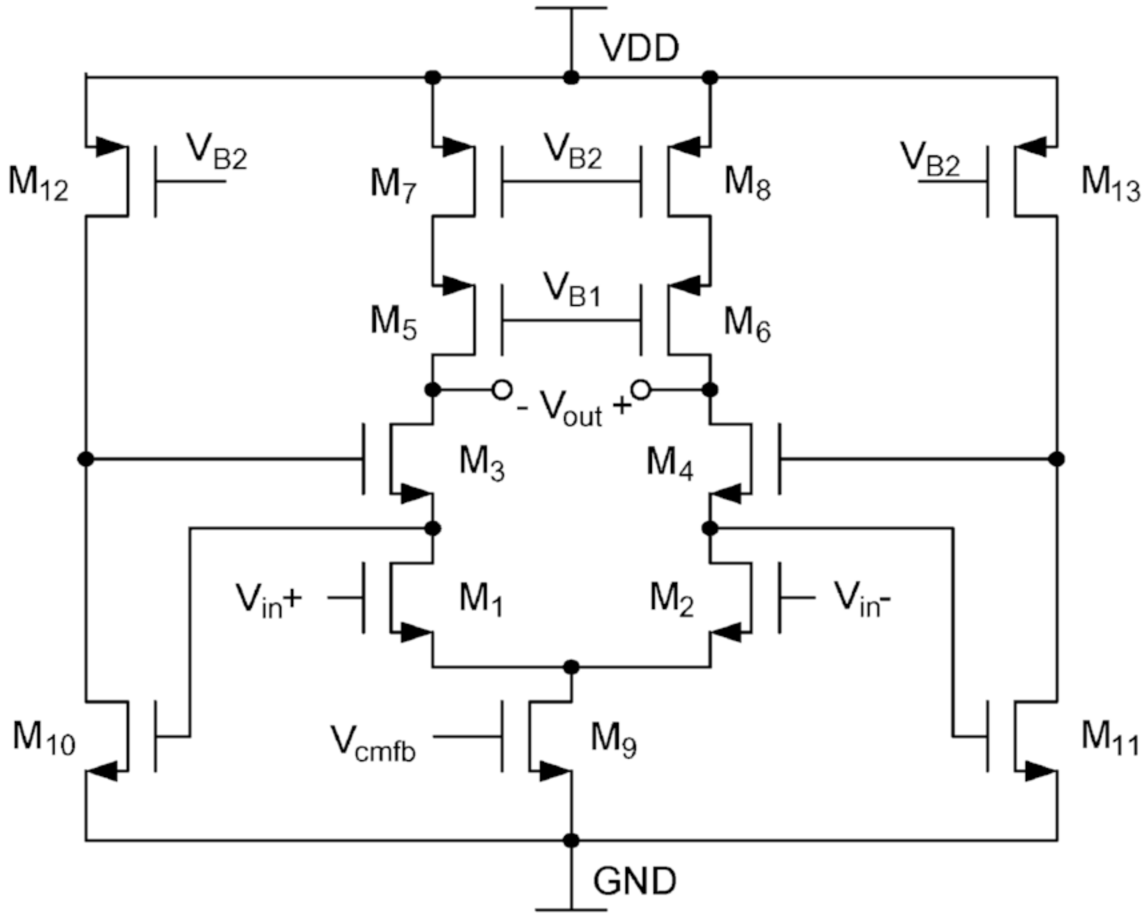

Figure 1: representation the schemmatic of Telescopic operational amplifier

But, when common mode input changes it also change sthe drain current of the mosfet and hence the trans conductance of both the mosfets changes and leads to change in the gain of the system.
If V_{cm} is very low it might turn of the transistor,So the bias currents (or) drain currents have minimum dependency on the V_{cm}.
these can be achieved by placing a current source in the circuit as shown in the fig, Iss is the current sourcenwhich makes the drain currents of the transistor independent of the common mode input levels

3.1 Parameter Definitions

3.2 Trans conductance ($\mathbf{g_m}$

Trans conductance indicates that how effectively a device signifies changes in input voltage to variations in output current.

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{1}$$

3.3 Threshold Voltage($\mathbf{V_{th}}$)

The gate-source voltage at which the mosfet attains inversion or it can be said that it is the gate-source voltage above or below which nmos or pmos is turned on. The transconductance curve is differentiated or drain current is double differentiated w.r.t gate-source voltage and the gate-source voltage at which the derivative is maximum gives us the threshold voltage.

$$V_{th} = V_{gs} \ at \ which \ \frac{d^2 I_D}{dV_{GS}^2} \ is \ maximum \tag{2}$$

3.4 Early Voltage($\mathbf{V_A}$)

In a MOSFET the channel length becomes smaller as a consequence of the drain space charge widening leading to smaller channel resistance and higher drain current. This effect is known as the Early effect in MOSFET. The voltage associated with this is early voltage.

$$V_A = \frac{1}{r_o I_{D_{sat}}} \tag{3}$$

3.5 Channel length modulation parameter($\boldsymbol{\lambda}$)

As (V_{DS}) increases beyond the overdrive voltage, the pinch-off point moves away from the drain end side and thus the effective channel length is reduced. However due to this, the current is not constant in the saturation region and starts to increase, and output resistance also reduces. This is called channel length modulation and the parameter representing the effect of reduced channel length is channel length modulation parameter.

$$\lambda = \frac{1}{V_A} \tag{4}$$

4 AC analysis

Ac analysis generally we did to find out small signal response of the circuit.we generally apply the AC and DC waves as the input ,here DC voltage is used for make the transistor in proper bias ,then we analyse the how AC input will get the gain .

4.1 AC parameters

4.1.1 voltage Gain $\mathbf{A_v}$:

Voltage gain is the one of the important parameter in AC analysis.It tells how much input amplifies by the circuit.generally we find out voltage gain by divide the small signal voltage output by the small signal voltage input.so maximum value of gain in the bode plot of gain treated as the voltage gain of the circuit.

$$A_v = \frac{v_{out}}{v_{in}} \tag{5}$$

4.1.2 Cut off frequency $\mathbf{f_c}$:

cut off frequency is up to which we have the half power .because to get proper gain we need at least half power. It is also called the 3db frequency ,because half power means we need to have the 70 percentage of Voltage .we are going to plot the gain versus frequency graph which is the bode plot. so it will be frequency at which gain will the 3db less than the maximum value of gain.

$$\text{cut off frequency} = \text{frequency}_{\text{at 3db less than maximum gain}}$$

4.2 Source Drain resistance $\mathbf{R_{ds}}$

r.It is used for analysis the gain of the circuit and also useful to design the current source.To find out the output resistance we can use the Channel length modulation parameter(λ) and Id at VGS-Vth.

$$Rds = \frac{V_A}{I_{ds}} \tag{6}$$

4.3 Output resistance R_o

To find out the output resistance of a circuit.we need to connect one test ac current souce at output and done the ac analysis find the output voltage .then fraction of test voltage to test current will be the output resistance.

$$Rout = \frac{V_{test}}{I_{test}} \tag{7}$$

4.4 Slew rate

Slew Rate Maximum Rate of change of output per micro second ,we treated as the slew rate.but in differential amplifiers we got maximum output when whole tail current is passing through one side

$$Slewrate = \frac{dV_{out}}{dt}_{max} \tag{8}$$

4.5 CMRR

CMRR means common mode rejection ratio It has the ability to maintain same output voltage by varying the supply voltage

$$CMRR = \frac{A_{diff}}{A_{comm}} = infinite|_{ideal} \tag{9}$$

4.6 PSRR

PSRR means power supply rejection ratio It defines how much common mode gain less with respect to the differential gain

$$PSRR = \frac{\delta V_{cc}}{\delta V_{out}} = infinite|_{ideal} \tag{10}$$

4.7 ICMR

ICMR means Input common mode Range,it is defined as range of common mode input we can applied to that circuit then all transistors in saturation.

5 Dividing the current by given power dissipation

Given the power disspiation is ¡= 10m W.Such that power dissipate through M9 and M10 should be less than or equal to 10m W

$$I_{\text{m9}} + I_{\text{m10}} * 1.8v <= 10mW$$

(11)

$$I_{\text{m9}} + I_{\text{m10}} <= 5.55mA \tag{12}$$

We will separete thee currents into

$$I_{\text{m9}} = 5mA \tag{13}$$

$$I_{\text{m10}} = 0.5mA \tag{14}$$

The given Slew rate is 50 V/ms
so

$$Slewrate = I_9/CL(15)$$

I_{M9}= 5mA,newline I_{M9}
C_{L} = 50u
C_{L} =100pF
We need to design the high swing.so we know high swing of differential amplifier(Telescope OP-AMP)

$$(V_{OD7} + V_{OD5} + V_{OD3} + V_{OD1} + V_{OD9}) = 0.9 \tag{16}$$

$$2(v_{DD} - (V_{OD7} + V_{OD5} + V_{OD3} + V_{OD1} + V_{OD9})) = 1.8 \tag{17}$$

5.1 Assigning of Over drive voltages to the transistors

As M9 holds more current we going to assign more over drive voltage as 0.3v.

$$V_{0D9} = 0.3 \tag{18}$$

For the other remaining voltages of PMOS and NMOS ,
we know PMOS have less mobility than NMOSbut holding same current as

the NMOS
So,

$$V_{0D7} = 0.2, V_{0D5} = 0.2 \tag{19}$$

we know NMOS have more mobility than PMOS but holding same current as the PMOS

$$V_{0D3} = 0.1, V_{0D1} = 0.1 \tag{20}$$

By using the over drive voltages we will find the aspect ratios of all transistors

5.1.1 Aspect ratio of M9

$$5 * 10^{-3} = 0.5 * 324.18 * 10^{-6} * \frac{W}{L} * 0.3^2 \tag{21}$$

$$\frac{W}{L}_{M9} = 324.71 \tag{22}$$

5.1.2 Aspect ratio of M10

,

$$0.5 * 10^{-3} = 0.5 * 324.18 * 10^{-6} * \frac{W}{L} * 0.3^2 \tag{23}$$

$$\frac{W}{L}_{Mb1} = 32.471 \tag{24}$$

Since all NMOS transistors are identical

$$\frac{W}{L}M1 = \frac{W}{L}M2 = \frac{W}{L}M3 = \frac{W}{L}M4 \tag{25}$$

By using the current equation,

$$2.5 * 10^{-4} = 0.5 * 324.18 * 10^{-6} * \frac{W}{L} * 0.1^2 \tag{26}$$

by solving above equation ,we got

$$\frac{W}{L}M1 = \frac{W}{L}M2 = \frac{W}{L}M3 = \frac{W}{L}M4 = 1461.219 \tag{27}$$

similarly all PMOS transistors are identical .

$$\frac{W}{L}M5 = \frac{W}{L}M6 = \frac{W}{L}M7 = \frac{W}{L}M8 \tag{28}$$

By using the current equation,

$$2.5 * 10^{-4} = 0.5 * 137.18 * 10^{-6} * \frac{W}{L} * 0.2^2 \tag{29}$$

by solving above equation ,we got

$$\frac{W}{L}M5 = \frac{W}{L}M6 = \frac{W}{L}M7 = \frac{W}{L}M8 = 911.2115 \tag{30}$$

so we got the all aspect ratios .so now we are going to find out the dc values of all the mosfets.

5.2 To find the DC voltage at gate

M1 and M2:

we now source voltage of M1 ,is nothing but drain voltage of M9 .which is 0.3.and we know overdrive voltage of 0.1.

V$_{0D1} = 0.1$
$V_{Gs1} - V_{th1} = 0.1$
$V_{G1} - V_{S1} - V_{th1} = 0.1$
$V_{G1} - 0.3 - 0.55 = 0.1$
$V_{G1} = V_{G2} = 0.95$

M3 and M4:

we now source voltage of M3 ,is nothing but drain voltage of M1 which is 0.4 and we know overdrive voltage for NMOS i.e., $\mathrm{V}_{0D3} = 0.1$

$V_{Gs3} - V_{th3} = 0.1$
$V_{G3} - V_{S3} - V_{th3} = 0.1$
$V_{G1} - 0.4 - 0.55 = 0.1$
$V_{G1} = V_{G2} = 1.05$

M7 and M8

we now source voltage of M7 ,is nothing but Vdd. and we know overdrive voltage for PMOS i.e., 0.2.

$\mathrm{V}_{0D7} = 0.2$
$V_{SG7} - V_{th7} = 0.2$
$V_{S7} - V_{G7} - V_{th7} = 0.2$
$1.8 - V_{G7} - 0.55 = 0.1$
$V_{G7} = V_{G8} = 1.05$

M5 and M6

we now source voltage of M5 ,source voltage of M5 nothing but drain voltage of M7 which is 1.6. and we know overdrive voltage of 0.2.

$\mathrm{V}_{OD5} = 0.2$
$V_{SG5} - V_{th5} = 0.2$
$V_{S5} - V_{G5} - V_{th5} = 0.2$
$1.6 - V_{G7} - 0.55 = 0.2$
$V_{G5} = V_{G6} = 0.85$

we obtain all the dc voltage at gate .

5.3 Measure gm and rds

so if you take minimum length of mosfet 180nm ,then early voltage is 0.9.such that r_{ds}, will be

$$r_{ds} = \frac{V_A}{I_D}$$
$$r_{ds} = 360$$

trans conductance of NMOS will be

$$gm_N = \frac{2I_D}{V_{gs} - V_{th}} \tag{31}$$

$$gm_N = \frac{2 * 2.5 * 10^{-3}}{0.1}$$
$$gm_N = 50m\mho$$

and trans conductance of PMOS will be

$$gm_P = \frac{2 * 2.5 * 10^{-3}}{0.2}$$
$$gm_P = 25m\mho$$

Gain obtained,

$$A_V = 108 \tag{32}$$

to increase the gain ,we are going to increase the $\mathrm{r_{ds}}$ .so we increase the length to 720nm
early voltage will be 3.6
rds will be 1440.

$$A_V = 1325 \tag{33}$$

5.3.1 Finding CL

Given GBW is 200 mega hz. Such that,

$$GBW = \frac{gm}{2 * \pi * C_L} = 200 * 10^6 \tag{34}$$

$$C_L < 30.1pF \tag{35}$$

5.4 Advantages of Differential Amplifier

- These circuit increases gain
- voltage swing is not improvised

6 Simulations and waveforms

6.1 DC analysis

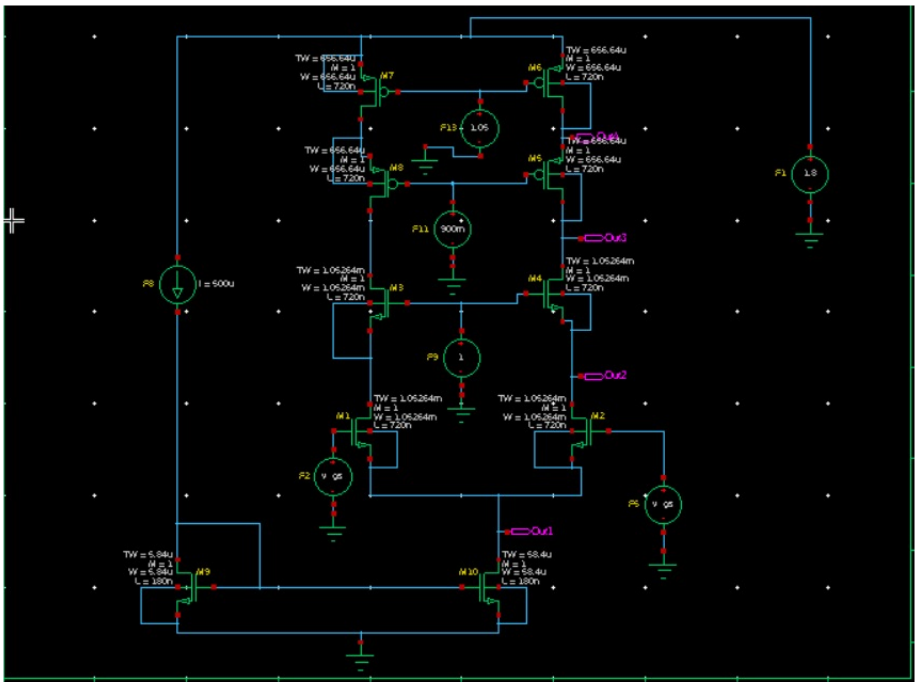

Figure 2: circuit diagram for DC analysis of Telescope amplifier

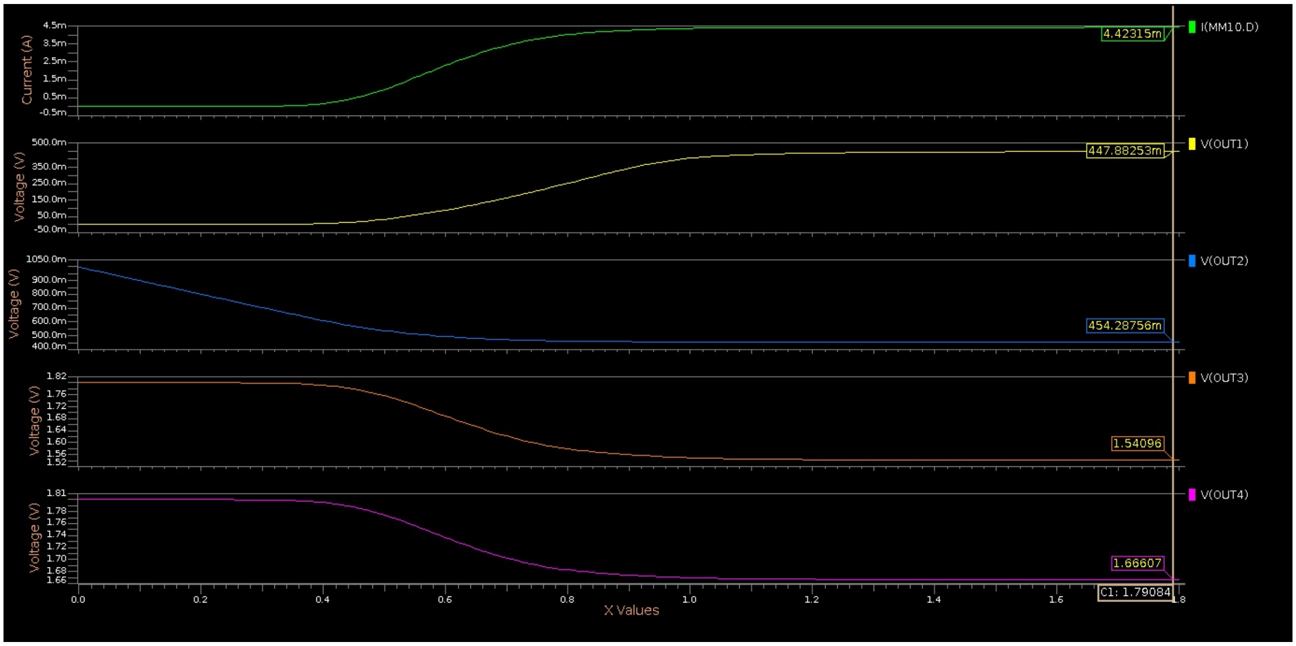

Figure 3: DC analysis of Telescope amplifier

6.2 AC analysis of Telescope amplifier

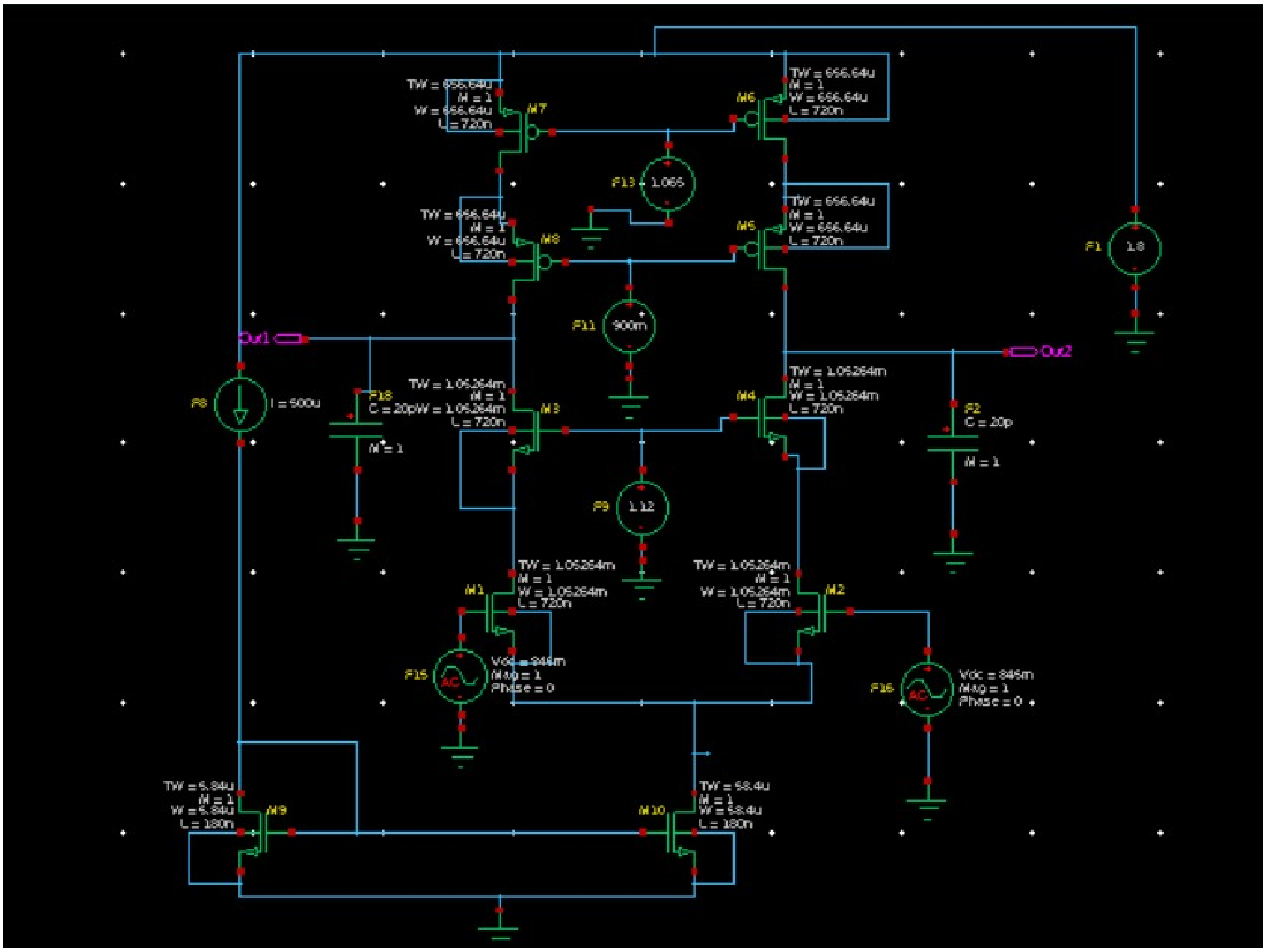

Figure 4: circuit diagram for AC analysis of Telescope amplifier

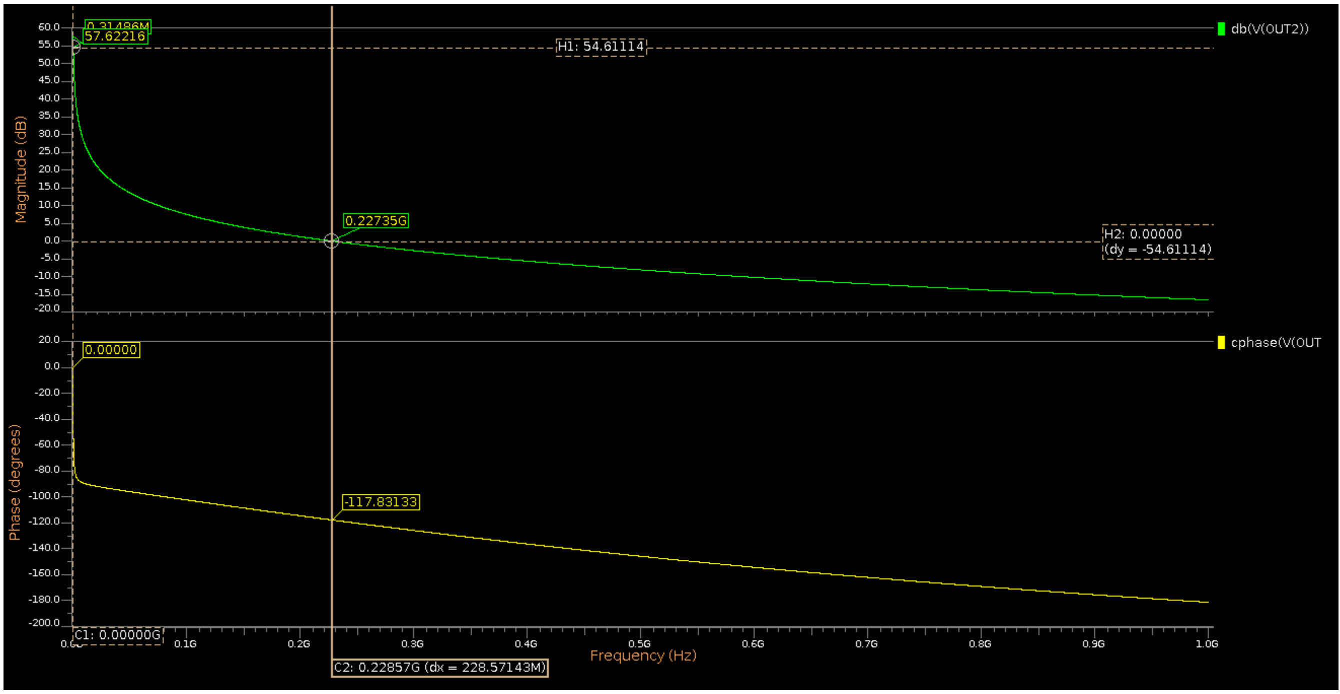

Figure 5: AC analysis of Telescope amplifier

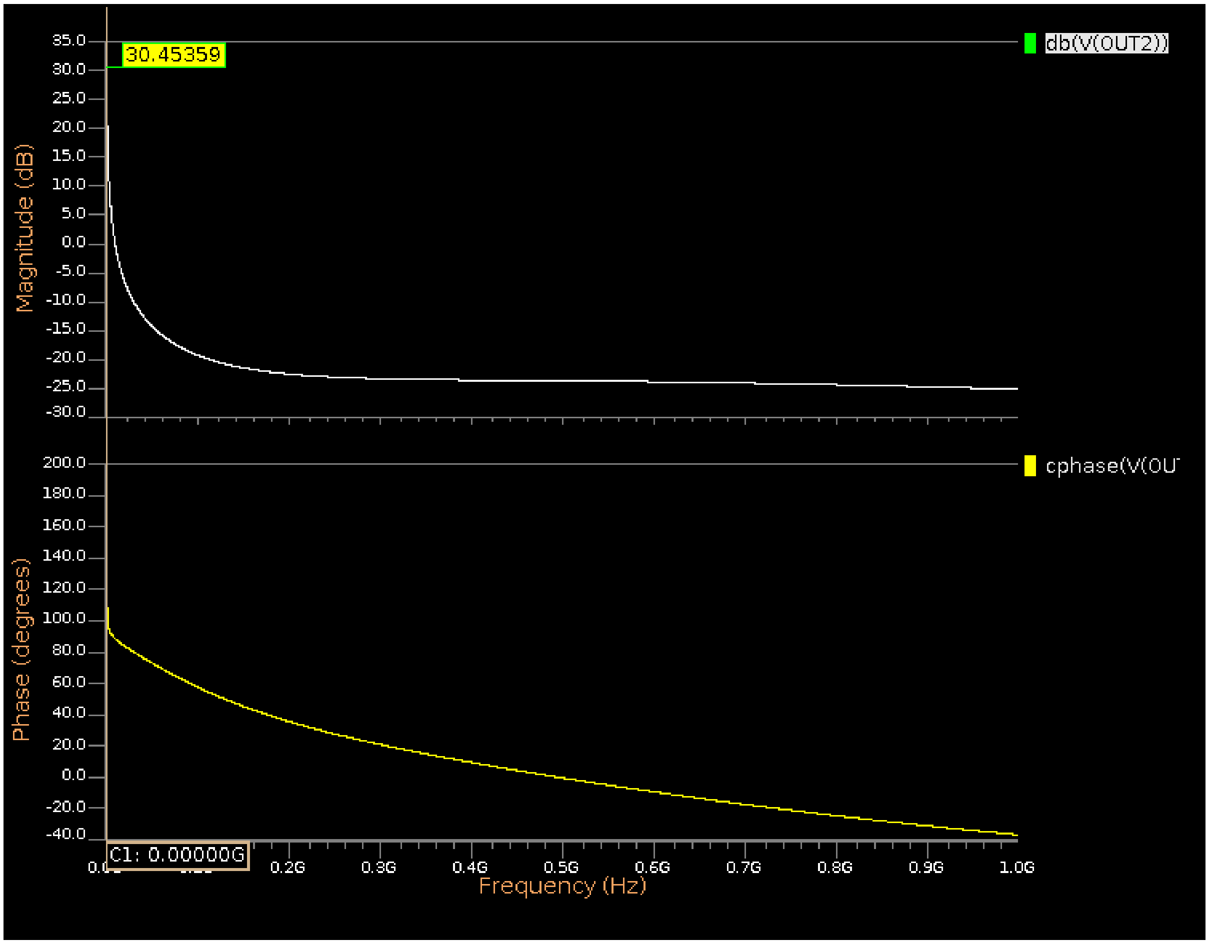

Figure 6: Common Mode gain of Telescope amplifier

6.3 PSRR analysis of Telescope amplifier

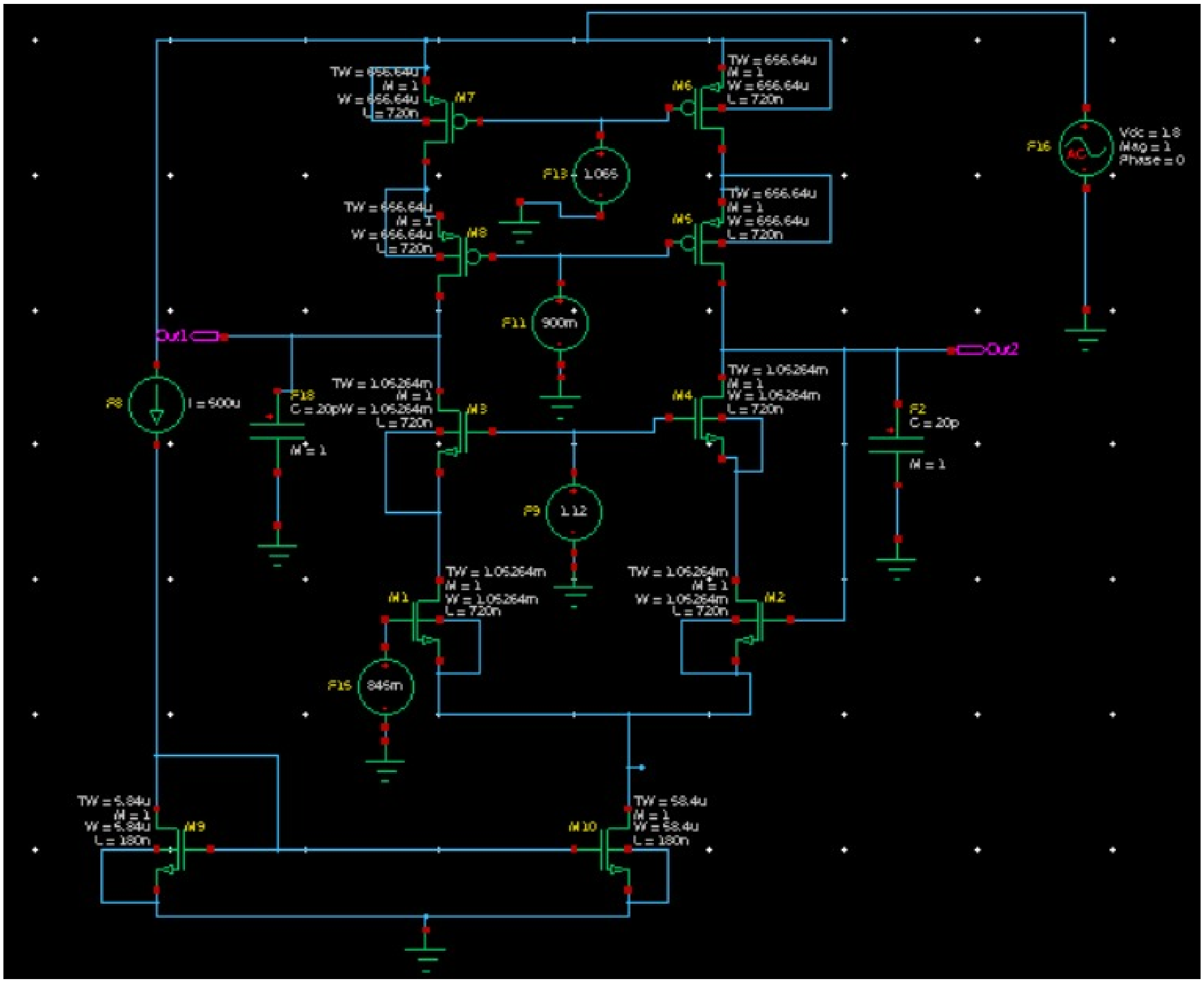

Figure 7: circuit diagram for PSRR analysis of Telescope amplifie

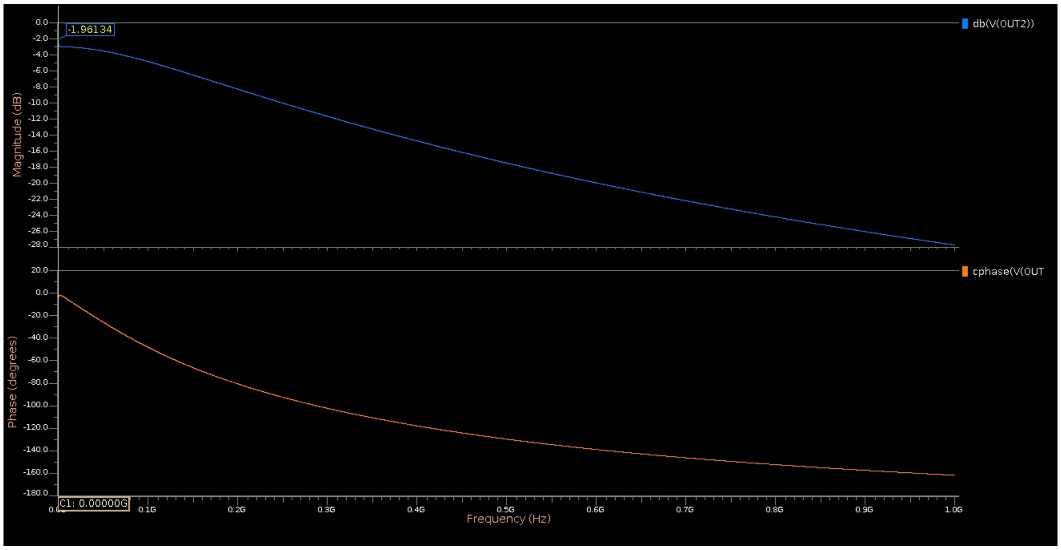

Figure 8: PSRR analysis of Telescope amplifier

6.4 ICMR and OCMR analysis of Telescope amplifier

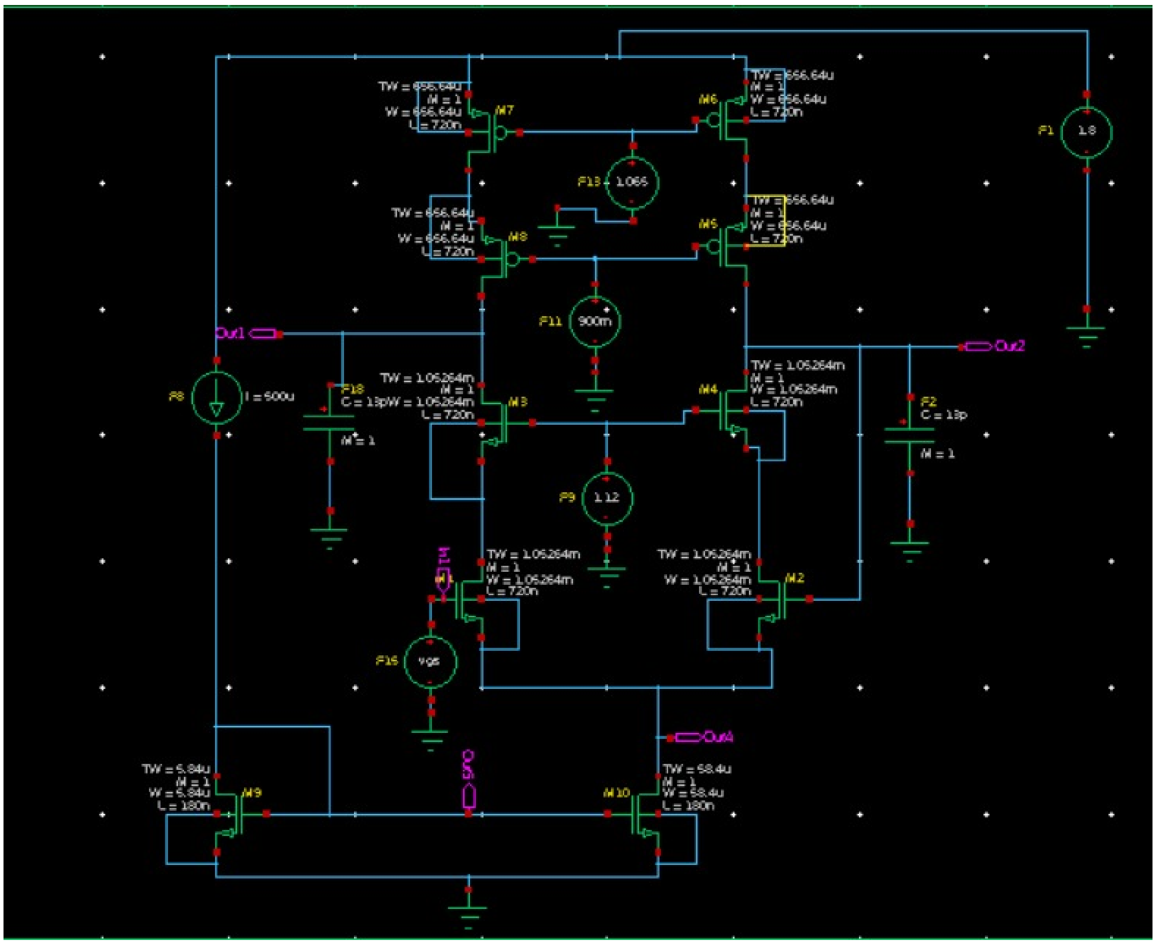

Figure 9: circuit diagram to find ICMR and OCMR analysis of Telescope amplifier

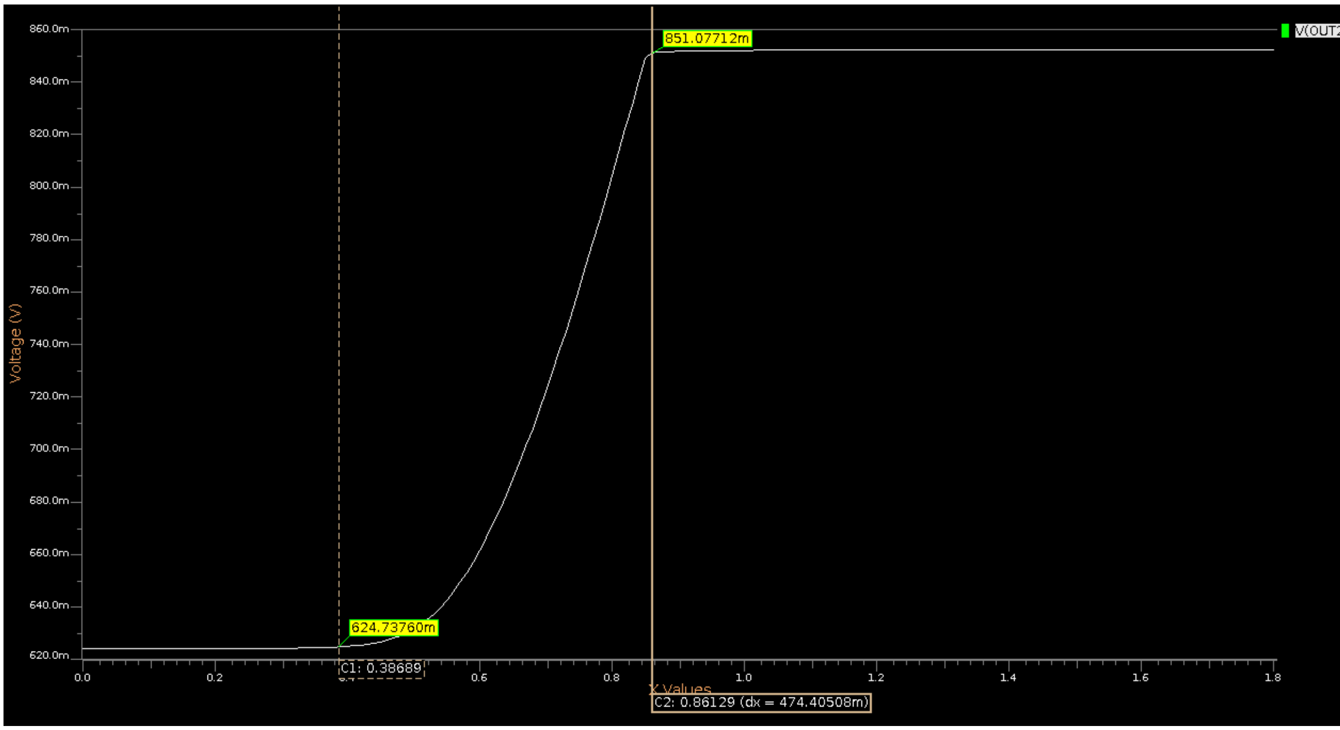

Figure 10: results of ICMR and OCMR analysis of Telescope amplifier

6.5 Slew rate

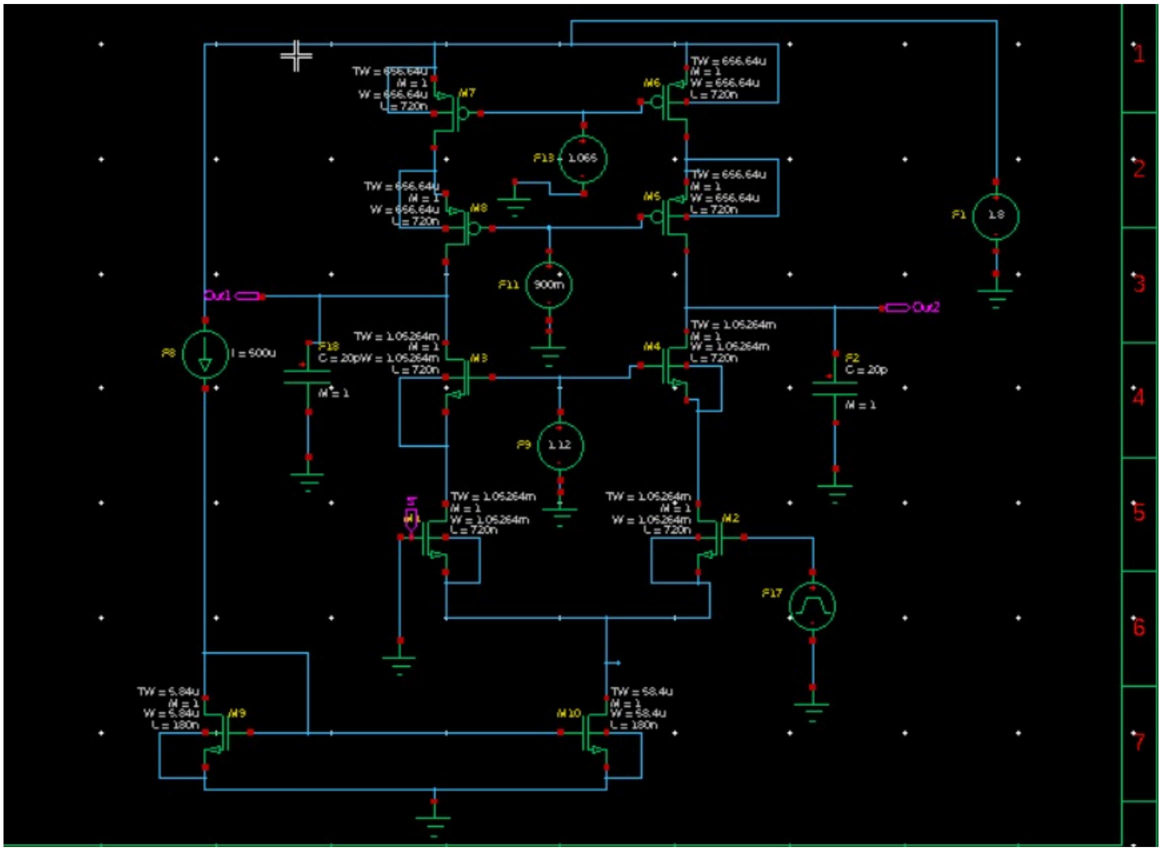

Figure 11: Circuit diagram to find the slew rate

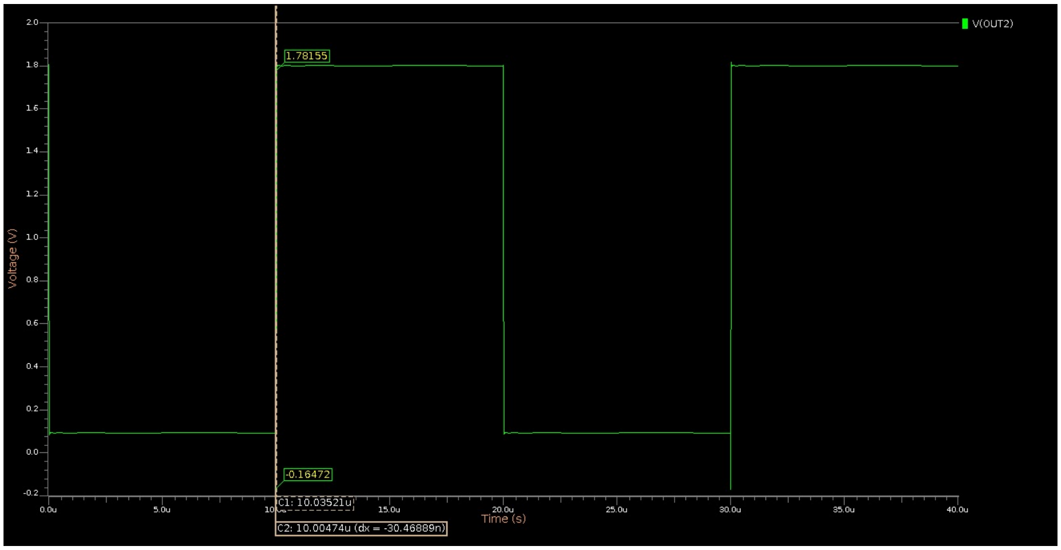

Figure 12: Results of slew rate

7 Comparsion Tables

7.1 (W/l) of all transistors

transistor	aspect ration	width	length
M1	1462	1.05m	720 nm
M2	1462	1.05m	720 nm
M3	1462	1.05m	720 nm
M4	1462	1.05m	720 nm
M9	10	58.5um	180nm
M5	1	5.85um	180nm
M7	912	655um	720nm
M8	912	655um	720nm
M6	912	655um	720nm
M5	912	655um	720nm

7.2 Bias voltages of transistors

transistor	V_G	V_{GS}	V_{DS}	I_D
M1	0.845v	0.539v	0.119v	2.089mA
M2	0.845v	0.539v	0.119v	2.089mA
M3	1.12v	0.693v	0.089v	2.089mA
M4	1.12v	0.693v	0.089v	2.089mA
M9	0.842	0.842	0.306	4.179 mA
M5	0.842	0.842	0.306	4.179 mA
M7	0.9	-0.709	-1.1	-2.089mA
M8	0.9	-0.709	-1.1	-2.089mA
M6	1.065	-0.735	0.191	-2.089mA
M5	1.065	-0.735	0.191	-2.089mA

7.3 Transient results

Variable	theoretical value	practicalvalue
slew rate	≥ 50	72.1
ICMR/OCMR max	–	0.853
ICMR/OCMR min	–	0.625

7.4 AC results

Variable	theoretical value	practicalvalue
gain	60 dB	57.612 dB
bandwidth	–	0.287 Mhz
GBW	$\geq$ 200Mhz	209 Mhz
PM	–	67.89
CMRR	–	29dB
PSRR	–	-2.71dB

8 Conclusions:-

- We have minimal resistance at the tail current mosfet as a result of the high current, so we receive low CMRR.
- All the results have been obtained practically and matching with the theoretical justification. The theoretical calculations have been done.