Himakar Gaddam

himakar.gaddam@gmail.com Las Cruces, NM 517-515-8828

OBJECTIVE

· Seeking a full time position in the area of Analog and Mixed-Signal IC Design where I can utilize my skills in the design process and while being innovative and resourceful, make a serious contribution to the company.

EDUCATION

Masters in Electrical Engineering, New Mexico State University AUG'14-DEC'15
· Las Cruces, NM **GPA**: 3.65/4.0
Courses: Digital VLSI Design, Analog VLSI Design, Computer Performance Analysis, ASIC Modeling & Synthesis, Random Signal Analysis, RF Microelectronics, Database Management System, Lean Tools for systems engineering.

Bachelors in Electronics and Communication Engineering, Osmania University SEP'10-MAY '14
· Hyderabad, India. **GPA**: 3.65/4.0

TECHNICAL SKILLS

Hardware Description Languages: Verilog
Programming Languages: C++, MySQL, and Core Java
IC Design and Testing Tools: Cadence IC tool suite OA (Virtuoso, Spectre Assura Analog artist XL, DRC and LVS extractions, Encounter RTL compiler)
Simulation Tools: MATLAB, Xilinx, LTspice.
Scripting languages: Python

EXPERIENCE

Intern at Defense Research Development Laboratory (DRDL), India Jan'14- May '14
PROJECT: Tracking of Maneuvering target using Kalman based estimator (MATLAB) - Implementation of effective 2D, 3D kalman filter for filtering noise content in received signal. We estimated the maneuvering aircraft state vectors (position, velocity, acceleration) using kalman filter (KF) and its variants like extended kalman filter (EKF) and unscented Kalman filter (UKF).

COURSE WORK AND ACADEMIC PROJECTS:

Analog Circuit Design: Designed, Simulated and laid out single stage amplifiers, differential amplifiers, current mirrors, Telescopic and Class-AB op-amps, OTA's and other circuits in cadence design environment. Familiar with poles and zeros analysis, frequency response, feedback systems, stability and frequency compensation.

CMOS Digital Circuit Design: Designed, simulated and laid out a DPLL that multiplies the input clock frequency from 180MHz to 900MHz, 16-bit Kogge-stone adder, 4-bit binary counter and other basic digital blocks such as flip-flops, static and dynamic logic gates, transmission gates, inverters/buffers.

Computer Performance Analysis: Techniques used to analyze performance of computer system workloads using statistical analysis techniques such as principal component analysis.

Design and Characterization of Standard Cells for Use in Synthesis Tools

- Created a library with standard cells using Complementary Static CMOS logic style. The custom library is used to synthesis a circuit from a logic coded in **Verilog** using **encounter** tool of **cadence**.

The same circuit is designed in custom approach using virtuoso of cadence and its characteristics are compared to the characteristics of the synthesized circuit.

REFERENCES: Available upon request