The application of Gate drain Underlap Architecture in TFET based inverters

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Abstract:

An emerging type of transistor device is TFETs, which are tunnel field transistors. MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are commonly used for low power electronic devices. Tunnel field-effect transistors (TFETs) have emerged as promising alternatives to conventional MOSFETs for low-power and high-performance integrated circuits. The structure of a TFET isvery close to that of a MOSFET, but with a different basic switching mechanism. TFET switching is performed by modulating quantum tunneling across the barrier rather than modulating thermionic emission across the barrier as in conventional MOSFETs. The purpose of this article is to survey TFET from its initial stages till now. This article studies and reviews the various types of TFETs available for design. The surface tunnel transistor is the first tunnel transistor to address speed, power and IOFF/ION ratio. Among the various gate design strategies, the concept of an underlay gate in TFET devices has received considerable attention in recent years.

TFETs are suitable for analog and RF applications because of their high on-state current, low ambipolar current, low SS, and low threshold voltage. This abstract presents a comprehensive overview of backing gate structures in TFET devices, focusing on their impact on device performance and design aspects. Gate overlap refers to the intentional misconnection between the source/drain regions and the gate electrode, resulting in physical overlap between the gate and channel regions. This design technique offers several advantages, including improved electrostatic control, reduced short-channel effects, improved subthreshold swing, and improved on-state current. In summary, this comprehensive review provides valuable insights into the technology of pad gate design for TFET devices. It serves as a reference for researchers and engineers involved in TFET device development, and provide a deeper understanding of the benefits and challenges associated with backing gate structures and their potential impact on future low-power and high-performance electronic devices.

Introduction:

The bottom gate of the Tunnel Field-Effect Transistor (TFET) device is a unique design feature that improves performance and energy efficiency. TFET is a type of transistor that uses quantum tunnelling phenomenon to achieve low power consumption and high switching speed. MOSFETs have played an important role in the development of many integrated circuits over the past half-decade,with their size now increasing to nano-meters. This bottom-gate configuration is specifically used to further optimize TFET performance and address some of the challenges associated with conventional transistor design. Increasing the size of the MOSFET to lower the power density results in a lower operating supply voltage.

In TFETs, low gate means that the gate electrode is deliberately mismatched or reduced compared to the source-channel region. This design choice creates an area of physical friction between the gate and source channel junctions. The p-i-n gate structure is used to represent the tunnel field transistor's structure. In addition, the bottom-gate design allows better control of the tunneling process in TFETs. Tunneling is the main mechanism that allows TFETs to exhibit low power performance.The main structural difference between TFET and MOSFETis the doping of the source and drain regions. The working principle of a TFET isa band tunnel, that is a p+ source where electrons are heavily doped from one energy band to another, and a lightly doped n-channel region junction (p+-n),i.e. a tunnel junction.

In addition, the bottom gate also helps reduce the Ambipolar conduction problem encountered in TFETs. In summary, the bottom gate configuration is a key design feature in TFET devices that improves performance and energy efficiency. It reduces leakage current, improves tunnel control, and reduces ambipolar conduction problems. Utilizing these advantages, bottom-gate TFETs have the potential to revolutionize low-power electronics and contribute to the development of energy-efficient computingsystems.

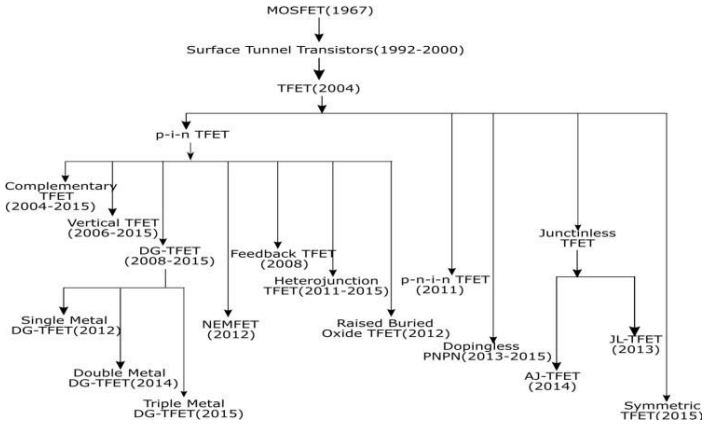


fig: Different structures of Mosfet and its evolution towards TFET.

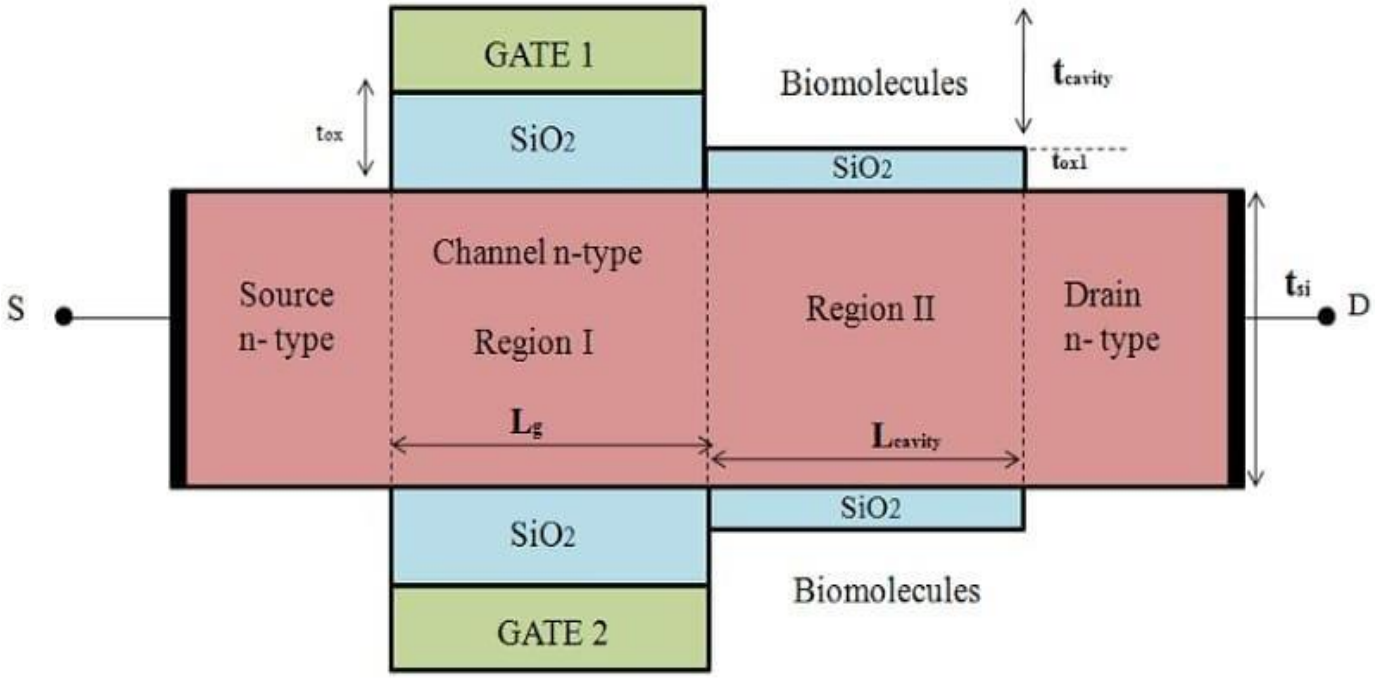
Tunnel Transistor has been evolved in 1992 by T. Baba, as one of the promising alternatives to the conventional MOSFET's based on various performance parameters as mentioned below:

Potential for exceeding the 60mV/decade sub- threshold swing.

- Ultra-low power and ultra-low voltage.
- Short Channel Effects.
- Reduction in the leakage currents.
- Exceeding the Speed requirements due to tunneling effects.
- Ability to work on sub-threshold and super-threshold voltage.
- Similarity in fabrication process as compared with MOSFET.
- Higher IOFF/ION current ratio .

Taking into consideration the above parameters, the MOSFET could be replaced by a potential substitute in terms of TFET for the purpose of high speed, ultra-low power, and energy efficient applications in the domain of integrated circuits . TFET from its inception in year 1992 to till May, 2015 with a brief introduction scaling of MOSFET and elaborated the exceeding performance of TFET with its conventional counterpart MOSFET.

Circuit Model:

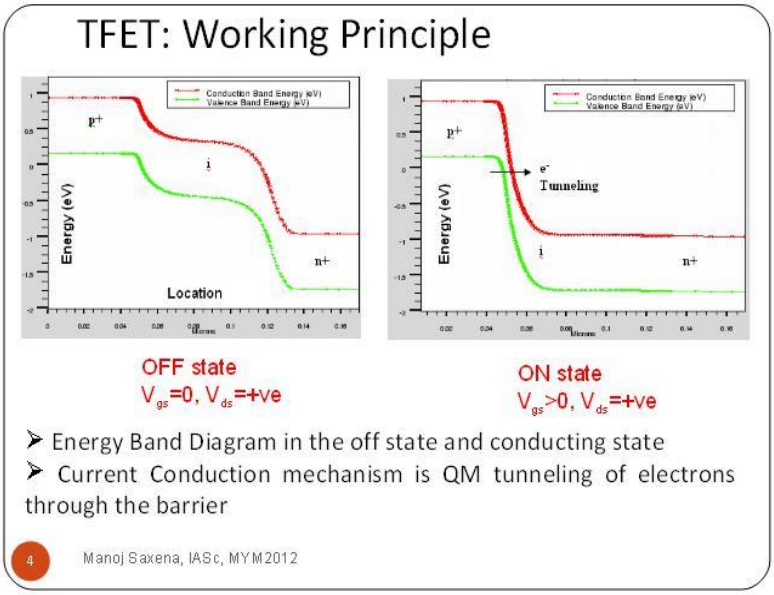


Working of the TFET:

The working principle of the under lap double-gate junction less MOSFET is as follows:

1. Structure: The transistor consists of a silicon channel between two gate electrodes, referred to as the double gate. The channel is typically doped with the same type of impurity to form a homogeneous semiconductor.
2. No Junctions: Unlike traditional MOSFETs, the junction less MOSFET does not have junctions (source/drain junctions) formed by different doping regions. Instead, the channel is uniformly doped.
3. Gate Control: The transistor's operation is controlled by applying voltages to the two gate electrodes. One gate is referred to as the control gate, while the other is the under lap gate.
4. Gate Voltages: By applying a positive voltage to the control gate and a negative voltage to the under lap gate, or vice versa, an electric field is created across the channel.
5. Channel Modulation: The electric field modulates the charge carriers (electrons or holes) within the channel, allowing for the control of the transistor's conductive properties.
6. Depletion Mode: Conversely, if the control gate voltage is low, the channel remains non-conductive, and the transistor operates in the "depletion mode." In this mode, the channel is depleted of charge carriers, resulting in high resistance between the source and drain.
7. Current Control: By adjusting the control gate voltage, the current flow through the transistor can be controlled, allowing for the amplification or switching of electrical signals.

The under lap double-gate junction less MOSFET offers several advantages, including improved control over channel properties, reduced leakage current, and enhanced device scalability. It is a promising transistor design for advanced nanoscale integrated circuits.



Gate overlap refers to the intentional misconnection between the source/drain regions and the gate electrode, resulting in physical overlap between the gate and channel regions. This design technique offers several advantages, including improved electrostatic control, reduced short-channel effects, improved sub threshold swing, and improved on-state current.

In summary, this comprehensive review provides valuable insights into the technology of pad gate design for TFET devices. It serves as a reference for researchers and engineers involved in TFET device development, and provides a deeper understanding of the benefits and challenges associated with backing gate structures and their potential impact on future low-power and high performance electronic devices.

Why TFET is needed?

To enhance the performance of TFET devices by improving sub threshold slope, increasing tunneling probability , Ambipolar, Conduction , Reducing short channel effects and enabling compatibility with low-power applications.

Mainly aimed at improving device performance. TFET's depends on quantum tunnelling for carrier transport across a narrow band gap semiconductor channel. Main Principle depends on

1. Enhanced tunneling probability: where under lap gate increases the electric field strength at source-channel junction.
2. Reduced leakage current: by reducing gate-channel overlap, under lap gate helps to minimize the Electric field.
3. Sub threshold Swing: this allows more efficient between on and off states.

The working principle of a TFET is a band tunnel, that is a p+ source where electrons are heavily doped from one energy band to another, and a lightly doped n-channel region junction (p+-n), i.e. a tunnel junction. In addition, the bottom gate also helps reduce the ambipolar conduction problem encountered in TFETs.

In summary, the bottom gate configuration is a key design feature in TFET devices that improves performance and energy efficiency. It reduces leakage current, improves tunnel control, and reduces ambipolar conduction problems.

Utilizing these advantages, bottom-gate TFETs have the potential to revolutionize low-power electronics and contribute to the development of energy-efficient computing systems. Scaling down of the MOSFET for the sake of reducing the power density resulted into reduction in the operating supply voltage as well.

Oxide TFET, Junctionless TFET, Double gate TFET(DG-TFET), Vertical TFET, Dopingless PNPN TFET are studied. The design parameters which have been developed in year 2015 have been explored to a maximum extent.

TFET device physics and operation band to band:

Equation is a common way to express BTBT transmission. Here in-the electron effective mass, ħ-Planck's constant divided by 2×2π, Eg is the band gap of the semiconductor material at the tunnel junction, and F is the electric field measured in V/m. This equation can be improved slightly by making it more specific to tunneling transitory .

There are four important conditions in order for band-to-band tunneling to take place:

1. Available states to tunnel-from,
2. Available states to tunnel-to,
3. An energy barrier that is sufficiently narrow for tunneling to take place and
4. Conservation of momentum.

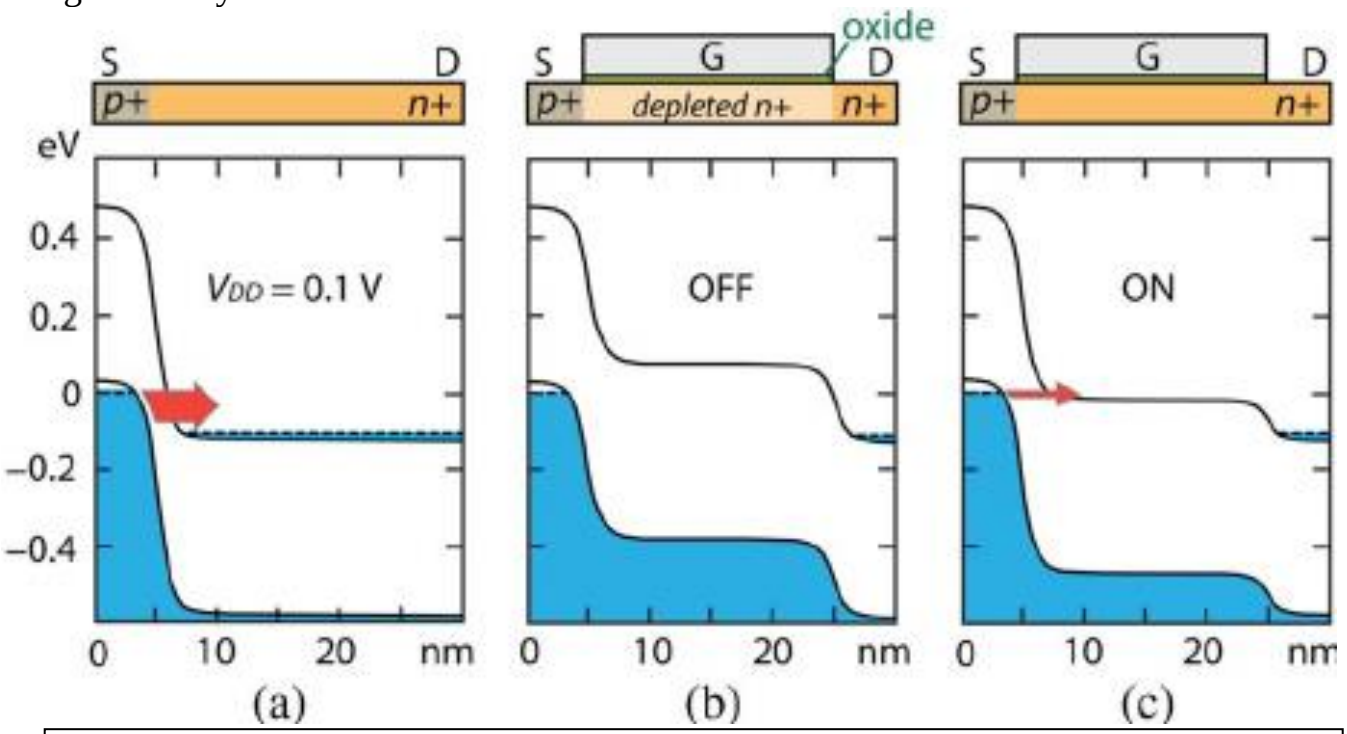


Fig: Energy band diagram and layer structure for an n TFET consisting of an n þ source (S), p þ drain (D), and gate (G). In (a) the Zener

Application:

- TFET is suitable for analog applications and radio frequency application because of its high ON state current, low ambipolar current, low SS and low threshold voltage.
- A field-effect transistor (FET) is a type of transistor that uses an electric field to control the current flow through a semiconductor channel. FETs are widely used in electronic circuits due to their high input impedance, low output impedance and high gain.
- TFETs are considered to be superior to that of MOSFETs and future work involves the designing of DG TFET with different materials to make it more suitable for RF/ analog or mixed signal circuit applications.
- Low power electronics.
- Ultra-Low power circuits with High speed.
- Analog-mixed circuits.

Table II. Performance Parameters

Tunnel FET device	Device Performance Parameters			
	Sub threshold swing (SS) in mV/dec	On current (Ion) in mA/um	Off current (Ioff) in nA/um	Ion to Ioff ratio
Double gate Si TFET	116.3	0.00252	9.43×10^{-8}	10^{11}
Hetero junction double gate TFET	95.64	0.0201	0.196	1.53×10^{4}
InAs based double gate TFET	61.2	0.24	3.39	7.13×10^{4}

Advantages:

The main benefits of using a FET in your electronics design are:

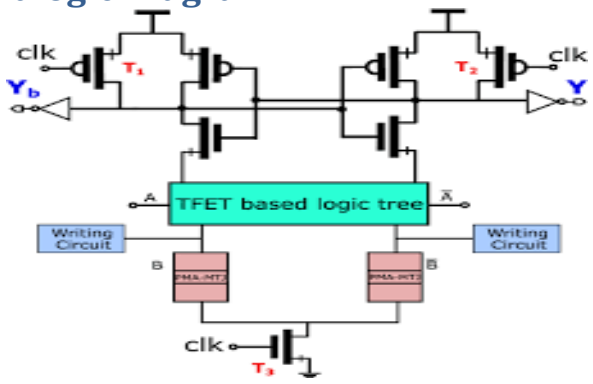
They are

- Small and inexpensive
- require little or no power for operation
- have a fast switching time
- provide a stable input voltage and have high efficiency

TFETs have advantages such as low off-state current (Ioff),low sub threshold swing(SS), and low power consumption compared with the conventional metal-oxide semiconductor field-effect transistors (MOSFETs).

Improved sub threshold swing: TFETs exhibit lower sub threshold swing (SS) values compared to traditional MOSFETs. Sub threshold swing is a measure of how efficiently a transistor can turn on and off, and lower values indicate better performance.

Circuit logic Diagram



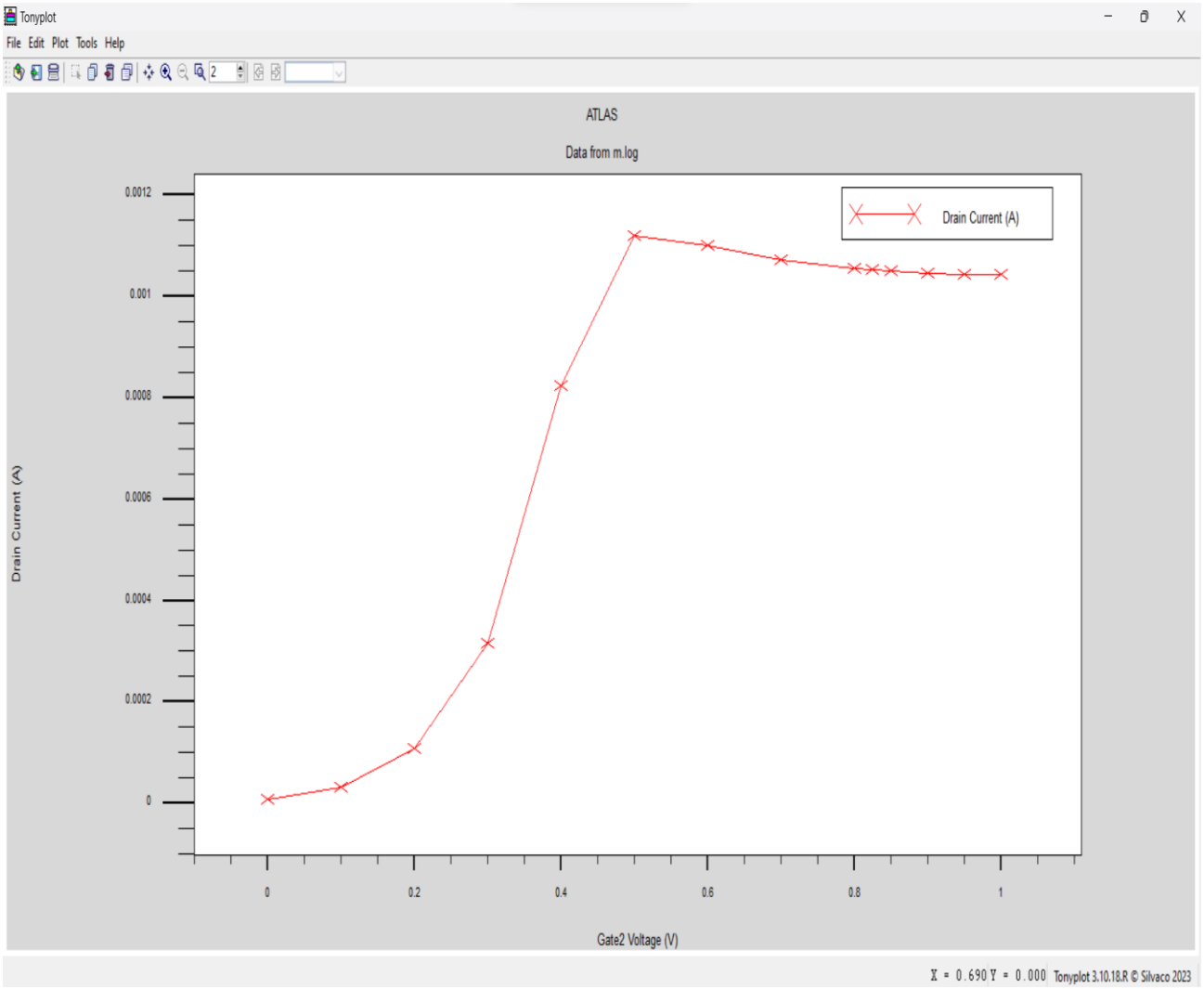
The under lap gate design helps to reduce the SS in TFETs, leading to improved energy efficiency and Improved sub threshold swing: TFETs exhibit lower sub threshold swing(SS) values compared to traditional MOSFETs , power consumption.

The underlap gate design can increase the on-state current of TFET

Better control over device characteristics:

- Ultra-low power and ultra-low voltage.
- Short Channel Effects.
- Reduction in the leakage currents.
- Exceeding the Speed requirements due to tunneling effect
- Ability to work on sub-threshold and super-threshold.

Output Graph



Advantages

The gate-drain underlap architecture offers several advantages in TFET-based inverters. Firstly, it enables lower subthreshold swing, improving the energy efficiency of the device. Secondly, it enhances the on-state current, allowing for higher speed and performance.

Lastly, it reduces the off-state leakage current, leading to lower power consumption and improved overall efficiency. These advantages make the gate-drain underlap architecture a promising approach for enhancing TFET-based inverter performance

Potential Applications:

The gate-drain underlap architecture has potential applications in various fields. It can be utilized in low-power integrated circuits, where energy efficiency is crucial. Additionally, it can find applications in high-performance computing, where improved device speed and reduced power consumption are desired. Furthermore, the gate-drain underlap architecture can be employed in renewable energy systems, enabling efficient power conversion. Its versatility makes it a promising architecture for a wide range of applications.

Conclusion:

In conclusion, the gate-drain underlap architecture in TFET-based inverters offers significant potential for enhancing efficiency and performance. By carefully designing the underlap length, we can achieve improved subthreshold swing, on-state current, and leakage current. The advantages of this architecture make it suitable for various applications in low-power integrated circuits, high- performance computing, and renewable energy systems. Embracing the gate-drain underlap architecture can pave the way for more efficient and high-performance TFET-based inverters.