Curriculum Vitae

Akhil Alla

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Career Objectives:

I seek challenging opportunities in Physical design where I can fully use my skills and knowledge for the success of the organization and establish a career for myself.

Academic Qualification:

- B.Tech(ECE) in Godavari institute of engineering and technology at Rajahmundry in 2016
- Diploma (ECE) in Godavari institute of engineering and technology at Rajahmundry in 2013.
- SSC in Nirmala English medium high school at Gowripatnam in 2010.

Technical Skills:

- Trained in Physical design for 8 months in **µlsi academy.**
- Trained in Physical verification DRC & LVS by using Calibre.
- Basics on TCL scripting and linux.
- Hands on experience on mentor graphics Nitro-Soc PNR tool.

Physical design Course Outline:

Digital electronics basics, CMOS fundamentals, ASIC design flow, PNR flow floorplanning, placement, clock tree synthesis and routing and physical verification.

Tools Used:

- Nitro-Soc PNR tool.
- Calibre.

Project:

Name	:	Processor
Layers	:	10 layers
Technology	:	45nm
Frequency	:	400MHz
Block area(sq.micron)	:	40372.416
Standard cell count	:	15061
What are all done for about the block	:	Floorplan, Placement and CTS.

Physical Design:

In the first step we do the floorplanning. In floorplanning Macro, I/O pad and physical cells (Tap, End cap) placement can be done and blockages are placed in floorplan level. In power planning we are creating a power grid such that all cells in the design will get power. After completion of power planning we go for placement to place standard cells. By the proper legalization we can avoid cell overlap.

In CTS, the goal is to propagate a clock to all sequential cells so we are building a clock tree with minimum skew and latency. After that we go for clock tree optimization to meet skew. The next step is signal routing. In the routing stage, on the routing grid the metal can be routed. The routing blockages will be removed at this stage. After the routing the database will go for signoff checks (STA, IR drop, DRC, LVS).

Physical Verification: DRC, LVS

In LVS, I verified the design to check any opens or shorts. To verify LVS, first we have to create spice netlist for layout and netlist after that only the both can be compared and result SVDB file created. The report file is created with results in database. In the report file the errors with locations can be showed.

Similarly in LVS, I checked DRC's for a routing databases and analyzed if any design violations are present. If any violations are in GDS file, I created a report file and send back to design engineer. The area based and incremental DRC can be done if the design is too long or if it needs to check selected area. If the design is too long, To save run time I run DRC to the design with selected checks only.

Personal Details :

Date of Birth	:	6/July/1995
Gender	:	Male
Father Name	:	Koteswara Rao
Marital Status	:	Unmarried
Nationality	:	Indian
Languages Known	:	English & Telugu
Permanent Address	:	Akhil Alla Duddukuru Devarapalli M.D West Godavari dist (Andhra Pradesh)

I hereby declare the information and the facts stated here is above true and the best of my knowledge and belief. I assure you that I will do my job with much dedication for the development of organization.

Place: Bangalore

Date:

Yours faithfully

Akhil Alla