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#-----------------------------------------------------------
# Vivado v2022.2 (64-bit)
# SW Build 3671981 on Fri Oct 14 05:00:03 MDT 2022
# IP Build 3669848 on Fri Oct 14 08:30:02 MDT 2022
# Start of session at: Sat May  6 17:00:52 2023
# Process ID: 39768
# Current directory:
C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Clu
ster.runs/synth_1
# Command line: vivado.exe -log Giga_Cluster.vds -product Vivado
-mode batch -messageDb vivado.pb -notrace -source Giga_Cluster.tcl
# Log file:
C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Clu
ster.runs/synth_1/Giga_Cluster.vds
# Journal file:
C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Clu
ster.runs/synth_1\vivado.jou
# Running On: Vamsi, OS: Windows, CPU Frequency: 2611 MHz, CPU
Physical cores: 10, Host memory: 16832 MB
#-----------------------------------------------------------
source Giga_Cluster.tcl -notrace
Command: read_checkpoint -auto_incremental -incremental
C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Clu
ster.srcs/utils_1/imports/synth_1/Giga_Cluster.dcp
INFO: [Vivado 12-5825] Read reference checkpoint from
C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Clu
ster.srcs/utils_1/imports/synth_1/Giga_Cluster.dcp for incremental
synthesis
INFO: [Vivado 12-7989] Please ensure there are no constraint
changes
Command: synth_design -top Giga_Cluster -part xazu3eg-sfvc784-1Q-q
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device
'xazu3eg'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or
device 'xazu3eg'
INFO: [Designutils 20-5440] No compile time benefit to using
incremental synthesis; A full resynthesis will be run
INFO: [Designutils 20-4379] Flow is switching to default flow due
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to incremental criteria not met. If you would like to alter this
behaviour and have the flow terminate instead, please set the
following parameter config_implementation
{autoIncr.Synth.RejectBehavior Terminate}
INFO: [Synth 8-7079] Multithreading enabled for synth_design using
a maximum of 2 processes.
INFO: [Synth 8-7078] Launching helper process for spawning children
vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 20744
INFO: [Synth 8-11241] undeclared symbol 'REGCCE', assumed default
net type 'wire'
[D:/Xilinx/Vivado/2022.2/data/verilog/src/unimacro/BRAM_SINGLE_MACR
O.v:2170]
---------------------------------------------------------------------
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Starting Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:05
. Memory (MB): peak = 1442.441 ; gain = 408.469
---------------------------------------------------------------------
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INFO: [Synth 8-638] synthesizing module 'Giga_Cluster'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/new/Giga_Cluster.vhd:43]
INFO: [Synth 8-638] synthesizing module 'Mega_Cluster'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/Mega_Cluster.vhd:42]
INFO: [Synth 8-638] synthesizing module 'Mini_Cluster'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/Cluster.vhd:47]
INFO: [Synth 8-638] synthesizing module 'CU'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/CU.vhd:48]
INFO: [Synth 8-638] synthesizing module 'D_flipflop'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/D_flipflop.vhd:41]
WARNING: [Synth 8-614] signal 'curr_val' is read in the process but
is not in the sensitivity list
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/D_flipflop.vhd:44]
INFO: [Synth 8-256] done synthesizing module 'D_flipflop' (0#1)
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[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/D_flipflop.vhd:41]
INFO: [Synth 8-226] default block is never used
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/CU.vhd:67]
INFO: [Synth 8-256] done synthesizing module 'CU' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/CU.vhd:48]
INFO: [Synth 8-256] done synthesizing module 'Mini_Cluster' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/Cluster.vhd:47]
INFO: [Synth 8-256] done synthesizing module 'Mega_Cluster' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/Mega_Cluster.vhd:42]
INFO: [Synth 8-638] synthesizing module 'MegaCluster2'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster2/MegaCluster2.src
s/sources_1/new/MegaCluster2.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'MegaCluster2' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster2/MegaCluster2.src
s/sources_1/new/MegaCluster2.vhd:42]
INFO: [Synth 8-638] synthesizing module 'MegaCluster3'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster3/MegaCluster3.src
s/sources_1/new/MegaCluster3.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'MegaCluster3' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster3/MegaCluster3.src
s/sources_1/new/MegaCluster3.vhd:42]
INFO: [Synth 8-638] synthesizing module 'MegaCluster4'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MEgaCluster4/MegaCluster4.src
s/sources_1/new/MegaCluster4.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'MegaCluster4' (0#1)
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MEgaCluster4/MegaCluster4.src
s/sources_1/new/MegaCluster4.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'Giga_Cluster' (0#1)
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[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/new/Giga_Cluster.vhd:43]
WARNING: [Synth 8-7129] Port C[2] in module CU is either
unconnected or has no load
---------------------------------------------------------------------
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Finished Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:06
. Memory (MB): peak = 1532.895 ; gain = 498.922
---------------------------------------------------------------------
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---------------------------------------------------------------------
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Finished Constraint Validation : Time (s): cpu = 00:00:01 ; elapsed
= 00:00:06 . Memory (MB): peak = 1532.895 ; gain = 498.922
---------------------------------------------------------------------
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---------------------------------------------------------------------
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Start Loading Part and Timing Information
---------------------------------------------------------------------
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Loading part: xazu3eg-sfvc784-1Q-q
INFO: [Synth 8-6742] Reading net delay rules and data
INFO: [Device 21-403] Loading part xazu3eg-sfvc784-1Q-q
---------------------------------------------------------------------
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Finished Loading Part and Timing Information : Time (s): cpu =
00:00:01 ; elapsed = 00:00:07 . Memory (MB): peak = 1532.895 ; gain
= 498.922
---------------------------------------------------------------------
-------------
WARNING: [Synth 8-327] inferring latch for variable 'Q_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/D_flipflop.vhd:48]
WARNING: [Synth 8-327] inferring latch for variable 'curr_val_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/D_flipflop.vhd:46]
WARNING: [Synth 8-327] inferring latch for variable 'Y_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
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uster.srcs/sources_1/imports/new/CU.vhd:55]
WARNING: [Synth 8-327] inferring latch for variable 'OUTPUT_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/new/Mega_Cluster.vhd:116]
WARNING: [Synth 8-327] inferring latch for variable 'OUTPUT_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster2/MegaCluster2.src
s/sources_1/new/MegaCluster2.vhd:97]
WARNING: [Synth 8-327] inferring latch for variable 'OUTPUT_reg'
[C:/Users/vamsi/OneDrive/Desktop/VHDL/Project2/Giga_Cluster/Giga_Cl
uster.srcs/sources_1/imports/Project2/MegaCluster3/MegaCluster3.src
s/sources_1/new/MegaCluster3.vhd:98]
---------------------------------------------------------------------
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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:01 ;
elapsed = 00:00:07 . Memory (MB): peak = 1532.895 ; gain = 498.922
---------------------------------------------------------------------
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No constraint files found.
---------------------------------------------------------------------
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Start RTL Component Statistics
---------------------------------------------------------------------
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Detailed RTL Component Info :
+---Adders :
       2 Input    5 Bit       Adders := 64
       3 Input    4 Bit       Adders := 64
+---XORs :
       2 Input      4 Bit         XORs := 64
+---Muxes :
       2 Input   40 Bit        Muxes := 1
---------------------------------------------------------------------
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Finished RTL Component Statistics
---------------------------------------------------------------------
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---------------------------------------------------------------------
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Start Part Resource Summary
-----------------------------------------------------------------------
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Part Resources:
DSPs: 360 (col length:72)
BRAMs: 432 (col length: RAMB18 72 RAMB36 36)
-----------------------------------------------------------------------
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Finished Part Resource Summary
-----------------------------------------------------------------------
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```