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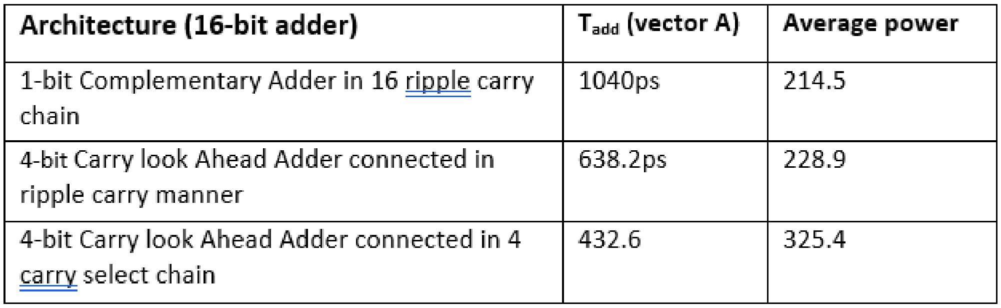
ECE 637 Project 3

Introduction: This project will study and analyze various 16-bit adders and sort out which gives the better output for the given specifications. As the adders play a vital role in electronic circuits, we select the best 16-bit adder by considering all the factors such as speed, power, and area. Further, we will also perform different processes at different temperatures and calculate delay and power delay products, respectively.

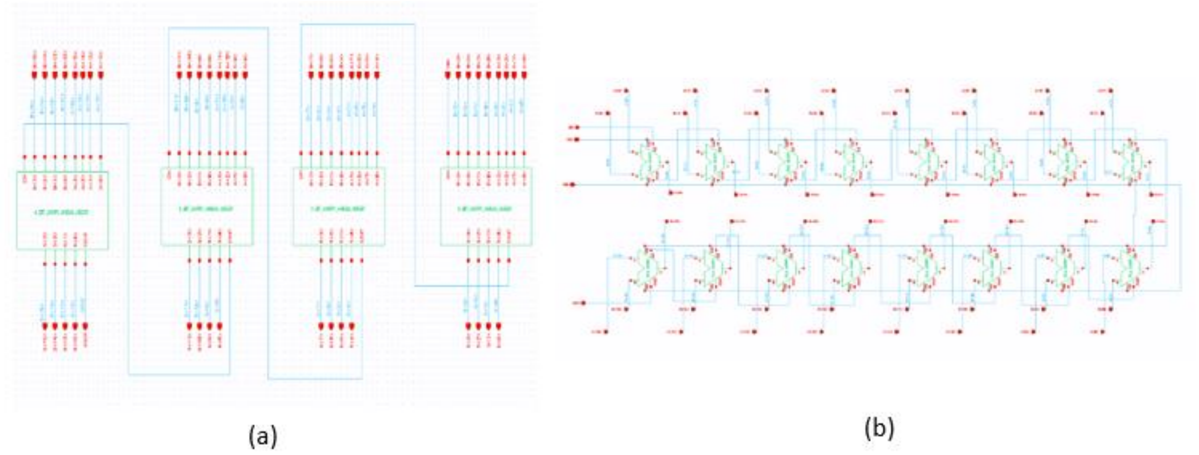
Review and simulation of different of adder architectures: For implementing a 16-bit adder, there are several architectures so, to analyze, we will use vector A (1111 1111 1111 1111 + 0000 0000 0000 0001) to observe the delay and select the required adder. Figure 1 shows the different adders with delay and average power at the TT corner at 27C. First in the list is a 1-bit Complementary adder in a ripple carry chain where 1-bit adders are connected in a ripple chain manner which has less number of transistors among all. Though it has less area and low power, it is prolonged. The delay is also more because each adder output is dependent on the previous adder output.



Architecture (16-bit adder)	**T_{add} (vector A)**	**Average power**
1-bit Complementary Adder in 16 ripple carry chain	1040ps	214.5
4-bit Carry look Ahead Adder connected in ripple carry manner	638.2ps	228.9
4-bit Carry look Ahead Adder connected in 4 carry select chain	432.6	325.4

Figure 1: Adder Architecture comparison using vector A at 27C and TT

To overcome, we choose to carry a look-ahead adder. Where carry is computed parallel with the sum and does not depend on any block as a ripple adder, we can see that the delay has declined in 4-bit carry look ahead connected in the ripple carry chain. Further, to meet the specifications mentioned, we improve such that 4- bit carry look-ahead adder is used to form the carry select method.



(a) (b)

Figure-2 Architectures of 1-bit Complementary Adder in 16 ripple chain and 4-bit CLA Adder connected in

Architecture and transistor-level circuit design 16-bit carry look ahead adder:

The 16-bit adder is built using repetitive 4-bit carry look ahead adder. In this 4-bit adder base cell, the carry for higher order bits are generated simultaneously. The following algorithm was used to generate these carry bits

$P_i = A_i + B_i$; $G_i = A_i . B_i$; $C_{i+1} = G_i + P_i.C_i$. And forcalculating sum bits, $S_i = P_i$ XOR C_i, where i=0,1,2,3

$C_1 = G_0 + P_0.C_{in}$; $C_2 = G_1 + P_1.C_1 = G_1 + P_1.(G_0 + P_0.C_{in}) = G_1 + P_1.G_0 + P_1.P_0.C_{in}$

$C_3 = G_2 + P_2.C_2 = G_2 + P_2.(G_1 + P_1.G_0 + P_1.P_0.C_{in}) = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_{in}$

$C_4 = G_3 + P_3.C_3 = G_3 + P_3.(G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2. P_1.P_0.C_{in}) = G_3 + P_3G_2 + P_3P_2.G_1 + P_3P_2.P_1.G_0 + P_3P_2.P_1.P_0.C_{in}$
For sum bits: $S_0 = P_0$ XOR C_{in}; $S_1 = P_1$ XOR C_1; $S_2 = P_2$ XOR C_2; $S_3 = P_3$ XOR C_3

A 4-bit sub-block was used to form 16-bit carry-select adder. In this, the computation for S_{4-7} and C_{5-8} takes place simultaneously for C_4 = ‘1’ and C_4 = ‘0’. A mux is used to select the final output S_{4-7} and C_{5-8} when C_4 computation is finished. Similarly, computation of (S_{4-7} , C_{5-8}) and (S_{4-7} , C_{5-8}) takes place. The complete 16-bit diagram is shown in Figure 3.

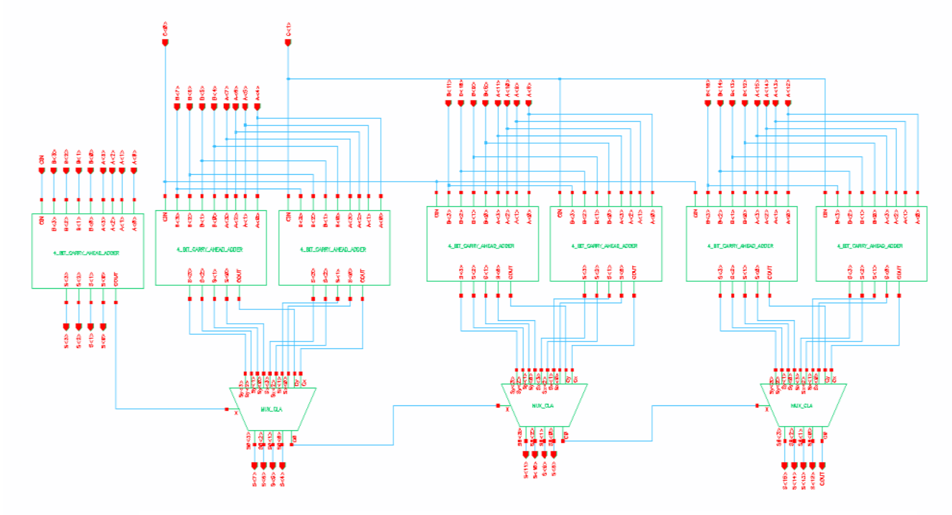


Figure 3: 16_bit adder using carry select method

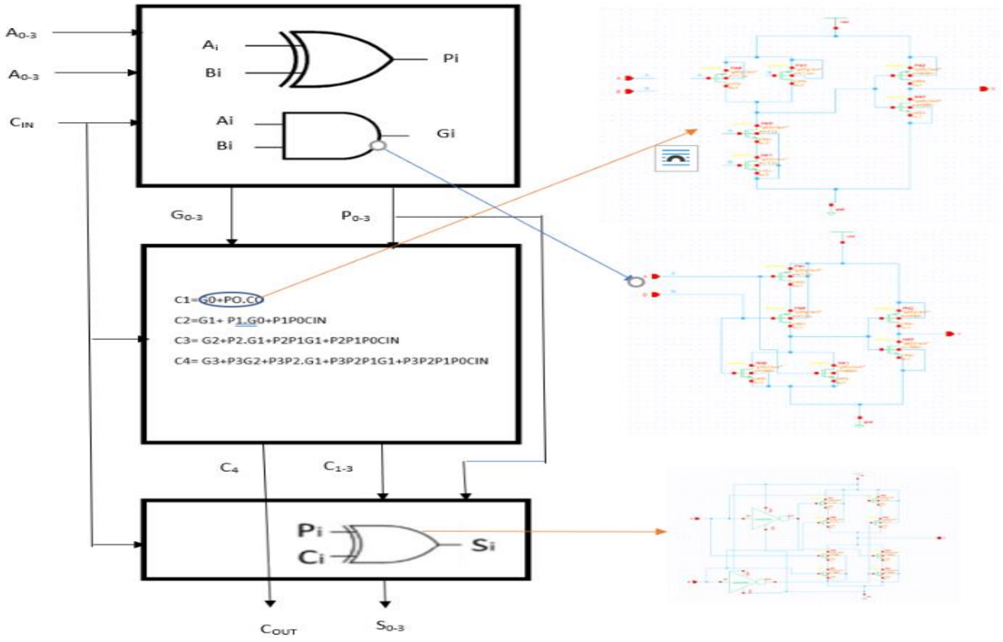


Figure 4 : Architecture of 4 bit carry ahead adder

Simulation results and analysis

To analyze the simulation results we need to add all the three given vectors. A = 1111 1111 1111 1111 + 0000 0000 0000 0001; Vector B = 1111 1111 1111 1111 + 1111 1111 1111 1111; and Vector C = 10101 1010 1010 1010 + 1010 1010 1010 1010. The output Cout, S15-0 for vector A, vector B and vector C are [carry=1, 0000 0000 0000 0000], [carry=1, 1111 1111 1111 111]}, and [carry=1, 0101 0101 0101 0100] respectively. All the results at different corners and temperatures were performed and depicted in table 1.

For all vectors, the delay is lowest at the FF corner and -25C and longest at the SS corner and 85C. It was also determined that the power was most significant in the SS corner and at 85C. This was caused by a slow slew rate of the internal signals, which resulted in a higher short circuit current.

vector	Process	Tempuratute	Delay(ps)	Power(uW)	PDP(fJ)
A	FF	-25	373.5	336	125.496
A	TT	27	432.6	325.4	140.768
A	SS	85	611.8	321.5	196.693
B	FF	-25	169.7	524.5	89.007
B	TT	27	199.6	509.64	101.724
B	SS	85	284.4	506.2	143.963
C	FF	-25	158.8	519.2	82.448
C	TT	27	199.5	504.4	100.627
C	SS	85	284.4	501.4	142.598

Table 1: delay, power and PDP for vector A, B and C

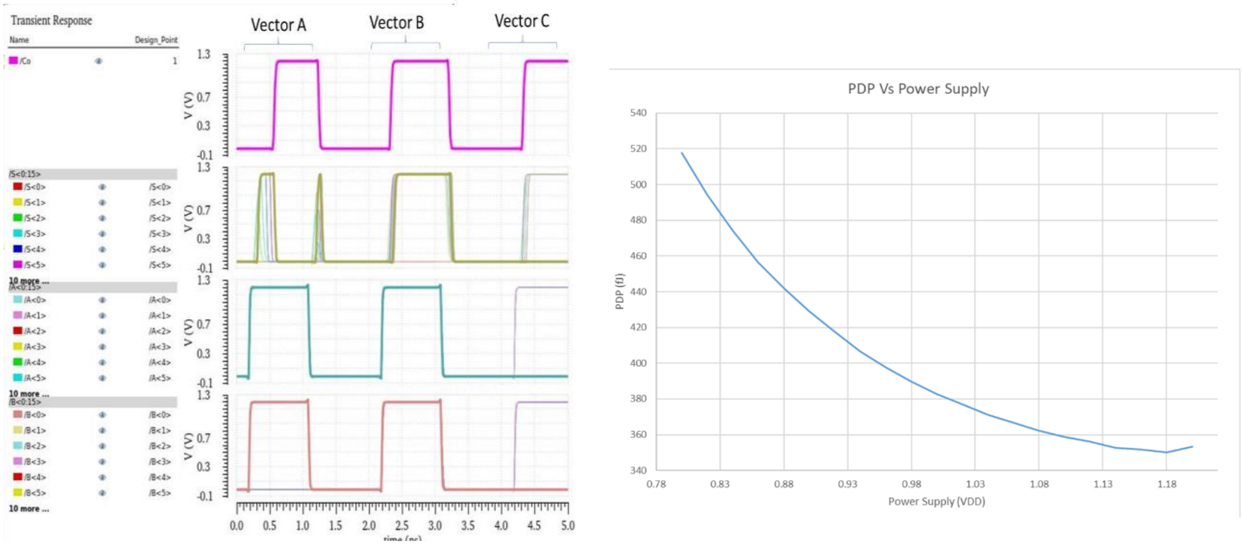


Figure 5:(a) Functional wave forms of vector A B and C (b)PDP vs VDD

Conclusion: In this project, various adder architectures with different transistor models were studied. A 16-bit adder was designed using carry-lookahead and carry select adder techniques. Adder delay was calculated at different corners and temperatures and analyzed. A plot depicting power delay product and supply voltage has been performed