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ECE-637 Project-2

Introduction and Motivation: The full adder is a three-number digital component that is implemented using logic gates. It is the most important component inside a processor's ALU, and it is used to increment addresses, table indexes, buffer pointers, and other locations where addition is necessary. The project also assists in the learning of cadence tools and the creation of sophisticated circuit configurations. This project helps in the understanding of circuit variations associated with a global and local mismatch, which is one of the major issues in VLSI, especially as transistor sizing

Circuit Design and Transistor sizing: Table 1 shows the truth table for a 1-bit full adder. The inputs are A, B, and CIN, whereas the outputs are S, and COUT. Figure 1 shows the implementation circuit, which is made up of 28 transistors and is called complementary static CMOS logic.

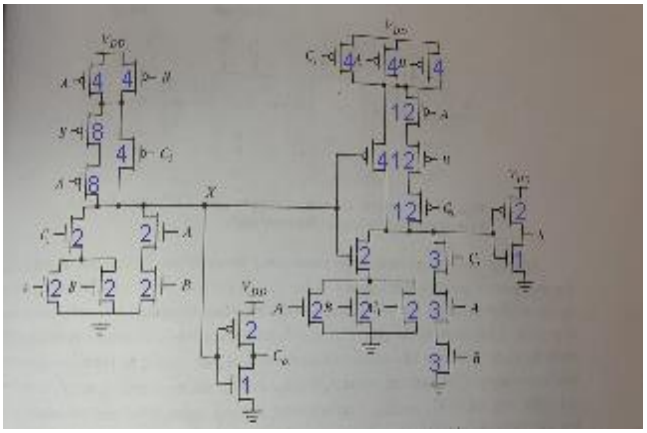


Figure 1: Complementary static CMOS full adder with finger width

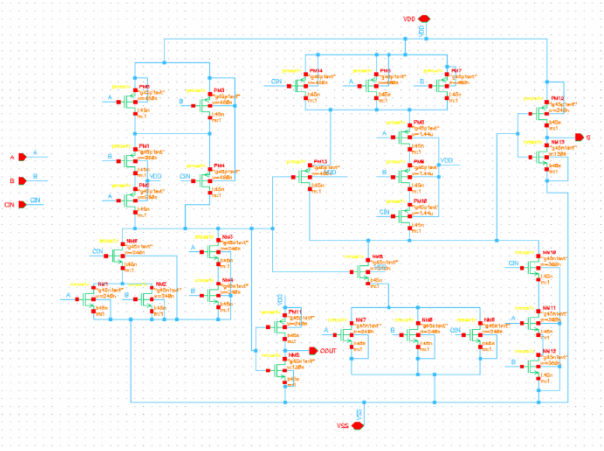


Figure 2: Schematic of 1-bit-adder

For circuit implementation, a 45 nm TSMC library was used. The gate length in the circuit was kept at a minimum of 45nm for the given technology node. Because electron mobility is nearly twice that of holes, the width of pmos is kept two times that of nmos to keep tpLH and tpHL similar.

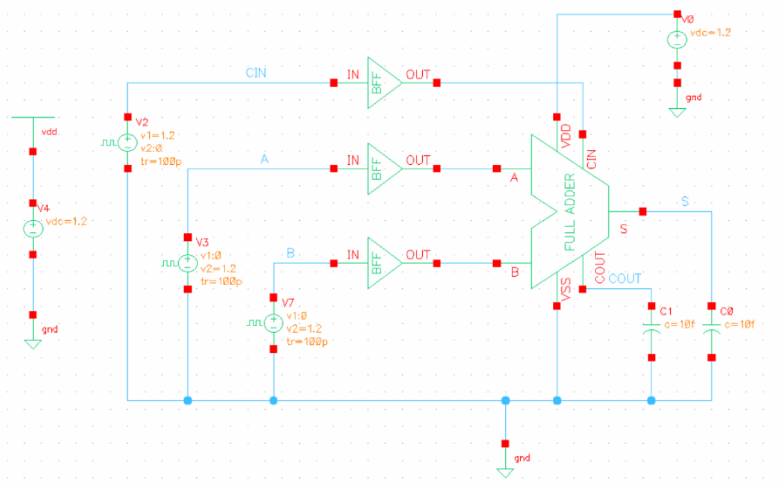
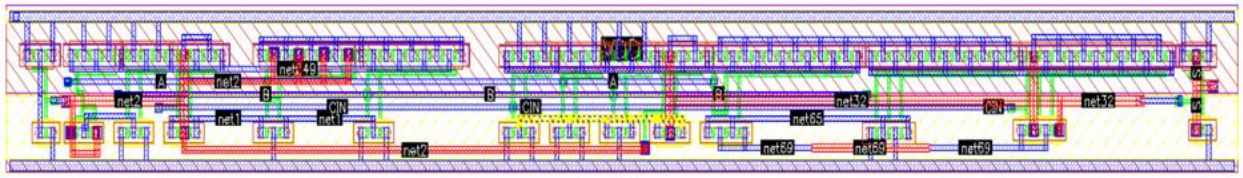


Figure 3: Testbench Schematic of 1-bit- adder

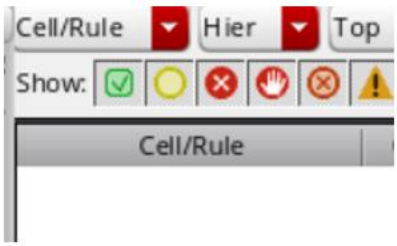
To make the tpHL and tpLH equal, we must make transistor sizing. So, we have taken the nmos and pmos transistors with gate length 45nm with a width of transistor 'W' 120nm. We have chosen the finger width as shown in the figure 1. It is selected in such a way that the difference between the tpLH and tpHL is almost zero. In addition, if there is a stack of two or three transistors, the width is doubled or tripled in that step to compensate for the stacking effect. For the whole circuit, pmos width is made twice compared to nmos to compensate hole and electron mobility mismatch and make tpLH equal to tpHL

We have also added buffer to each input as shown in figure 3 to prevent the signal source from being affected by whatever currents that the load may be produced with. A 10fF capacitor load is also given to both outputs of the adder.

Layout:



(a)



(b) (c)

Figure 4: Layout of 1-bit-full adder (a) Circuit layout (b) DRC clean report (c) LVS clean report

The above figure shows the layout of the 1-bit- full adder circuit with DRC and LVS clean results. As we have made transistor sizing with finger widths, the width of the transistors has increased with fingers which is greater than 120nm. But the height of every transistor is not affected. For the connections in the layout we have used M1 and M2 metal layers are used. For all three input connections M1 has been used and for some connections which are complicated M2 layer has been used. M2 is used as minimum as possible to avoid the overall delay. In the layout, only transistors of complementary adder circuits are used. Transistors of the buffer are not included, if it is included the overall area will increase.

Simulation results and analysis:

Figure 5 depicts the waveform of a functional simulation. A is toggled at a frequency of 1GHz in this input, while input B and input CIN are toggled at 0.5GHz and 0.25GHz, respectively. The waveform depicts the successful operation of a 1-bit full adder for all possible input combinations. The waveform is simulated using the previous section's schematic design at a temperature of 27 degrees Celsius and typical devices (TT).

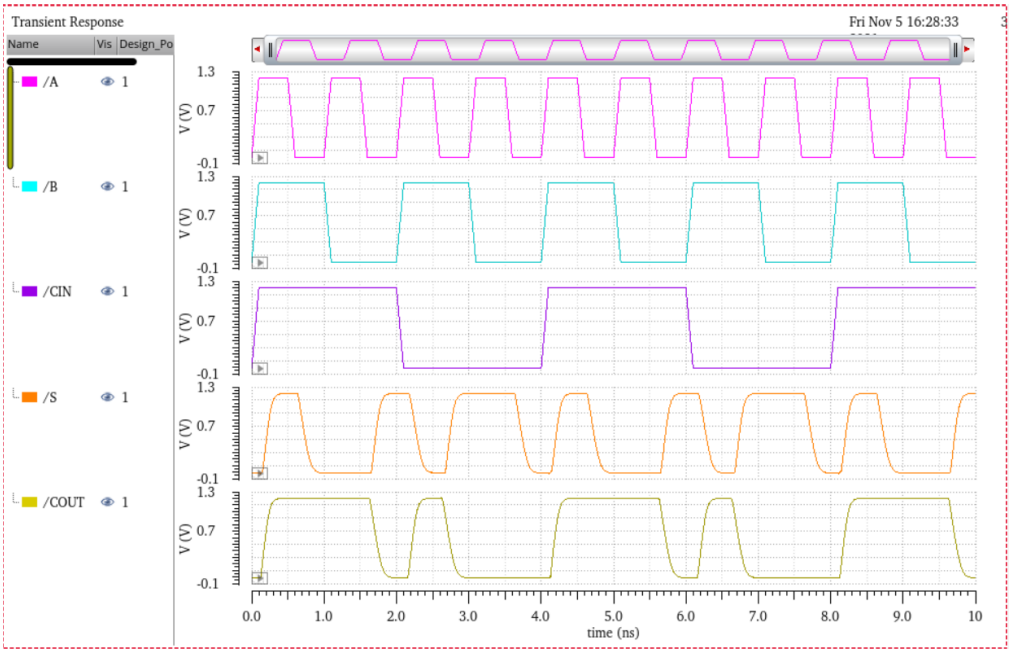


Figure 5: 1-bit full adder simulation waveform for all input combination

We simulate the outputs for all possible combinations of inputs and toggle the result for each of them to understand the propagation delay (for corner TT and temperature 27C). To do so, we simulate all 64 feasible input transitions. The worst possible delay for each combination of inputs is shown in table 1 for both schematic (pre-layout simulation) and layout (post-layout simulation).1-bit full adder simulation waveform for all input combination

The worst-case for each combination happens when all input toggles. For example, the propagation delay of sum S is maximum for case A=1, B=1, CIN=0. This is because there will be a greater number of transitions when (A, B, CIN) changes from (0, 0, 1) to (1, 1, 0). A similar trend can be observed for all possible combinations of inputs. It was observed that the schematic and layout showed worse delay for cases A=1, B=0, CIN=0. This can be because of a greater number of transitions as well as more loaded internal nodes for the case. It was also observed that the propagation delay of sum S and carry out COUT signal in layout was degraded. This is because of parasitics in the layout. The reduction in metal capacitance could improve the post-layout simulation result.

Now we evaluate the circuit by changing the process corners (FF, FS, SF, SS, and TT) as well as the temperatures (-25C and 27C) in the worst-case scenario where (A, B, CIN) changes from (0,0,1) to (1, 1, 0). Table 2 shows the propagation delay, average power, and power delay product. The delay is highest

at the SS corner, where both nmos and pmos are slow. The FF corner, on the other hand, has a minimal delay.

INPUT			OUTPUT		DELAY			
					Pre- Layout		Post-Layout	
A	B	CIN	S	COUT	S	COUT	S	COUT
0	0	0	0	0	170.3	156.5	259.3	239.6
0	0	1	1	0	222.7	179.7	366.4	284.9
0	1	0	1	0	198.4	165.7	326.6	264
0	1	1	0	1	196.7	173.9	356.1	288.4
1	0	0	1	0	196.6	173.9	356.8	288.6
1	0	1	0	1	198.3	165.9	326.6	264.2
1	1	0	0	1	222.8	179.6	366.6	265.1
1	1	1	1	1	170	156.5	259.1	239.6

Table 1: Propagation Delays for sum S and carry output COUT computation (For both pre-layout simulation and post-layout simulation)

Temp		CORNER				
		FF	FS	SF	SS	TT
27C	Delay(ps)	188	211.8	240.1	274.4	22.8
	Avg Power (uW)	40.64	39.27	39.68	38.37	39.4
	Power Delay product(fJ)	7.64032	8.31738	9.52716	10.52872	8.77832
-25C	Delay(ps)	154.9	176.1	200.2	231.2	186
	Avg Power (uW)	39.98	38.62	39.25	37.87	38.8
	Power Delay product(fJ)	6.19290	6.80098	7.85185	8.75554	7.2168

Table 2: Propagation Delays, Average Power and Power Delay Product for different corner (FF, FS, SF, SS and TT) and temperature (27C and -25C)

To analyze local mismatch, 100 Monte Carlo simulations are performed for the worst-case delay when (A, B, CIN) changes from (0, 0, 1) to (1, 1, 0) at 27C and 1.2V. We run a 100-sample simulation to evaluate the change in propagation delay and power.

	Min	Max	Mean	Std. Dev
Delay(ps)	217.7	229.2	223.2	2.845
Power(uw)	39.16	39.67	39.4	0.124

Table 3: Monte Carlo simulation results

Conclusion: The design of a 1-bit full adder circuit has been completed, and the layout has been implemented. The simulations of the circuit schematic and layout were compared. In the pre-layout simulation, the effect of global and local mismatch was also noticed. The influence of temperature was also studied. The project gave me a lot of knowledge of how to design sophisticated digital logic and the different design factors that must be considered. Furthermore, the project provided an excellent understanding of how to use cadence for circuit analysis and design, as well as insights into its numerous capabilities.