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ECE-637 PROJECT-1

Introduction:

A logic gate is an electronic device that implements a Boolean function. A logical operation is performed on one or more binary inputs to create a single binary output. In this project, we will design a simple Inverter, NAND, and NOR logic gates, both schematics and layouts in Cadence. And analyze the gates results such as Propagation Delay, Average Power, and PDP (Power Delay Product).

General specifications for all the Gates are as follows
45 nm CMOS technology with VDD = 1.2 V, Capacitive load = 2 fF, Wn = 120 nm, Wp = 2*Wn, Clock frequency = 1 GH.

Propagation delay = maximum (tpHL, tpLH); Average Power= average (Current)*VDD
% DIFF = ((Layout result – Schematic result)/Schematic result) *100

Part-1: Inverter

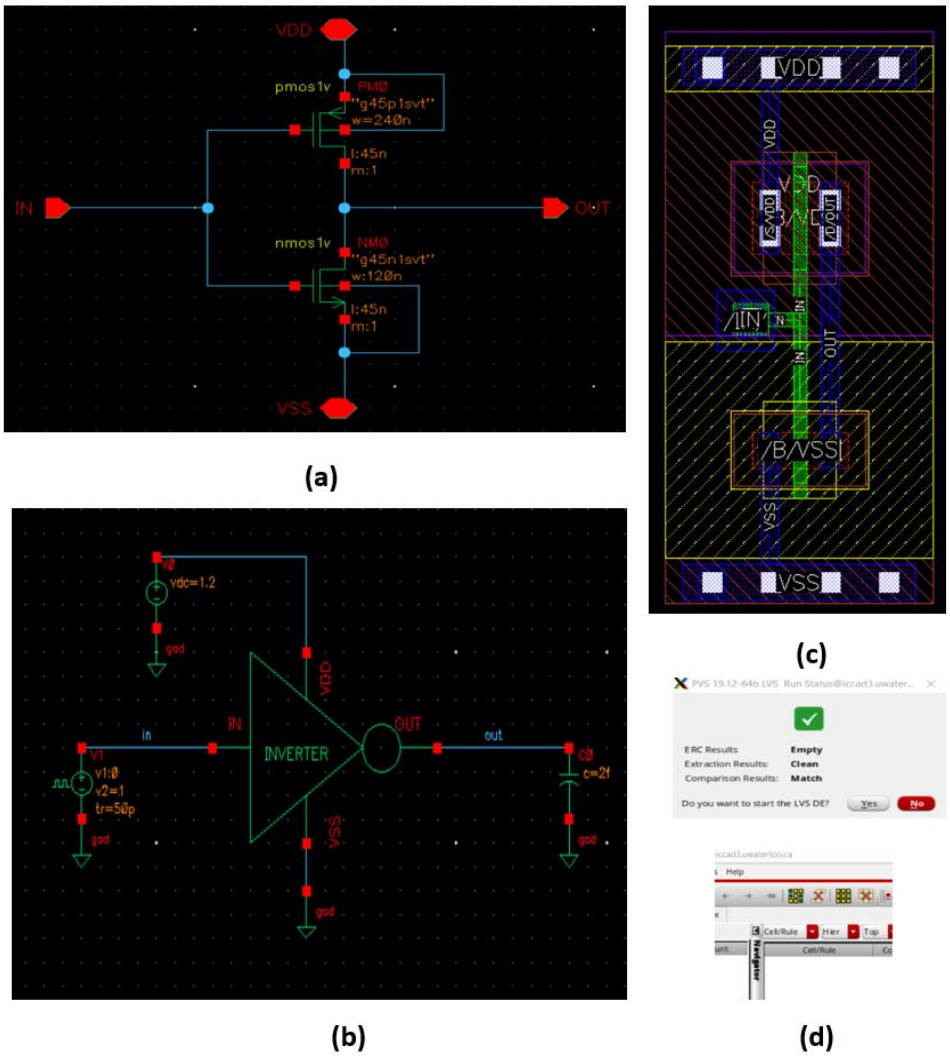

Fig-1: (a)Schematics (b) Test bench (c) Layout and (d) DRS and LVS results of Inverter.

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	INVERTER		
	Schematic	**Layout**	**DIFF %**
tpLH	27.15 ps	28.35 ps	4.41%
tpHL	31.97 ps	33.45ps	4.62%
Propagation delay	31.97 ps	33.45 ps	4.62%
Avg Power	3.295 uW	3.501uW	6.25%
PDP	0.105 fJ	0.117 fJ	11.42 %

Table 1: Propagation Delay, Average Power, and PDP of Inverter.

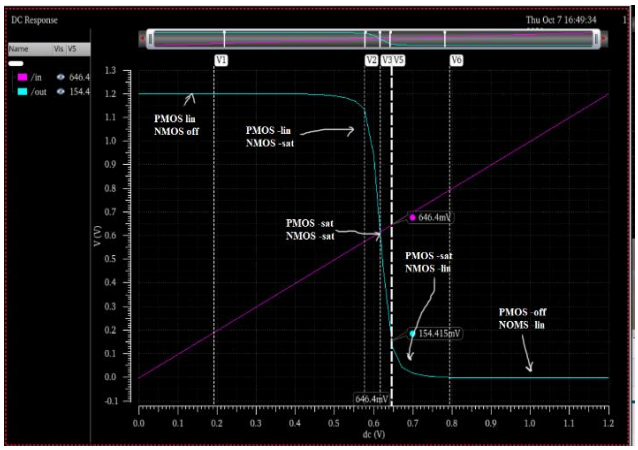
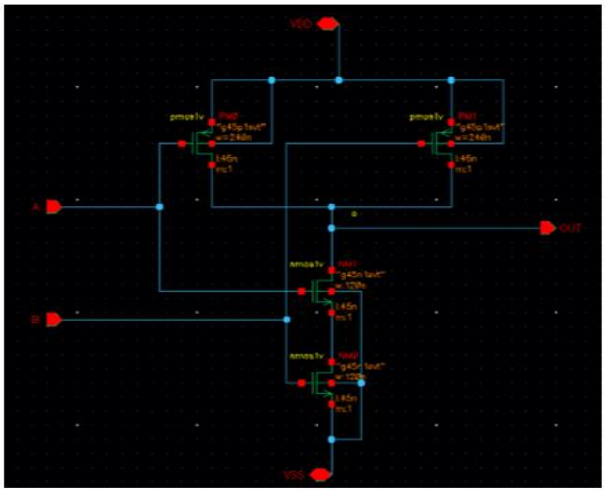
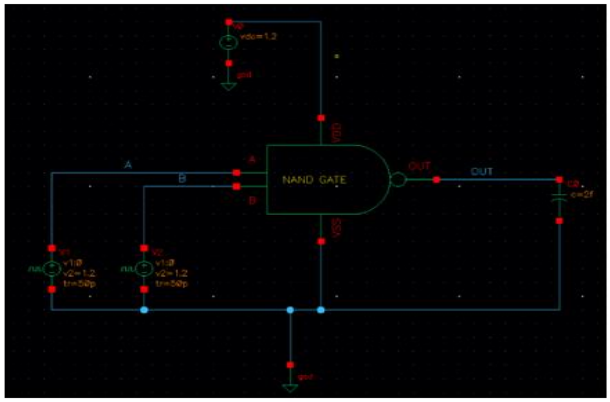


Fig-2 Voltage characteristics of the Inverter with five regions of operation

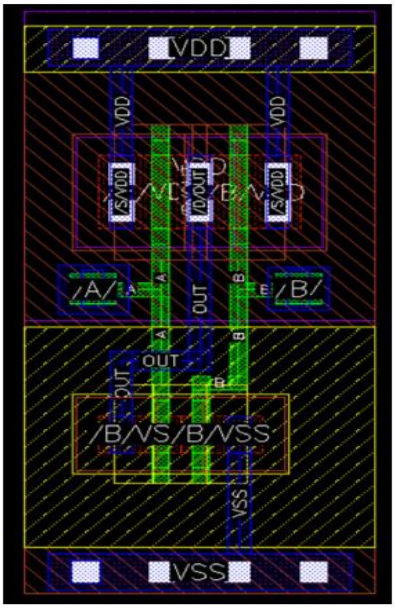
Part-2: NAND Gate



(a)



(b)



(c)

(d)

Fig-3: (a)Schematics (b) Test bench (c) Layout and (d) DRS and LVS results of NAND.

	NAND GATE		
	Schematic	**Layout**	**DIFF %**
tpLH	20.1ps	21.58 ps	7.36%
tpHL	52.96 ps	55.9 ps	5.55%
Propagation delay	52.96 ps	55.9 ps	5.55%
Avg Power	3.579uW	3.904uW	9.08%
PDP	0.189fJ	0.218fJ	15.34 %

Table 2: Propagation Delay, Average Power, , and PDP of NAND Gate.

	NOR GATE		
	Schematic	**Layout**	**DIFF %**
tpLH	43.2 ps	46.28 ps	7.12%
tpHL	23.29 ps	23.81 ps	2.23%
Propagation delay	43.2 ps	46.28 ps	7.12%
Avg Power	3.48 uW	3.792 uW	8.96%
PDP	0.150 fJ	0.175 fJ	16.6%

Table 3: Propagation Delay, Average Power and PDP of NOR Gate.

Part-3: NOR Gate

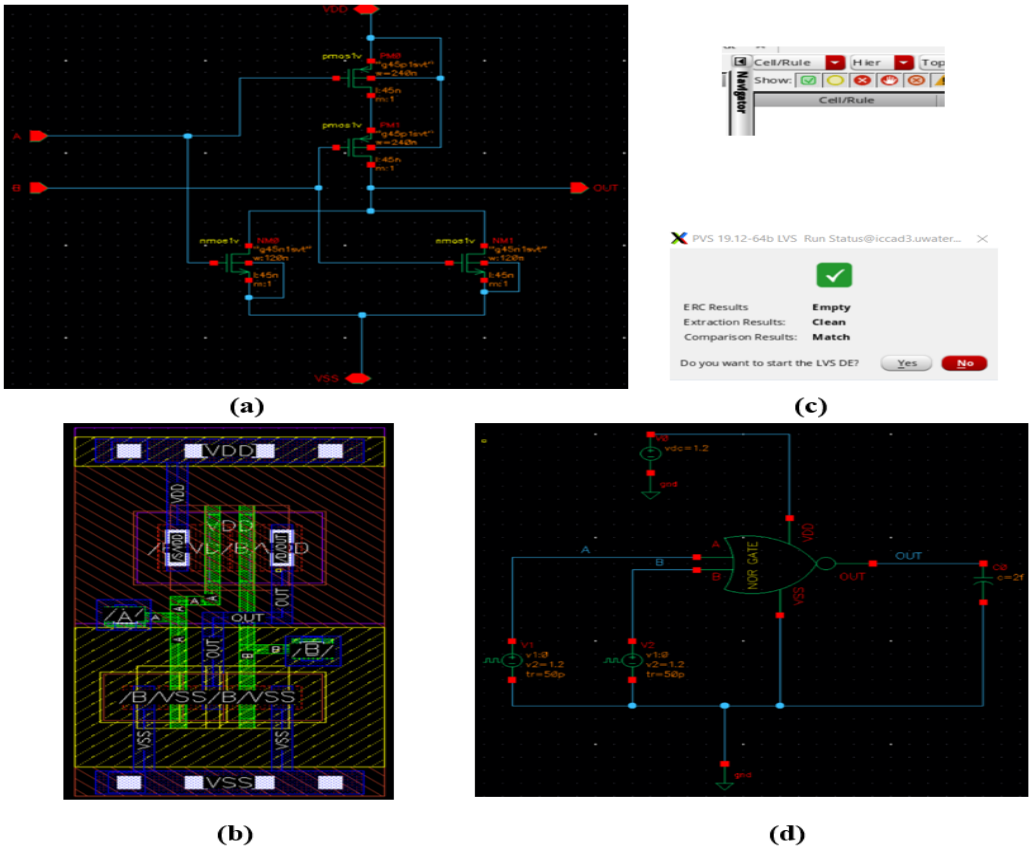


Fig-4: (a)Schematics (b) Layout (c) DRS and LVS results and (d) Test bench of NOR.

CONCLUSION: All three logic gates such as Inverter, NAND, and NOR have been designed. Various parameters like propagational delay, average power, and PDP have been calculated and observed the difference before and after post-layout simulation. There is a 4 to 10% percent change in the parameters due to parasitic extraction.