```
/*************************************************************************
* Date: Aug. 16, 2006
* File: Reg1.v (440 Examples)
*
* Model of a 32 bit register with an asynchronous reset (active low)
*************************************************************************/

//*********************************************************
module Reg32(Q, D, clk, reset_);
//*********************************************************

   output [31:0] Q;
   input  [31:0] D;
   input         clk, reset_;
   reg    [31:0] Q;

   always @(posedge clk or negedge reset)
   if (!reset_)
      Q <= 32'b0;
   else
      Q <= D;

endmodule
```