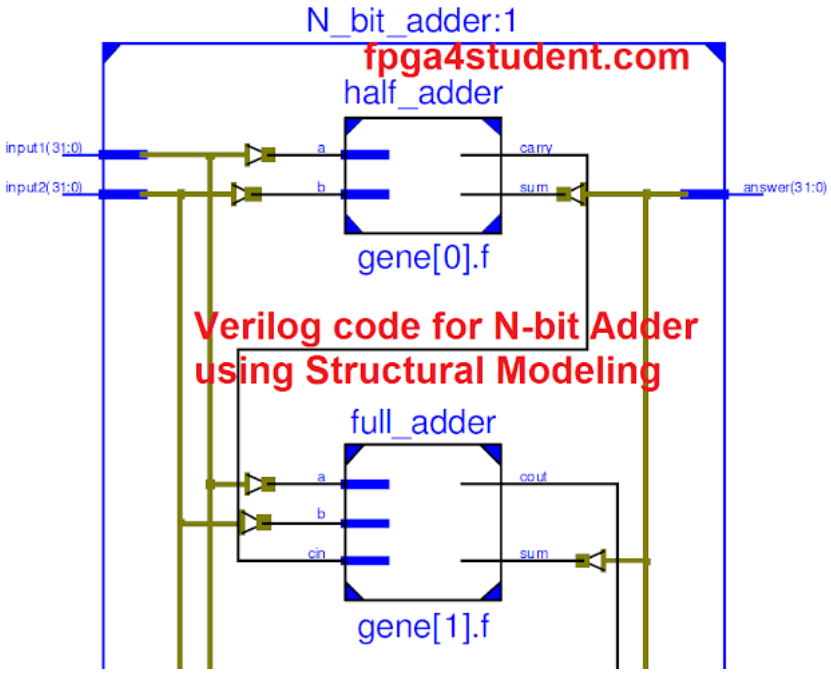
N-bit Adder Design in Verilog

The next Verilog/ VHDL project is a complete co-processor specially designed for cryptographic applications. The co-processor has standard instructions and dedicated function units specific for security. The co-processor is implemented mainly in VHDL, but the N-bit Adder is designed in Verilog. The Verilog code for the N-bit Adder will be instantiated later in a VHDL design. In next posts, implementations of major modules in the co-processor will be presented. The complete co-processor design and implementation will be presented after every part of the co-processor is posted.

This post presents Verilog code for N-bit Adder designed for the co-processor. The Verilog code for N-bit Adder is done by using Structural Modeling.



As shown in the above picture, the N-bit Adder is simply implemented by connecting 1 Half Adder and N-1 Full Adder in series. The Verilog code for N-bit Adder is designed so that the N value can be initialized independently for each instantiation. To do it, the Verilog code for N-bit A Generate Statement in Verilog to create a chain of full adders for implementing the N-bit Adder.

Verilog code for N-bit Adder using Structural Modeling:

```
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// Verilog project: Verilog code for N-bit Adder
// Top Level Verilog code for N-bit Adder using Structural Modeling
module N_bit_adder(input1,input2,answer);
parameter N=32;
input [N-1:0] input1,input2;
   output [N-1:0] answer;
   wire  carry_out;
  wire [N-1:0] carry;
   genvar i;
   generate
   for(i=0;i<N;i=i+1)
     begin: generate_N_bit_Adder
   if(i==0)
```

```
  half_adder f(input1[0],input2[0],answer[0],carry[0]);
   else
  full_adder f(input1[i],input2[i],carry[i-1],answer[i],carry[i]);
     end
  assign carry_out = carry[N-1];
   endgenerate
endmodule

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// Verilog project: Verilog code for N-bit Adder
// Verilog code for half adder
module half_adder(x,y,s,c);
   input x,y;
   output s,c;
   assign s=x^y;
   assign c=x&y;
endmodule // half adder

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// Verilog project: Verilog code for N-bit Adder
// Verilog code for full adder
module full_adder(x,y,c_in,s,c_out);
   input x,y,c_in;
   output s,c_out;
 assign s = (x^y) ^ c_in;
 assign c_out = (y&c_in)| (x&y) | (x&c_in);
endmodule // full_adder
```


Testbench Verilog code for N-bit Adder:

```
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// Testbench Verilog code for N-bit Adder
module tb_N_bit_adder;
 // Inputs
 reg [31:0] input1;
 reg [31:0] input2;
 // Outputs
 wire [31:0] answer;

 // Instantiate the Unit Under Test (UUT)
 N_bit_adder uut (
  .input1(input1),
  .input2(input2),
  .answer(answer)
 );

 initial begin
  // Initialize Inputs
  input1 = 1209;
  input2 = 4565;
  #100;
  // Add stimulus here
 end

endmodule
```
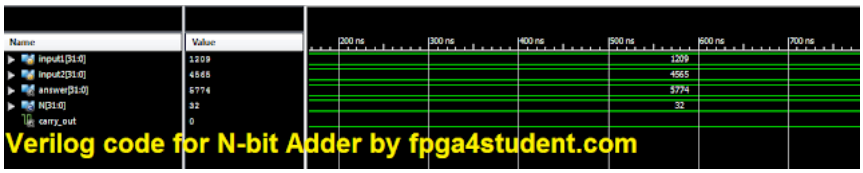


Simulation Waveform for the N-bit Adder:



By running the Testbench Verilog code for the N-bit Adder, we can verify the correctness of the N-bit Adder. The simulation waveform shows that the N-bit Adder accurately operates.

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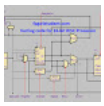

Verilog Code for 16-bit RISC Processor

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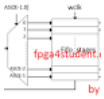

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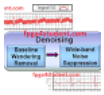

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