8/18/2018 Gates4 - HDLBits

Gates4 O

← vectorgates ② (/wiki/vectorgates)

vector3○ (/wiki/vector3) →

Build a combinational circuit with four inputs, in [3:0].

There are 3 outputs:

- out_and: output of a 4-input AND gate.
- out_or: output of a 4-input OR gate.
- out_xor: output of a 4-input XOR gate.

See also: Even wider gates O (/wiki/gates100).

```
Module Declaration
module top_module(
   input [3:0] in,
   output out_and,
   output out_or,
   output out_xor
);
```

Write your solution here

```
module top_module(
input [3:0] in,
output out_and,
output out_or,
output out_xor
);
endmodule
```

Submit

Submit (new window)

Upload a source file... ¥

Retrieved from "http://hdlbits.01xz.net/mw/index.php?title=Gates4&oldid=1317 (http://hdlbits.01xz.net/mw/index.php?title=Gates4&oldid=1317)"

Problem Set Contents

- Getting Started
- **▼ Verilog Language**
 - ▶ Basics
 - ▼ Vectors
 - ✔ Vectors (/wiki/vector0)
 - ♦ Vectors in more detail (/wiki/vector1)
 - ✔ Vector part select (/wiki/vector2)

 - Four-input gates (/wiki/gates4)
 - O Vector concatenation operator (/wiki/vector3)
 - O Vector reversal 1 (/wiki/vectorr)
 - O Replication operator (/wiki/vector4)
 - O More replication (/wiki/vector5)
 - ▶ Modules: Hierarchy
 - ▶ Procedures
 - ▶ More Verilog Features
- ▶ Circuits
- ▶ Verification: Reading Simulations
- ▶ Verification: Writing Testbenches