


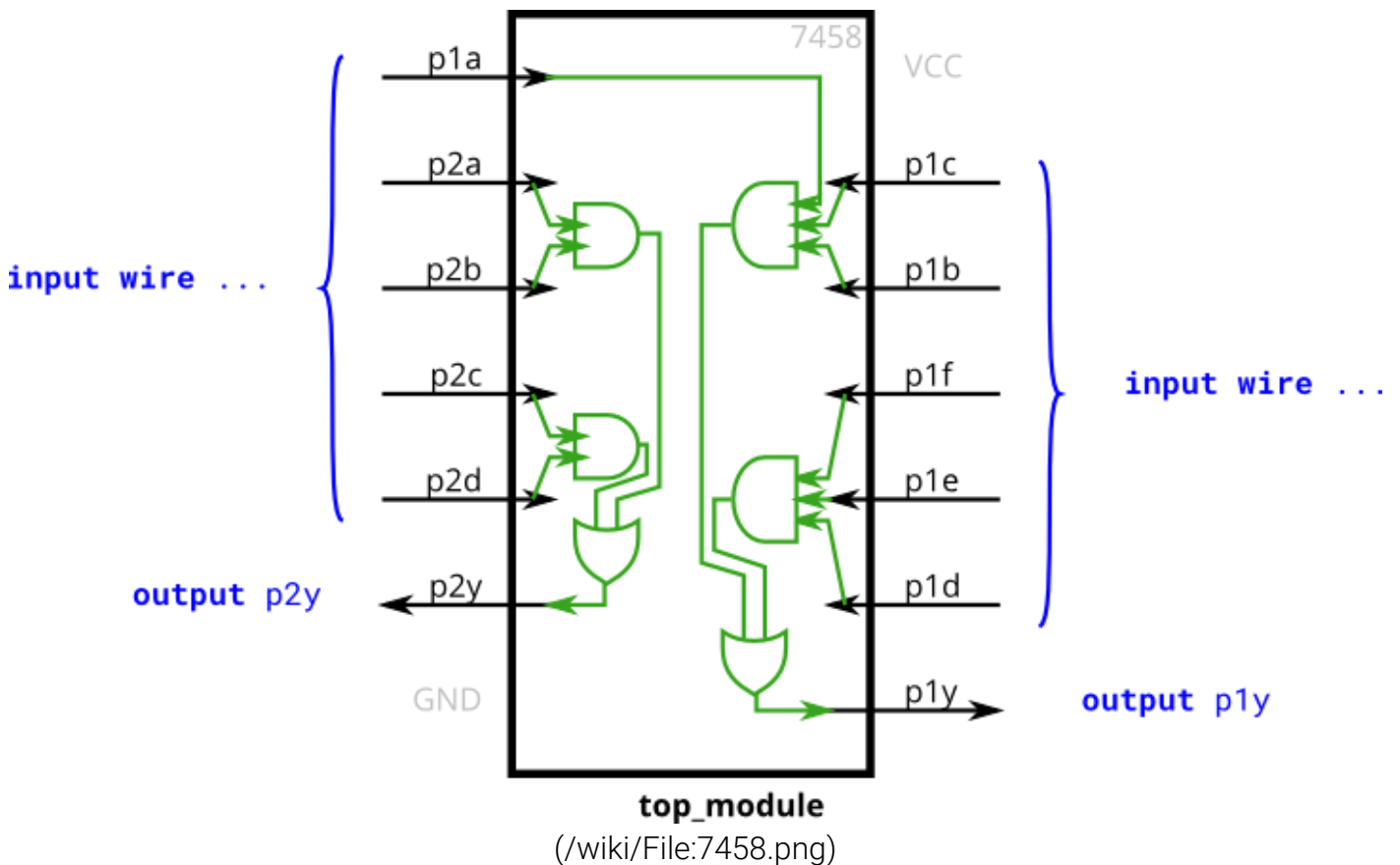
7458

[← wire_decl !\[\]\(666e09182d4cd268646ea700ea60dcdf_img.jpg\)](#) (/wiki/wire_decl)

[vector0 !\[\]\(c3d993ca47bfe2a953c700506ce31fa0_img.jpg\)](#) (</wiki/vector0>) [→](#)

The 7458 is a chip with four AND gates and two OR gates. This problem is slightly more complex than 7420  (</wiki/7420>).

Create a module with the same functionality as the 7458 chip. It has 10 inputs and 2 outputs. You may choose to use an assign statement to drive each of the output wires, or you may choose to declare (four) wires for use as intermediate signals, where each internal wire is driven by the output of one of the AND gates. For extra practice, try it both ways.



Expected solution length: Around 2–10 lines.

Module Declaration

```
module top_module (
    input p1a, p1b, p1c, p1d, p1e, p1f,
    output p1y,
    input p2a, p2b, p2c, p2d,
    output p2y );
```

[Hint...](#)

You need to drive two signals (p1y and p2y) with a value.



Write your solution here

```
1 module top_module (  
2     input p1a, p1b, p1c, p1d, p1e, p1f,  
3     output p1y,  
4     input p2a, p2b, p2c, p2d,  
5     output p2y );  
6  
7  
8 endmodule  
9
```

Submit

Submit (new window)

Upload a source file... 

 [wire_decl](/wiki/wire_decl) 

[vector0](/wiki/vector0)  









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