Notgate

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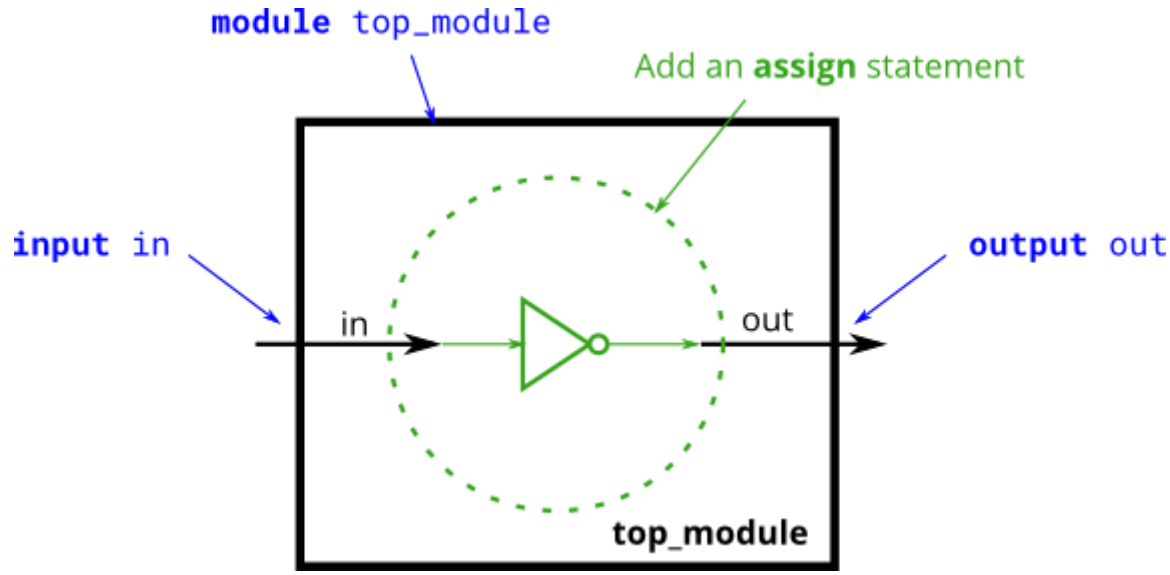
Create a module that implements a NOT gate.

This circuit is similar to wire (/wiki/wire), but with a slight difference. When making the connection from the wire `in` to the wire `out` we're going to implement an inverter (or "NOT-gate") instead of a plain wire.

Use an assign statement. The `assign` statement will *continuously (A change in the inputs immediately updates the output.) drive* the inverse of `in` onto wire `out`.



(/wiki/File:Notgate.png)

Expected solution length: *Around 1 line.*

Module Declaration

```
module top_module( input in, output out );
```

Hint...

Verilog has separate bitwise-NOT (~) and logical-NOT (!) operators, like C. Since we're working with a one-bit here, it doesn't matter which we choose.

Write your solution here

```
1 module top_module( input in, output out );
2
3 endmodule
4
```

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Solution

Show solution

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