Vectorr

← vector3 (/wiki/vector3)

vector4 (/wiki/vector4) →

Given an 8-bit input vector [7:0], reverse its bit ordering.

See also: Reversing a longer vector (/wiki/Vector100r).

Module Declaration

```
module top_module(
    input [7:0] in,
    output [7:0] out
);
```

Hint...

- `assign out[7:0] = in[0:7];` does not work because Verilog does not allow vector bit ordering to be flipped.
- The concatenation operator may save a bit of coding, allowing for 1 assign statement instead of 8.

Write your solution here

```
1 module top_module(
2     input [7:0] in,
3     output [7:0] out
4 );
5
6 endmodule
7
```

Submit | Submit (new window)

Upload a source file... ⌄⌄

Solution

Show solution

Problem Set Contents