

Vectorr ○

← vector3 ✓ (/wiki/vector3)

vector4 ○ (/wiki/vector4) →

Given an 8-bit input vector [7:0], reverse its bit ordering.

See also: Reversing a longer vector (/wiki/Vector100r).

Module Declaration

```
module top_module(  
    input [7:0] in,  
    output [7:0] out  
);
```

Hint...

Write your solution here

```
1 module top_module(  
2     input [7:0] in,  
3     output [7:0] out  
4 );  
5  
6 endmodule  
7
```

Submit

Submit (new window)

Or upload a file

Verilog source: vectorr.v

Upload and simulate

Solution

Show solution

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