```verilog
`timescale 1ns / 100ps

/***********************************************************************
 * Date: Aug. 28, 1999
 * File: Test Decoder 2 to 4.v    (440 Examples)
 *
 * Testbench to generate some stimulus and display the results for the
 * 2-to-4 decoder module.
 ***********************************************************************/

//*********************************************************
  module Test_decoder_2to4;
//*********************************************************
    wire  Y3, Y2, Y1, Y0;
    reg   A, B;
    reg   en;

    // Instantiate the Decoder (named DUT {device under test})
    decoder_2to4  DUT(Y3, Y2, Y1, Y0, A, B, en);

    initial  begin
       $timeformat(-9, 1, " ns", 6); #1;
       A  = 1'b0;          // time = 0
       B  = 1'b0;
       en = 1'b0;
       #9;
       en = 1'b1;       // time = 10
       #10;
       A  = 1'b0;
       B  = 1'b1;       // time = 20
       #10;
       A  = 1'b1;
       B  = 1'b0;       // time = 30
       #10;
       A  = 1'b1;
       B  = 1'b1;       // time = 40
       #5;
       en = 1'b0;       // time = 45
       #5;
    end

    always @(A or B or en)
       #1 $display("t=%t",$time," en=%b",en," A=%b",A," B=%b",B," Y=%b%b%b%b",Y3,Y2,Y1,Y0);

  endmodule
```