Module shift

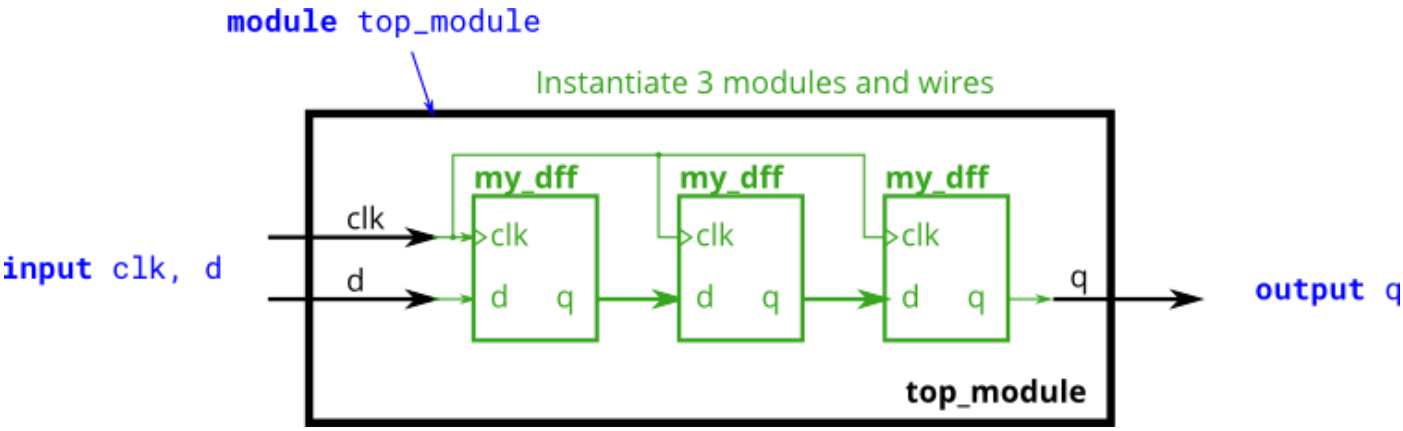
module_name (/wiki/module_name)

module_shift8 (/wiki/module_shift8)

You are given a module `my_dff` with two inputs and one output (that implements a D flip-flop). Instantiate three of them, then chain them together to make a shift register of length 3. The `clk` port needs to be connected to all instances.

The module provided to you is: `module my_dff ( input clk, input d, output q );`

Note that to make the internal connections, you will need to declare some wires. Be careful about naming your wires and module instances: the names must be unique.



(/wiki/File:Module_shift.png)

Module Declaration

```
module top_module ( input clk, input d, output q );
```

Write your solution here

```
1 module top_module ( input clk, input d, output q );
2
3 endmodule
4
```

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Solution

Complete problem first to see solution

module_name (/wiki/module_name)

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