

Vectorr

[← vector3 !\[\]\(666e09182d4cd268646ea700ea60dcdf_img.jpg\) \(/wiki/vector3\)](#)[vector4 !\[\]\(c3d993ca47bfe2a953c700506ce31fa0_img.jpg\) \(/wiki/vector4\) →](#)

Given an 8-bit input vector [7:0], reverse its bit ordering.

See also: Reversing a longer vector (/wiki/Vector100r).

Module Declaration

```
module top_module(  
    input [7:0] in,  
    output [7:0] out  
);
```

Hint...

- `assign out[7:0] = in[0:7];` does not work because Verilog does not allow vector bit ordering to be flipped.
- The concatenation operator may save a bit of coding, allowing for 1 assign statement instead of 8.

Write your solution here

```
1 module top_module(  
2     input [7:0] in,  
3     output [7:0] out  
4 );  
5  
6 endmodule  
7
```

Upload a source file... 

Solution

[← vector3 !\[\]\(1f56542a42e2413e44a2b2023033aa2e_img.jpg\) \(/wiki/vector3\)](#)

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