Smart Integrated Systems Laboratory

Working Progress for PhD course

Technical Report

A Considering to the NoC's saturation points with Injection-rate base-on Gem5 simulator

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Abstract

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1 Target and Scope of the Project

In this report, I would like to focus on some of the following tasks:

1. How to run Gem5 to build an computer architecture such as ARM, X86, RISC-V.
2. How to find out the saturation points of Network-on-Chip with diverse of benchmarks.
3. Understanding of Garnet2.0 to applying on new ideas for doing my thesis

2 Theoretical basics

3 The scenarios for doing the test

3.1 scenario 1:

3.2 Discussion and Conclusion

4 References

4.1 Gem5 Simulator

The Gem5 simulator is a modular platform that can be used for computer-systems architecture research. Gem5 includes many features such as Multiple interchangeable CPU models, A NoMali GPU model, Event-driven memory system, A trace-based CPU model that plays back elastic traces, which are dependency and timing annotated traces generated by a probe attached to the out-of-order CPU model; Homogeneous and heterogeneous multi-core; Multiple ISA support; **full-system capability**; Multi-system capability; Power and energy modeling and Co-simulation with SystemC.

All of the above features can reference from link-ref-for-Gem5 features in detail

In addition, Gem5 is also known as a modular discrete event driven computer system platform, in which can be understand via the following points:

1. The components in Gem5 can be changed and rearranged, parameterized, extended or replaced to suit our design.
2. Gem5 simulates the passing of time as a series of discrete events.

4.2 Garnet2.0

5 Theory and definition — Related works

6 Data and Results

7 Conclusion

Acknowledgements and References

References